3A PROCESSOR MAINTENANCE DATA

COMMON SYSTEMS

CONTENTS PAGE

1. GENERAL 5
A. Maintenance Operations 6
B. Backplane Tools and Materials . . 6
C. Backplane Wire Removal/Replacement Procedure 6
D. Circuit Pack Replacement Procedures 7
E. Optional Methods of Circuit Pack Replacement 14
F. Cautions Pertaining to Circuit Packs . 14
G. Maintenance Operations 14
2. 3A CENTRAL CONTROL 14
A. Description of 3A Instruction Set . 18
B. Generic Program Loading 19
C. Troubleshooting Aids 19
D. References 20
E. System Initialization 26
F. Manual Initialization Procedures . 26
G. Postmortem Output Message . . . 26
H. References 27
I. Memory Reload 39
J. Memory Reload Verification . . . 39
K. Troubleshooting Aids 39

CONTENTS PAGE

L. Overwrite 43
M. Setup Procedure 43
N. Overwrite Procedure 43
O. Overwrite File Administration . . 49
P. Manual Operation Procedures . . 64
Q. Panel Interrupts 64
R. Automatic Operations 83
S. Register Bit Assignments 83
T. Data Cartridge Insertion and Removal 93
U. Insertion of Data Cartridge . . . 93
V. Removal of Data Cartridge . . . 93
W. Generic Program Restarts 93
X. References 93
Y. 3A CC Diagnostic Test Sequence . 103
3. INPUT/OUTPUT 107
A. Physical Layout 107
B. Remote Serial Interface (RSI) . . 107
C. Parallel Channel Interface (PCI) . 111
D. Direct Memory Access 116
E. CTI Unit 116
4. MAIN STORE (MAS) 118

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CONTENTS PAGE

A. Physical Layout 118

B. MAS Verification Procedures . . . 118

C. MAS Utility Functions 118

5. MAINTENANCE FRAME 124

A. Physical Layout 124

B. System Status Panel Verification and Operation 124

C. Tape Data Controller (TDC) Verification and Operation 124

6. PROGRAMMABLE MAGNETIC TAPE SYSTEM 141

A. Physical Layout 141

B. Verification and Diagnostics . . . 141

7. TTY AND TTYC VERIFICATION 145

A. Physical Layout 145

B. TTY and TTYC Verification and Diagnostic 145

8. POWER 157

A. Physical Layout 157

B. Frame Power Distribution 157

9. SUPPLEMENTARY REFERENCE MATERIAL . 164

SCHEMATIC DRAWING INDEX 164

INDEX TO EOS DOCUMENTS 165

Figures

1. Duplex 3A Processor Frame 169

2. 3A Processor with Supplementary Store . 170

3. Wire Wrap Repair Procedures 171

CONTENTS PAGE

4. 3A Processor Frame and Mounting Plate Numbering 180

5. Maintenance Frame Equipment and Mounting Plate Numbering 181

6. 947-Type Connector Pin Numbering . . 182

7. Relay Contact Numbering 183

8. 3A CC Control Panel 184

9. 3A CC Interior 185

10. 3A CC Circuit Pack Locations 186

11. 3A CC Instruction Set Layouts . . . 187

12. DMA Unit 188

13. PCH Unit 188

14. CTI/Power Unit 189

15. CTI/Power Unit Component Locations . 190

16. MASC and Memory Unit Circuit Pack Locations 191

17. Maintenance Frame 192

18. System Status Panel (No. 3 ESS) . . 193

19. System Status Panel (TNS) 193

20. System Status Panel (No. 5 ETS) . . 194

21. System Status Panel (No. 2B ESS) . . 194

22. System Status Panel Controller . . . 195

23. System Status Panel and Relay Unit J1C056A 196

24. System Status Panel and Relay Unit, Rear View 197

25. Tape Data Controller 0 or 1, Front View 197

26. Tape Data Controller 0 or 1, Rear View 198

CONTENTS PAGE

27. Cartridge Tape Transport KS-21447, L2 . 199
28. PROMATS Frame 200
29. PROMATS Frame, Upper Section . . . 201
30. Display Control Panel, Front View . . 202
31. Tape Transport and Power Supply . . 203
32. Power Supply KS-21104, L3 Interior View 203
33. Teletypewriter Controller J1C054A . . 204
34. Processor Frame Power Unit 205
35. Maintenance Frame Power Unit J1C061A 206
36. Maintenance Frame Power Unit Component Locations 207
37. Maintenance Frame Power Unit Component Locations, Rear 208
38. Maintenance Frame Power Distribution . 209
39. Connector and CTF Locations 210

Tables

A. List of 3A Processor Circuit Packs and Locations 8
B. Circuit Pack Replacement Procedures 11
C. 3A CC Control Panel Keys, Lamps, and Switches 15
D. Generic Loading Verification Reference Documents 20
E. Generic Loading Verification Procedures—EOS 21
F. Postmortem 32-Word Group Format . 28

CONTENTS PAGE

G. Automatic System Initialization Output Messages 32
H. Manually Generated Initialization—EOS 33
I. No. 2B ESS Initializations 35
J. No. 3 ESS Initializations 36
K. ETS Initializations 36
L. System Initialization Reference Documents 37
M. Setting Software Clock—All Systems 38
N. Memory Reload Verification Procedures 40
O. Memory Reload Verification Reference Documents 42
P. Overwrite Procedure—EOS . . . 44
Q. Determining Overwrite Status . . 50
R. Activate an Overwrite 51
S. Deactivate an Overwrite 52
T. Remove Deactivated Overwrite . . 53
U. List Overwrite Data 54
V. Generic and Issue Header Insertion . 56
W. Replace GENID and ISSID 56
X. Loading New or Old Data . . . 58
Y. Generating Overwrite Check Numbers 60
Z. Display a General Register . . . 65
AA. Load and Display a General Register 66

CONTENTS PAGE

AB. Load a General Register with Incorrect Parity 67
AC. Display a Special Register 68
AD. Load and Display a Special Register 69
AE. Load a Special Register with Incorrect Parity 70
AF. Display Contents of Store 71
AG. Display Consecutive Contents of Store 72
AH. Write Contents of Store 73
AI. Write Consecutive Contents of Store . 74
AJ. Compare Address 75
AK. Compare Data 77
AL. Compare Address and Data . . . 78
AM. Execute a Program 81
AN. Execute a Program Step-by-Step . 82
AO. TTY Commands 83
AP. 3A CC Reference Documents . . . 84
AQ. Microcontrol Status Register Bit Assignments 85
AR. System Status Register Bit Assignments 86
AS. Store Address Register Bit Assignments 88
AT. Maintenance Status Register Bit Assignments 89
AU. Main Memory Status Register Bit Assignments 90
AV. Interrupt Set Register Bit Assignments 91
AW. Error Register Bit Assignments . . 92

CONTENTS PAGE

AX. Data Cartridge Insertion - EOS . . 94
AY. Data Cartridge Insertion - 2B ESS . 96
AZ. Data Cartridge Insertion - No. 3 ESS 97
BA. Data Cartridge Removal - EOS . . 98
BB. Data Cartridge Removal - No. 2B and No. 3 ESS 99
BC. Generic Program Restarts - EOS . 100
BD. Data Cartridge Reference Documents 102
BE. 3A CC Diagnostic Test Sequence . 104
BF. RSI Verification Procedure 107
BG. Diagnostic Request Formats . . . 108
BH. RSI Diagnostic Test Numbers . . . 109
BI. RSI Reference Documents 110
BJ. PCH Verification Procedures . . . 111
BK. PCH Diagnostic Test Numbers . . 112
BL. PCH Reference Documents . . . 112
BM. DMA Verification Procedure . . . 113
BN. DMA Diagnostic Test Numbers . . 114
BO. DMA Reference Documents . . . 115
BP. CTI Unit Verification Procedure . . 116
BQ. CTI Unit Diagnostic Test Numbers . 116
BR. CTI Unit Reference Documents . . 117
BS. Typical Designations and Functions of MAS Bus Leads 119
BT. MAS Audit Control 120
BU. MAS Manual Requests 120
BV. MAS Audit Results 121

CONTENTS PAGE

BW. MAS Utilities 122
BX. MAS Error Recovery 123
BY. MAS Reference Documents . . . 123
BZ. EOS SSP Key Buffer—Bit Assignments 125
CA. EOS SSP Status Buffer—Bit Assignments 126
CB. System Status and Control . . . 127
CC. System Emergency Manual Control—Controls/Indicators 129
CD. SSP Reference Documents 131
CE. TDC Cartridge Removal Procedure . 132
CF. TDC Cartridge Insertion Procedure . 133
CG. TDC Verification Procedure . . . 134
CH. TDC Diagnostic Test Numbers . . 135
CI. CTT Controller Commands and Functions 136
CJ. TDC Reference Documents (to be supplied) 140
CK. PROMATS Verification Procedure . 141
CL. PROMATS Diagnostic Test Numbers . 142
CM. PROMATS Reference Documents . . 144
CN. TTY and TTYC Verification . . . 146
CO. TTYC Diagnostic Test Sequence . . 147
CP. TTY and TTYC Reference Documents 148
CQ. TTY Responses 149
CR. Binary/Decimal Conversion Table . 151
CS. Octal/Decimal Conversion Table . . 152

CONTENTS PAGE

CT. Hexadecimal/Decimal Conversion Table 153
CU. ASCII Hex/Octal Conversion Table . 155
CV. KS-21104 Power Converter Fuses . 157
CW. Processor Frame Fuse Assignments . 158
CX. CTI/Power Unit Fuses 162
CY. Maintenance Frame Fuses 163

1. GENERAL

1.01 This section provides maintenance data pertinent to the 3A Processor.

1.02 When this section is reissued, the reason(s) for reissue will be listed in this paragraph.

1.03 This maintenance and operations manual is intended to provide the experienced maintenance technician with abbreviated information techniques and procedures for operating, diagnosing, and maintaining a 3A Processor. See Fig. 1 and 2.

1.04 This manual is divided into sections which are concerned with the major functional units of a 3A Processor. Each section attempts to collect in one place relevant data to serve as "memory joggers" for each functional area of a 3A Processor.

1.05 Certain units and operations that are treated in this manual may not be present or required in all systems, depending on the particular application. These portions of this manual should be disregarded when the information does not pertain to the system being used.

1.06 This manual is not intended to be a tutorial or an ordered list of operations to be performed. It is a collection of data and procedures, any part of which may be used as a particular situation may require.

A. Maintenance Operations

1.07 Backup assistance is available whenever needed so that system downtime can be minimized. The following guidelines are provided to aid in making a decision to call in outside aid:

(1) When a 3A Central Control (CC) goes out of service and cannot be restored within ten minutes, the Switching Control Center (SCC), or equivalent, should be notified.

(2) The Technical Assistance Center (TAC), or equivalent, should be notified in not more than one hour.

(3) The Western Electric (WE) Regional Product Engineering Control Center (PECC) should be contacted in not more than four hours.

(4) If the trouble is still not corrected, the WE system PECC must be contacted within eight hours.

(5) In case of a total outage the regional PECC should be notified within ten minutes, and the system PECC within 20 minutes. The following information should be collected before calling:

- Broadcast warning messages applied to the 3A Processor
- Recent Change Notices installed
- Recent history
- Occurrences of initialization
- Hardware and software problems
- State of 3A Processor before system failure.

B. Backplane Tools and Materials

1.08 The following tools and materials are normally required for removing and replacing backplane wires:

ID NUMBER	EQUIPMENT
ITE-4525A	Tone buzzer
TK-828	Midget tool kit
R-443D	Tweezer
R-4437	Battery powered wire-wrap gun
R-4444	Heat gun
R-4475	Terminal markers
R-4554	Magnifying lens
R-4559	Wire probe
R-4563	Polyimide sleeving
R-4584	28- and 30-gauge wire stripper
R-4621	Wire unwrapper
R-4622	6-inch wire-wrap extension
R-4668	Wire underpass tool
900289703	Filament scissors
RM-628437	Teflon sleeving
RM-583101	Fiber sheet
KS-21336,L1	28-gauge wire, green
KS-21336,L1	30-gauge wire, green

C. Backplane Wire Removal/Replacement Procedure

1.09 To prevent damage to MLPWB backplane wires during removal and replacement, it is important that the procedures shown in Fig. 3 be followed exactly.

1.10 Equipment locations are made up of two elements: the mounting plate number and the circuit pack position number. The schematic drawing for a particular unit depicts unit equipment locations and the schematic drawing for the frame depicts frame equipment locations. For example, a unit 06-22 equipment location corresponds to 054-22 frame equipment location. The prefix 0 in the number 054 indicates frame 0 and a 1 indicates frame 1.

D. Circuit Pack Replacement Procedures

1.11 When it is necessary to remove and replace a circuit pack, the correct procedure must be followed and the circuit packs must be handled with care. Read paragraph 1.13, "Cautions Pertaining to Circuit Packs" before replacing a pack. Diagnostic output messages identify circuit packs that appear to be faulty to the diagnostics. Refer to Table A of this section for a listing of 3A Processor circuit packs and locations or consult the Output Message Manual and the Trouble Locating Manual (TLM) for details on identifying a specific circuit pack location, code, and series. When replacing a series of circuit packs one at a time, execute the appropriate diagnostic after each replacement to determine if the fault has been cleared. If the fault has not been cleared, reinsert the original circuit pack in its location before removing and inserting the next circuit pack (the TLM provides a list of the order of replacement). Always check the code and series on the circuit pack handle and be certain that the codes match between the original and replacement circuit packs. Table B provides a procedure to follow when replacing circuit packs. Procedures may vary according to system application; nevertheless, always follow the procedures for the system application to avoid service interruption and/or damage to the circuit pack.

TABLE A

LIST OF 3A PROCESSOR CIRCUIT PACKS AND LOCATIONS

PACK TYPE AND NUMBER	NOMENCLATURE	LOCATION
CP 01	Word Control	AM
CP 02	Word Control	AL
CP 03	Word Control	AK
CP 05	Status and Control	AJ
CP 07	Expander 1	AH
CP 09	Status Scanner 1	FA
CP 12	—48v Power Converter	EC
CP 34	Cross Connect and Test	AG
CP 35	Status Scanner 2	EB
CP 35	Status Scanner 3	EA
CP 37	Combined I/O	AA, AB,AC, AD
CP 48	Word Control	AF
FA 1010	Bit Slice Bd 1	06-09, 10, 11, 12, 13 14, 15, 16, 17, 18
FA 1011	From 4/8 Decoder	06-33
FA 1012	DMU Bd 1	06-22
FA 1012	DMU Bd 1	06-24, 25
FA 1012	DMU Bd 2	06-27
FA 1014	DMU Bd 3	06-28
FA 1015	DMU Bd 4	06-23
FA 1015	DMU Bd 5	06-26
FA 1016	Microcontrol Bd 1	02-35
FA 1017	Microcontrol Bd 2	02-34
FA 1018	Microcontrol Bd 3	02-33
FA 1019	Microcontrol Bd 4	06-32
FA 1020	Microcontrol Bd 5	06-14
FA 1021	Microcontrol Bd 6	06-35
FA 1022	Microcontrol Bd 7	02-32
FA 1023	Microcontrol Bd 8	02-31
FA 1024	Bit Slice Bd 2	02-16, 17, 18
FA 1024	Bit Slice Bd 3	02-8, 9, 10, 12, 13
FA 1025	Clock	06-31
FA 1026	DMU Bd 2	06-21
FA 1027	Error Reg Bd 1	10-23
FA 1028	Error Reg Bd 2	10-22
FA 1030	Misc Decoder and Bit Slice High	02-19
FA 1031	4/8 Checker	02-02
FA 1031	4/8 Checker	06-04
FA 1033	Program Timer Counters	02-25
FA 1034	Console and 3A CC Interface	06-06

TABLE A (Contd)

LIST OF 3A PROCESSOR CIRCUIT PACKS AND LOCATIONS

PACK TYPE AND NUMBER	NOMENCLATURE	LOCATION
FA 1035	MCh Bd 3	02-28
FA 1036	MCh Bd 3	02-27
FA 1037	MCh Bd 3	02-26
FA 1038	I/O Bd 1	10-03
FA 1038	I/O Bd 1 Ch 1	10-07
FA 1038	I/O Bd 1 Ch 2	10-11
FA 1039	I/O Bd 2	10-04
FA 1039	I/O Bd 2 Ch 1	10-08
FA 1039	I/O Bd 2 Ch 2	10-12
FA 1040	Ext MAS Interface	02-05
FA 1040	Ext MAS Interface	02-06
FA 1040	Ext MAS Interface	02-07
FA 1046	Double Store Read	02-23
FA 1095	TO 4/8 Decoder	06-34
FA 1100	Panel Interface	056-21, 22, 23, 24
FA 1101	I/O Interface	056-25
FA 1101	I/O Interface	056-26
FA 1103	E2A Interface	056-17, 18, 19
FA 1211		066-02-10, 14
FA 1212		066-02-02
FA 1213		066-02-06
FB 6	Fuse Pack	72-01, 12, 03, 04
FB 152	+12v Reference	056-03
FB 152	+12v Reference	10-28
FB 374	MPCH Address	072-28
FB 375	MPCH Information	072-29, 31
FB 378	SPCH Information	072-32, 35, 38, 41
FB 379	SPCH Control, Address	072-33,34,36,37, 39, 40, 42, 43
FB 382	DMA Register 1	072-10, 12, 13, 14
FB 383	DMA Register 2	072-9
FB 384	DMA Register 3	
FB385	Add 1	
FB 386	Comparator	
FB 387	DMA Control	072-26
FB 388	CC Interface	072-23
FB 389	DMA Priority	072-22
FB 390	Status 1	072-21
FB 391	DMA Status 2	
FB 392	DMA Store Bus Control	072-16, 17
FB 486	Crystal Oscillator	06-29

TABLE A (Contd)

LIST OF 3A PROCESSOR CIRCUIT PACKS AND LOCATIONS

PACK TYPE AND NUMBER	NOMENCLATURE	LOCATION
FC 201	I/O Subchannel Ch 0	
FC 201	I/O Subchannel Ch 1	10-09
FC 201	I/O Subchannel Ch 2	10-13, 14
FC 202	Mtce Interface	02-26
FC 208	I/O Interface	056-28
FC 209	Relay Driver	056-16
FC 21	+3v Regulator	02-01
FC 21	+3v Regulator	02-21
FC 21	+3v Regulator	02-44
FC 21	+3v Regulator	056-02
FC 21	+3v Regulator	06-01, 02
FC 21	+3v Regulator	06-44
FC 21	+3v Regulator	10-01
FC 21	+3v Regulator	10-29
FC 22		066-02-01
FC 373	MPCH Control	078-16
FC 374	MPCH Address	078-18
FC 375	MPCH Information Circuit	078-20
FC 378	Information Circuit	078-04, 07, 10, 23, 26
FC 379	SPCH Control, Address	078-05, 06, 08, 09, 11, 12, 24, 25 27, 29, 32, 33, 35, 38, 39
FC 393	DMAR	072-05
FC 93	MPCH Control	072-27
JK 00	TDC 062-070	
JK 05	SPI Interface A	05-34
JK 06	SPI Interface B	05-33
JK 07	SPI Interface C	05-32
JK 08	Bus Terminator	05-17
JK 09	Bus Terminator	05-16
JK 11	Buffer	05-31
JK 12	Buffer	05-29
JK 13	Buffer	05-28
JK 14	Sync Data Set Ctlr A	05-27
JK 15	Sync Data Set Ctlr B	05-24
JK 16	Tape Controller A 05-22	
JK 17	Tape Controller B 05-21	
JK 18	Tape Controller C	05-20
JK 19	Tape Controller D	05-19

TABLE B

CIRCUIT PACK REPLACEMENT PROCEDURES

STEP	PROCEDURE	RESPONSE	REMARKS
			Caution: Read paragraph 1.13 "Cautions Pertaining to Circuit Pack Replacement" before changing circuit packs.
1	Observe SSP OUT-OF-SERVICE LED for the on-line 3A CC.	LED is off.	LED must be off.
	Enter on terminal: RMV:CU!	OK	Removes off-line 3A CC from service. If switch fails, call for assistance.
	On the SSP: Observe LOCK lamp for on-line 3A CC.	Off	
	Depress LOCK pushbutton for on-line 3A CC.	FORCE and SELECT lamps are lighted.	On-line 3A CC is forced to remain on-line.
2	At the off-line 3A CC Control Panel:		
	Depress MANUAL pushbutton.	MANUAL lamp lights (amber).	Off-line 3A CC manual state enabled.
	Depress POWER pushbutton.	POWER lamp is off.	***Note:*** If power cannot be removed from off-line 3A CC, check that on-line 3A CC is locked on-line. At rear of off-line 3A CC Control Panel, set locking toggle switch to TEST MODE and repeat Step 1 to remove power.
3	Replace circuit pack (refer to application Trouble Locating Manual [TLM] for the circuit pack number to replace).		***Caution:*** Check that pack type, number, and series are the same (code on pack handle).

TABLE B (Contd)

CIRCUIT PACK REPLACEMENT PROCEDURES

STEP	PROCEDURE	RESPONSE	REMARKS
4	At the 3A CC Control Panel:		
	Depress POWER pushbutton.	POWER lamp is lighted (green).	Restore power to 3A CC and its main store.
	Depress MANUAL pushbutton.	MANUAL lamp is off.	
5	If the 3A CCs were not switched (Step 1):		
	Enter on terminal:		
	SW:CU:UCL!	OK	Switches to the other 3A CC.
			If switch fails, call for assistance.
6	If diagnostics are being executed in REPEAT mode:		
	At the SSP:		
	Depress TEST CONTROL-EXECUTE pushbutton.	EXECUTE lamp is lighted.	Diagnostics are executed in REPEAT mode.
	Observe TEST CONTROL - PASS -FAIL lamps.	PASS is lighted.	All tests passed, return to procedure where fault was first indicated.
		FAIL is lighted.	Diagnostics failed.
	Depress TEST CONTROL—EXECUTE pushbutton.	EXECUTE is off.	Disables diagnostics REPEAT mode.
7	Replace the next circuit pack listed in TLM.		
	If the pack is an on-line pack, verify fault cleared.		

TABLE B (Contd)

CIRCUIT PACK REPLACEMENT PROCEDURES

STEP	PROCEDURE	RESPONSE	REMARKS
8	Execute the diagnostic that failed in the step mode.		When replacing a series of circuit packs, execute the diagnostic after each pack replacement to determine if fault cleared. If not cleared, reinsert original pack in its position before removing and replacing the next pack listed in the TLM.
9	At the SSP:		
	Depress PANEL POWER pushbuttons:		
	CIRCUIT POWER and LAMP POWER	Both are off.	Power removed for pack removal and replacement.
	Remove and replace circuit pack.		Check that replacement pack is the same as pack removed by code on handle.
10	At the SSP:		
	Depress PANEL POWER pushbuttons:		
	CIRCUIT POWER and LAMP POWER	Both are lighted.	Power is restored to circuit packs.
	Depress TEST CONTROL—EXECUTE pushbutton.	M tt DGN CU a COMPLETE ATP	Diagnostics completed and all tests passed.
			If diagnostics failed, repeat the replacement of packs until fault is cleared or all packs listed in TLM have been replaced.
			If fault is not cleared after all packs are replaced, call for assistance.
11	Enter on terminal:		
	CLR:RPT!	OK	Clears REPEAT mode.

E. Optional Methods of Circuit Pack Replacement

1.12 Optional or alternate methods of circuit pack replacement may be applicable to certain system applications. If alternate methods or procedures are applicable, follow the procedures to avoid service interruption or damage to equipment.

F. Cautions Pertaining to Circuit Packs

1.13 The following cautions relating to circuit packs should be observed.

(1) Circuit packs should be handled by their edges or faceplates to avoid deforming components and leads or scratching the gold-plated connector contacts. Touching connector contacts also contaminates gold plating and causes poor connections.

(2) Before removing or inserting a circuit pack, power must be removed from the circuit unless the Trouble Locating Manual indicates otherwise.

(3) When changing circuit packs in attempting to locate a trouble, always restore a pack to its original location if the replacement pack does not clear the trouble. This will aid in isolating the trouble by returning the circuit to the original configuration which existed at the time the failure was first detected.

(4) Always replace a circuit pack with a circuit pack having the same type, number, and series designators as the pack being replaced. All circuit packs are identified on their front handle by a unique code consisting of the circuit pack type, number, and series (for issue) designators. For example:

FC - Circuit Pack Type

398 - Number

1 - Series

G. Maintenance Operations

Processor Frame J1C106B-1

1.14 Figure 4 relates the unit and frame equipment locations for the 3A Processor frame as well as showing the J code and unit schematic drawing numbers.

Maintenance Frame J1C060A-1

1.15 Figure 5 relates the unit and frame equipment locations for the Maintenance Frame as well as showing the J codes and unit schematic drawing numbers.

Connector Pin Numbering 947A & B

1.16 Figure 6 shows the 947A and 947B connectors as seen from the rear of the frame.

1.17 In locating pins other than the coaxial terminating field (CTF) the row number and line number are used in combination to make up a 3-digit number. For example, terminal 215 indicates row 2, line 15.

1.18 The center pins are ground terminals and are usually noted as GRD0 and GRD1 counting from right to left from the rear.

1.19 The CTF terminals are numbers of two digits. The leftmost digit is the row number and the second digit is the line number. For example, terminal 23 indicates row 2, line 3.

Relay Winding and Spring Terminal Arrangement

1.20 Relay terminal number arrangements for AF-, AG-, AJ-, and AL-type relays that have 12 positions may be found in the upper half of Fig. 7.

1.21 Relay terminal number arrangements for AK- and AM-type relays are found in the lower half of Fig. 7.

2. 3A CENTRAL CONTROL

2.01 Figures 8, 9, and 10 depict the primary hardware elements of the 3A Central Control (3A CC). Table C gives additional information related to the 3A CC panel keys, lamps, and switches.

TABLE C

3A CENTRAL CONTROL PANEL KEYS, LAMPS, AND SWITCHES

AREA	DESIGNATION	COLOR	INDICATION OR FUNCTION
LOAD AND DISPLAY	0-19, PH, PL LEDs	Green	Visual indication of contents of the display buffer. The LEDs are divided into groups of three or four for easy conversion to either octal or hexadecimal. When all LEDs are lighted, it may indicate an erroneous request.
	0-19, PH, PL (switches)	Blue white gray	Manual input to the display buffer. Switches are divided into groups of three (by blue and white colors) for easy conversion to octal. Switches are also divided into groups of four for easy conversion to hexadecimal. PH (parity high) and PL (parity low) are used only when the ENABLE MANUAL PAR switch is operated.
	ENABLE	Gray	Allows manual setting of parity switches.
REGISTER SELECT	8, 4, 2, 1 (Switches)	White	Selects one of the 16 general or 16 special (panel addressable) registers.
	SPECIAL/GENERAL	White Switch	This switch in the down position selects the general register group. When in the up position, it selects the special register group. Either position is effective only when the EXECUTE switch is operated.
		Green LED	The GENERAL lamp indicates when this group has been selected. The SPECIAL lamp indicates that this group has been selected.
REGISTER	LOAD	White	Allows the contents of the load and display keys to be loaded into the register designated by the REGISTER SELECT switches (can only be performed when EXECUTE is operated).
	DISPLAY Switch	White	Allows the LOAD and DISPLAY lamps to display the contents of the register selected by the REGISTER SELECT switches (can only be performed when EXECUTE is operated).
COMPARE	ADR Switch	White	Enables the match between the contents of the store address register with the address input register masked by the address mask register.
	ENABLED LED	Green	Indicates when a COMPARE function is active.
	DATA Switch	White	Enables the match between the contents of the store data register and the data input register masked by the data mask register.

TABLE C (Contd)

3A CENTRAL CONTROL PANEL KEYS, LAMPS, AND SWITCHES

AREA	DESIGNATION	COLOR	INDICATION OR FUNCTION
MEMORY	INC ADR Switch	White	Increments the contents of the store address register by one following a manual store operation (can only be performed when EXECUTE is operated).
MEMORY	DISPLAY	White	Reads the main store at the address in the SAR and displays the contents of that loca-tion (can only be performed when EXECUTE is operated).
	HIGH BITS/ LOW BITS Switch	White	When in the down position, allows display or storage of bits 0 through 15 of data in a main store location. In the up position, bits 16 through 32 of a wide store will be displayed.
MODE	HALT	White	Puts the 3A CC in a microstore loop that executes no program code, but honors interrupts from the panel (can only be performed when EXECUTE is oper-ated).
	HALTED Switch	Green	Indicates that the 3A CC is in a halt loop.
	STEP Switch	White	Allows the execution of program in-instructions one at a time (only performed when EXECUTE is oper-ated).
	BASIC/ EXTENDED		Enables the HIGH BITS/ LOW BITS switch in the high position if the store is wider than 16 bits.
COMMAND	REJECT LED	Green	Indicates that the last manual function attempted was not performed. This may be due to an incorrect combination of panel keys.
	EXECUTE Switch	Gray	Initiates a microprogram interrupt that results in performance of the selected manual panel function.
STATUS	POWER Key/Lamp	Green	Depending on 3A CC state, operation causes a se-quential restoral of power to the 3A CC and its main store. Power removal occurs only if MANUAL is op-erated and 3A CC is either locked off-line or in test mode.
	ACTIVE Lamp	Green	Indicates status of the 3A CC. Follows the "one" side of the CC flipflop.
	NOT ACTIVE Lamp	White	Indicates status of the 3A CC. Follows the "zero" side of the CC flipflop.

TABLE C (Contd)

3A CENTRAL CONTROL PANEL KEYS, LAMPS, AND SWITCHES

AREA	DESIGNATION	COLOR	INDICATION OR FUNCTION
STATUS	MANUAL Key/Lamp	Amber	Operation enables the manual state in the not-active 3A CC only. The manual state permits panel load and display functions.
	ERROR Lamp	Red	STOP flipflop. This flipflop is set by error detection circuits or the other 3A CC and is cleared by initialization hardware or the other 3A CC. When this lamp is lighted, the 3A CC is in the STOP state.
	RESET CIRCUITS Key	White	Active only in the MANUAL mode. Initializes the critical flipflops and puts the 3A CC in the HALT state. The HALTED lamp is lighted.
	TEST MODE Lamp	Red	Lights only when the test mode switch (inside the control panel) is active. Test Mode switch enables panel functions in the on-line 3A CC and disables the program timer function. ***Caution:*** When this lamp is lighted, use of the control panel in the on-line system may cause interruption of service.
	LAMP & PWR TEST Key	White	Used to ensure that all lamps within STATUS area will light and to perform a test of the power alarm circuits in the power converters and FB152 circuit packs. The power converters are located within other units of the frame. When the key is operated, the converter LEDs will light. When the key is released, the converter LEDs will extinguish.

A. Description of 3A Instruction Set

Addressing Scheme

2.02 The 3A CC can access over a million words of memory via a 20-bit addressing arrangement. This 20-bit address is normally generated by incrementing the program address (PA) register by one on each memory access. However, any 20-bit address can be generated or obtained by any one of the following methods:

(a) The 20-bit address may be contained within a double word (two 16-bit words) instruction. In this case, bits 3 through 0 of the first word of the instruction correspond to bits 10 through 16 of the address; and bits 15 through 0 of the second word of the instruction correspond to bits 15 through 0 of the address. The addressing range is any location within 1,048,576 words.

(b) The 20-bit address may be generated by adding a 4-bit value (N) or a 12-bit value (K) to a general register pair (RP). The address base is continued in any RP from 0 to 14 (RP must be even).

(c) The 20-bit address may be generated by adding the contents of one general register to RA. The addressing range is any location from RA to (RA + 65,535).

(d) The 20-bit address may be generated by adding or subtracting an 8-bit number (OFFSET) to or from the contents of PA. The addressing range is any location from PA to (PA + or - 255).

(e) The 20-bit address may be generated by adding the contents of one of the general registers to PA + 1. The addressing range is any location from (PA + 1) to (PA + 65,535).

(f) The 20-bit address may be generated by combining 8 bits within the instruction for bits 7 through 0 of the address and 12 bits stored in the microprogram store for bits 8 through 19 of the address. The addressing range is any location within a 255-word boundary depending on the constant in microprogram store.

2.03 The basic instruction set is stored in the main store and each instruction is fetched via the main store bus when needed. Within each instruction is a 7-bit operation (OP) code. This OP code points the microprogram control of the 3A CC to a starting address for a microsequence which performs the desired function of the instruction.

2.04 The three types of instructions in the 3A basic and extended instruction set are the single word, double word, and triple word instructions (See Fig. 11). Single word instructions are the most commonly used within the system. Double word instructions are often used because either 16 bits of data or a 20-bit address is required in an instruction. Triple word instructions are used in multiple register manipulations.

2.05 The 3A CC instructions are general purpose in nature to enable reading from or writing into any of the general registers. Since most of the instructions allow any general register to be used, it is not necessary to move the data to a special register to perform a function.

2.06 The general formats for the instructions in the 3A CC systems are:

(a) RR—Register-to-register

(b) RN—Register and immediate operand

(c) RxR—References memory by adding an index register to an address register pair

(d) RxN—References memory by adding N or K to an address register pair

(e) CM—Communications instructions

(f) RI—Register and immediate data

(g) MM—Memory-to-memory

(h) SL—Specified 20-bit data to load a register pair of reference memory

(i) SB—Subroutine instructions

(j) SS—Specified 8-bit offset in branch operation

(k) MS—Miscellaneous instructions.

Each instruction format contains two parity bits, one branch allowed (BA) bit, and a 7-bit OP code.

Classes of Instructions

2.07 The instructions used in the 3A CC are divided into classes according to functions performed. These classes are:

(a) Data transfer instructions

(b) Branch instructions

(c) Arithmetic instructions

(d) Logic instructions

(e) Bit operation instructions

(f) Input/output instructions

(g) Maintenance instructions.

Data Transfer Instructions

2.08 The data transfer class of instructions controls the exchange of information within the system. These instructions are divided into the following subclasses:

(a) Memory-to-Register—This subclass involves the transfer of data from memory location to a 3A CC register.

(b) Register-to-Memory—This subclass involves the transfer of data from a 3A CC register to a memory location.

(c) Register-to-Register—This subclass involves a transfer of one of the 3A CC registers to any one of the other 3A CC registers.

(d) Memory-to-Memory—This subclass involves a transfer of data from one memory location to another memory location.

2.09 Refer to Section 254-340-102 for detailed explanations of the 3A CC basic and extended instruction set, and to Section 232-305-103 for the No. 2B ESS instruction set.

B. Generic Program Loading

2.10 The details necessary to load an application generic program into the Main Store of an Auxiliary 3A Processor in the EOS are provided. One Control Unit is placed in service and then it is used to bring the other Control Unit into service or to diagnose the alternate off-line unit if trouble is encountered. The procedures in this section are applicable only to the 3A Processor EOS. For the No. 2B Electronic Switching System (ESS) applications, the No. 3 ESS applications, and the 3A Processor applications, refer to the appropriate documents or BSPs referenced in Table D.

2.11 Procedures are provided for loading the generic program into main store when the main store has X-ray programs residing in it, and when it does not. Refer to the Generic Loading Verification Procedures (Table E) for specific procedures to follow.

- EOS provides a multiple generic capability for those applications requiring a large generic file. EOS supports the capability of including a second generic file (GENERIC2) on the cartridge tape. This capability permits applications to load a large generic file that extends beyond track 0 on the cartridge tape. Implementation of this capability splits the large generic into two generic files; the GENERIC file residing on track 0, and the GENERIC2 file residing on track 1. If the application does not need the multiple generic capability, the changes to implement it are invisible to single generic application users.

C. Troubleshooting Aids

2.12 If the generic program is not successfully loaded according to the procedures herein, it may be assumed that the control unit (CU) stopped because of a hardware or a software fault. The display buffer contains the PA + 1 (address) of the "From" address of the last data transfer. Note the address.

2.13 Bit 1 of the System Status (SYS STAT) register is the "Block Hardware Check" (BHC) bit. If this bit is 0, The Error Register (ERR) will indicate whether or not the CU stopped due to an error check circuit fault.

2.14 If the BHC = 1 or the ERR = 0, the current PA and the "From" PA (noted above) should be looked up in the program listings. The program listings will have to be studied to determine the function being performed when the CU stopped.

D. References

2.15 The documents listed in the Reference Documents Table (Table D) may be useful during the loading of the generic programs.

TABLE D

GENERIC LOADING VERIFICATION REFERENCE DOCUMENTS

DOCUMENT	SUBJECT
IM-2H200-04	Input Message Manual, No. 2B Electronic Switching System
OM-2H200-04	Output Message Manual, No. 2B Electronic Switching System
IM-3H300-01	Input Message Manual, No. 3 Electronic Switching System
OM-3H300-01	Output Message Manual, No. 3 Electronic Switching System
IM-4C001-01	Input Message Manual (EOS) for the Extended Operating System
OM-4C001-01	Output Message Manual (EOS) for the Extended Operating System
TLM-1C900-01	Common Systems Processor Trouble Locating Manual
TLM-4C706-01	Tape Data Cartridge TLM (CTAPM)
232-xxx-xxx	No. 2B Electronic Switching System
233-xxx-xxx	No. 3 Electronic Switching System
254-xxx-xxx	3A Processor Extended Operating System
254-340-086	Initialization and Recovery—3A Processor, Extended Operating System

TABLE E

GENERIC LOADING VERIFICATION PROCEDURES—EOS

STEP	PROCEDURE	RESPONSE	REMARKS
	Note: All wiring operations and x-ray tests must have been completed.		
1	Verify the following:		
	(1) On both 3A CC Control Panels that the		
	POWER key/lamp is lit.	On (green)	
	MANUAL key/lamp is lit.	On (white)	
	TEST MODE lamp is lit.	On (red)	TEST MODE is controlled by TMR key on the rear of the 3A CC Control Panel.
	(2) On both TDCs that the		
	TDC POWER lamp is lit.	On	
	(3) On the SSP that the		
	CKT POWER lamp/key is lit.	On (green)	
	LAMP POWER key is lit.	On (green)	
2	Remove tape cartridges from TDCs and insert Generic Program cartridges in both TDCs.		Issues of generic program cartridges must be the same.
3	After initialization is complete, follow procedures in paragraph 1.13, "Data Cartridge Insertion and Removal" when removing and inserting data cartridges.		Correct procedures must be followed when inserting or removing data cartridges.

TABLE E (Contd)

GENERIC LOADING VERIFICATION PROCEDURES—EOS

STEP	PROCEDURE	RESPONSE	REMARKS
4	Generic Program loading: If x-ray programs presently reside in Main Store, do the following: (1) On the active 3A CC Control Panel the LOAD AND DISPLAY lamps are active (flicker). (2) Observe TTY printout. (3) On the SSP depress: (a) SELECT 0 or SELECT 1 (for active CU) key (b) FORCE key (4) On the SSP depress: ENABLE key MEMORY RELOAD key INIT EXECUTE key (5) If VSS application, depress the MEMORY RELOAD TDC key in place of MEMORY RELOAD in procedure 2. (6) Observe tape movement in the tape cartridge. (7) Observe that the maintenance TTY bell will sound for about 3 minutes.	 A prompt (#) symbol is printed. On 9 (red) On (red) On (red) On (red) On (red)	 Selects CU to be active. System is bootstrapping and reading generic program into Main Store.

TABLE E (Contd)

GENERIC LOADING VERIFICATION PROCEDURES—EOS

STEP	PROCEDURE	RESPONSE	REMARKS
	(8) Observe display buffer LEDS (bottom row) on SSP.		Displays "bouncing ball" effect.
	(9) LOAD AND DISPLAY lamps on forced-active 3A CC Control Panel are active.	Flickering	Dynamic display of PA + 1 (address) of last data transferred.
	(10) Observe active and standby 3A CC Control Unit STATUS lamps.		
	ACTIVE lamp is on for active 3A CC Control Unit.	On (green)	
	NOT ACTIVE lamp is on for the standby 3A CC Control Unit.	On (white)	
	(11) A group of TTY printouts are generated. Refer to OM-4C0001-01 and to the applications Output Message (OM) Manual for the details of the printouts.		
5	If Procedures 1 through 10 are successful, perform the following:		
	(1) On both 3A CC Control Panels:		
	Release TMR key.	Off	
	Release MANUAL key.	Off	
	(2) On the SSP:		
	Release SELECT (0 or 1) key for the active CU.	Off	
	(3) After about 2 minutes, 2 TTY messages are printed.	tt UPD OMAS COMPL	Loading complete.
		tt REPT CU STAT AVL	Active CU available.

TABLE E (Contd)

GENERIC LOADING VERIFICATION PROCEDURES—EOS

STEP	PROCEDURE	RESPONSE	REMARKS
6	If procedures 1 through 12 are not successful, repeat the procedures using the standby (other) CU. If neither CU can be loaded successfully, the troubleshooting aids may be useful. Troubleshoot the CU that progressed the furthest in initialization.		
7	If x-ray programs do not reside in Main Store perform the following:		
	(1) On both the 3A CC Control Panels:		
	Depress RESET CIRCUITS key		
	MODE—HALT lamp lit	On (white)	On both panels.
	(2) On the SSP:		
	Depress SELECT 0 key	On (red)	Selects CU 0 to be active.
	Depress FORCE key	On (red)	CU 0 forced active.
	(3) On active 3A CC Control Panel:		
	Clear word HEX 20 on Main Store.		
	If unable to clear, power down and then restore.		Write protect was enabled. Clear write protect.
	(4) On CU 0 place TMR switch down and when tape moves, put TMR switch up.		

TABLE E (Contd)

GENERIC LOADING VERIFICATION PROCEDURES—EOS

STEP	PROCEDURE	RESPONSE	REMARKS
	In Procedures 1 through 4		TTY bell will sound for 3 minutes and "bouncing ball" effect will be observed on SSP LEDs.
8	If initialization was successful, perform the following:		
	(1) On both 3A CC Control Panels:		
	Release TMR key	Off	
	Release MANUAL key	Off	
	On the SSP:		
	(2) Release SELECT 0 key	Off	
	(3) After about 2 minutes, 2 TTY messages are printed	tt UPD OMAS COMPL	Loading complete
		tt REPT CU STAT AVL	CU 0 available
9	If Procedures 1 through 7 are not successful, repeat the procedures using CU1.		
10	If neither CU can be loaded successfully, the troubleshooting aids may be useful. Troubleshoot the CU that progressed the furthest in the initialization.		

E. System Initialization

2.16 These procedures contain references to system initialization in a typical application and serve only as an example. For specifics, refer to the handbook issued with each specific application. Also refer to Input/Output Message Manual IM/OM-4C001-01.

F. Manual Initialization Procedures

2.17 Initialization levels may be generated automatically by the system application software or may be generated manually. Depressing ENABLE and INIT EXECUTE keys causes a MRF in both control units (CUs). Various levels of initializations may occur depending on which key is operated prior to the INIT EXECUTE key operation. A postmortem dump of register contents (see Table F) may be used to determine the cause of the initialization.

Automatic System Application Software Initialization (Bootstrap)

2.18 System initialization may occur to recover system integrity automatically in various levels. The first initialization indication is an output message on the TTY. A typical message is shown in Table G.

2.19 When the 3A Processor bootstraps itself, the appropriate light on the SSP will be lighted for the type of bootstrap. A BACKDT is for a backdate bootstrap and a MEMORY RELOAD is for a complete memory reload. If no light is lighted while the bootstrap is in process, then the bootstrap is a CHECKSUM bootstrap. These lights will remain on after the system comes up.

Manually Generated Initialization

2.20 Load both tape cartridges.

2.21 At the SSP, follow the procedures in Table H for the Extended Operating System (EOS). For the No. 2B ESS and No. 3 ESS initializations, typical procedures are provided in Tables I and J, respectively. Table K identifies initialization levels for the Electronic Translation System (ETS). Table L provides a list of reference documents relating to the 2B ESS, 3B ESS, EOS, Tape DATA Controller, System Status Panel, etc.

Setting Software Clock

2.22 Set and check the software clock by following the procedures in Table M.

G. Postmortem Output Message

2.23 When trouble occurs that is serious enough to require clearing of memory and/or registers and restoring the 3A Processor to a known good state, an initialization action automatically takes place. Generally, the degree of the initialization becomes more drastic each time an initialization attempt fails. The degree of severity is identified by the initialization level number. The higher the number, the more severe is the action taken to restore the processor state. A postmortem dump is used to determine the cause of a system initialization. The dump is printed out on the terminal (TTY) either automatically, when the system leaves the initialization state, or in response to the input message OP:POSTMORT!. The dump consists of two 32-word groups. Each group is formatted on a 4-by-8 array (four lines by eight columns of data). These two groups of data words represent the processor states during the last series of initializations.

2.24 The details of the format of the 32 data word groups is shown in Table F. The format of the postmortem message and printout is generally:

```
tt OP POSTMORT aaaaa

    8 data words
    8 data words
    8 data words
    8 data words

OP POSTMORT bbbbb

    8 data words
    8 data words
    8 data words
    8 data words

OP POSTMORT COMPL
```

Where:

tt is the minutes past the hour.

aaaaa is the address where the first group of 32 data words is stored.

bbbbb is the address where the second group of 32 data words is stored.

data word is a 4-digit hexadecimal number.

A typical postmortem message group is shown below.

```
33 OP POSTMORT 014C7
   8302 0008 040A 048A 9400 0000 085A 7BBC
   0000 4841 0021 2174 0000 DFF7 0000 07BB
   0000 D7ED 0001 83BB 10F0 0000 0002 120A
   0000 0000 0000 0000 0000 0000 0000 0000

33 OP POSTMORT 014E7
   7D01 0011 0004 0011 1590 9200 0000 67EC
   0040 1D90 4C31 0000 0000 DD01 0000 67DE
   0000 67EA 3A20 5262 1070 0000 0002 120E
   3A20 8000 0000 56E2 0000 0000 0000 0128

   OP POSTMORT COMPL
```

2.25 If the CU ***was*** in the INITIALIZATION state:

The first four lines of data words (32 words) represent the state of the system when the last initialization occurred. The second four lines of data words (32 words) represent the state of the system when the first initialization occurred.

2.26 If the CU ***was not*** in the INITIALIZATION state:

The first four lines of data should agree with the second four lines of data and represent the state of the CU in which the error occurred at the time of initialization.

2.27 Refer to the Output Message Manual OM-4C001-01 for details of the printouts of the postmortem dump and output messages.

H. References

2.28 The references listed in Table G will be useful during system initialization.

TABLE F

POSTMORTEM 32-WORD GROUP FORMAT

	COLUMN							
LINE	1	2	3	4	5	6	7	8
1	(Note 1)	Task	SYSTATE (Note 2)	Init. Data (Note 3)	TI (Note 4)	IS Reg.	PA Reg. (bits 19-16)	PA Reg. (bits 15-0)
2	R8	R9 (Note 5)	R10 (Note 5)	R11	Spare	IM Reg.	DB Reg. (bits 19-16)	DB Reg. (bits 15-0)
3	R13	R13	R14	R15	HG Reg.	(Note 9)	SS Reg. (bits 19-16)	SS Reg. (bits 15-0)
4	HG(0)	HG(1)	HG(0)+16	HG(1)+16	(Note 6)	(Note 7)	(bits 19-16) (Note 8)	(bits 15-0) (Note 8)

Legend

DB - Display Buffer Register
ER - Error Register
HG - Hold-Get Register
IM - Interrupt Mask Register
IS - Interrupt Set Register
PA - Program Address Register
R8-R15 - General Registers
SS - System Status Register
TI - Timing Counter

Refer to Notes 1 through 9 on the following pages.

Note 1:

Data are divided into fields as follows:

BIT NO.	MEANING
2-0	Initialization Level

LEVEL	TYPE of INITIALIZATION
1	Normal
2	Partial clear
3	Partial clear
4	Emergency audit
5	Emergency audit
6	Transient, stable, recent change, stable and recent change, memory reload, or backdate office data

3	Flat - If bit equals 1, initialization level reached its maximum value and was recycled before the system left the initialization state.
9-4	Seconds past the minute
15-10	Minutes past the hour.

Note 2:

System state detector (SYSTATE) buffer data. A one (1) in a bit position has the following meaning.

BIT NO.	MEANING
0	Off-line 3A CC is in standby
1	Off-line 3A CC is out of service
2	Off-line 3A CC is unavailable
3	Initialization timing interval is in progress
4	Off-line 3A CC is out of service due to a fault
5	Off-line 3A CC has been manually removed from service
6	Off-line 3A CC memory is being updated by the system
7	Off-line 3A CC is being used by a program
8	Off-line 3A CC is in the manual mode
9	Indicates which 3A CC is on-line (active) 0 — 3A CC No. 0 is active (on-line) 1 — 3A CC No. 1 is active
10	Off-line main store is out of service (OOS)
11	System Status Panel (SSP) is out of service
12	Maintenance channel is out of service
13	A 3A CC restoral is in progress
14	System Status Panel memory reload request
15	System Status Panel initialization request.

Note 3:

Initialization (Init) Data is as follows:

BIT NO.	MEANING
0	If 1, a control unit switch did not occur
1	If 1, an initialization was caused by a maintenance channel (MCH) message
2, 3	If 01, a first timeout caused the initialization If 11, a second timeout caused the initialization
4	The 3A CC was forced on-line or locked
5	If 1, memory reloading from tape caused initialization
6	IF 1, main store is out-of-date
7	If 1, the other main store is not accessible
8	Indicates which 3A CC is initializing 0 — 3A CC No. 0 is initializing 1 — 3A CC No. 1 is initializing
9	If 1, maintenance channel failed while the off-line registers were being retrieved for the postmortem dump
10-13	Unassigned
14	If 1, System Status Panel memory reload requested
15	If 1, System Status Panel initialization requested.

Note 4:

A 1 in a bit position has the following meaning:

BIT NO.	MEANING
14	This is the first timeout
15	This is the second timeout.

Note 5:

If a 3A CC (CU) switch did not occur, data are meaningless.

Note 6:

A kernel fault type occurred BEFORE the kernel audit. If 0, no kernel fault was detected in the auxiliary 3A Processor only. For No. 2B ESS and No. 3 ESS the data word is HG(0)+32.

Note 7: (Not available)

Note 8:

A 1 in a bit position has the following meaning:

BIT NO.	MEANING
0	TO decoder error
1	FROM decoder error
2	IB X and Y field parity error
3	Bus parity error
4	Data manipulation logic (DML) match error
5	Parity error (MAR)
6	Clock error
7	My store error A
8	Mismatch (MAR-RAR)
9	Function register parity error
10	My store read parity error
11	My store write protect error
12	My store fast timeout
13	Branch allowed error
14	Other store error B
15	Other store error A
16	Other store fast timeout
17	Input/Output multiple channel select
18	Program Timer (PT) reset received by on-line 3A CC
19	Switch received by on-line 3A CC.

Note 9:

For No. 2B ESS, Store Address Register contents in case of a control unit (CU) switch.

TABLE G

AUTOMATIC SYSTEM INITIALIZATION OUTPUT MESSAGES

RECOVERY TTY OUTPUT MESSAGE		
11 = Initialization level number		
ss = SYSTATE contents as follows:		
bit	0	Off-line CU standby
bit	1	Off-line CU out of service
bit	2	Off-line CU locked
bit	3	In initialization interval
bit	4	Off-line CU removed automatically
bit	5	Off-line CU removed manually
bit	6	Off-line CU memory being updated
bit	7	Off-line CU used by program
bit	8	Off-line CU panel in manual
bit	9	= 0 = CU0 on-line
bit	9	= 1 = CU1 on-line
bit	10	Off-line main store out of service
bit	11	SSP is out of service
bit	12	Maintenance channel out of service
bit	13	Restore CU in progress
bit	14	Unconditional switch in progress
bit	15	Off-line CC power key operated
ii = Initialization data as follows:		
bit	0	= 1 = No switch occurred
bit	1	MCH message caused initialization
bits	2,3	= 01 = First timeout
bits	2,3	= 11 = Second timeout
bit	4	CU forced or locked on-line
bit	5	= 1 = Initialization by reload memory
bit	6	Main store out of date
bit	7	No access to other main store exists
bit	8	= 0 = CU0 is initializing
bit	8	= 1 = CU1 is initializing
bit	9	= 1 = Main channel failed while off-line registers retrieved for postmortem
bit	14	SSP memory reload request
bit	15	SSP initialization request

TABLE H

MANUALLY GENERATED INITIALIZATION — EOS

STEP	PROCEDURE	RESPONSE	REMARKS
1	Depress ENABLE key	ENABLE lamp lights	
2	Depress one, none, or all of the following keys:		Controls initialization level.
			If key depressed accidentally, release key by depressing it again before depressing INIT EXECUTE key.
	STABLE CALLS key		LEVEL 5 initialization.
	MEMORY RELOAD key		BOOTSTRAP with translation file.
	BACKDT OFFICE DATA key		BOOTSTRAP with backdate file.
3	Depress INIT EXECUTE key	ENABLE lamp extinguishes	BOOTSTRAP initialization complete.
4	Type:		Check time of day.
	OP:CLK!	hh mi ss	Hour, minute, second.
			Reset clock if necessary*.
5	System in NORMAL state	SYSTEM NORMAL lamp is lighted.	
	For LEVEL 3 initialization:		LEVELS 3 and 4 — all tasks are restarted and all messages are preserved. EOS system memory is not reconstructed.
	Depress ENABLE key		
	Depress INIT EXECUTE key		

* Refer to Table L

TABLE H (Contd)

MANUALLY GENERATED INITIALIZATION — EOS

STEP	PROCEDURE	RESPONSE	REMARKS
	For CHECKSUM Bootstrap:		
	Depress ENABLE key		
	Depress INIT EXECUTE key		
	Repeat CHECKSUM steps three (3) times in succession.		
6	For LEVEL 5 initialization:		LEVELS 5 and 6 initialization.
	Depress ENABLE key		
7	Depress ENABLE key		
	Depress one, none, or all of the following keys:		Controls initialization level.
			If key depressed accidentally, release key by depressing it again before depressing INIT EXECUTE key.
	STABLE CALLS key		LEVEL 5 initialization.
	MEMORY RELOAD key		BOOTSTRAP with translation file.
	BACKDT OFFICE DATA key		BOOTSTRAP with backdate file.

TABLE I

NO. 2B ESS INITIALIZATIONS

INITIALIZATION		INITIATED	
LEVEL	NAME	AUTOMATIC	MANUAL
1	Nominal (no memory)	Yes	No
2	Partial clear	Yes	No
3	Partial clear	Yes	No
4	Emergency audit	Yes	No
5	Emergency audit	Yes	ENAB, INIT EXEC
6	Transient clear	Yes	ENAB, INIT EXEC, ENAB, INIT EXEC
6	Stable calls	No	ENAB, STAB CALLS, INIT EXEC
6	Recent change	No	ENAB, REC CHG, INIT EXEC
6	Stable calls and recent change	No	ENAB, STAB CALLS, REC CHG, INIT EXEC
6	Memory reload	No	ENAB, MEM RELOD, INIT EXEC
6	Backdate office data	No	ENAB, MEM RELOD, BACKDT OFFICE DATA, INIT EXEC

TABLE J

NO. 3 ESS INITIALIZATIONS

INITIALIZATION		INITIATED	
LEVEL	NAME	AUTOMATIC	MANUAL
1	Partial clear	Yes	No
2	Partial clear	Yes	No
3	Partial clear	Yes	No
4	Transient clear	Yes	ENABLE, INIT EXEC
5	Stable clear	Yes	ENABLE, STABLE CALLS INIT EXEC or INIT EXEC, MEMORY RELOAD, ENABLE

TABLE K

ETS INITIALIZATIONS

LEVEL	NAME
1	Partial Task
2	AMA Billing
3	Checksums reload
4	Complete memory reload
5	Memory reload (no recent change)

TABLE L

SYSTEM INITIALIZATION
REFERENCE DOCUMENTS

DOCUMENT	SUBJECT
IM-2H200-04	Input Message Manual, No. 2B Electronic Switching System (ESS)
OM-2H200-04	Output Message Manual, No. 2B Electronic Switching System (ESS)
IM-3H300-01	Input Message Manual, No. 3 Electronic Switching System (ESS)
OM-3H300-01	Output Message Manual, No. 3 Electronic Switching System (ESS)
IM-4C001-01	Input Message Manual (EOS) for the Extended Operating System
OM-4C001-01	Output Message Manual (EOS) for the Extended Operating System
TLM-1C900-01	Common Systems Processor Trouble Locating Manual
TLM-4C706-01	Tape Data Cartridge TLM (CTAPM)
232-100-100	No. 2B Electronic Switching System (ESS) General Description
233-000-003	No. 3 Electronic Switching System (ESS) General Description
254-340-001	3A Processor Extended Operating System General Description
254-300-170	Tape Data Controller, Description and Theory - Common Systems
254-300-180	System Status Panel, SSP Controller, and SSP Panel Relay Unit, Description and Theory of Operation - Common Systems
254-300-190	Teletypewriter and Teletypewriter Controller, Description and Theory of Operation
254-340-086	Initialization and Recovery - 3A Processor Extended Operating System

TABLE M

SETTING SOFTWARE CLOCK — ALL SYSTEMS

STEP	PROCEDURE	RESPONSE	REMARKS
	This procedure applies to ALL system applications.		
1	To set time of day type:		Sets hours, minutes, and seconds (hh, mi, and ss).
	SET:CLK:TIME(hh,mi,ss)!		hh = 0 - 23 hours mi = 0 - 59 minutes ss = 0 - 59 seconds
2	To set date and time of day type:		Sets month, day, and year (mo, dd, yr).
	SET:CLK:TIME(hh,mi,ss), DATE(mo,dd,yr)!		mo = 1 - 12 dd = 1 - 31 yr = 0 - 99
3	To interrogate clock type:		Request time of day, date.
	OP:CLK!	tt OP CLK mo/dd/yr hh:mi:ss XXX	Current time date.

I. Memory Reload

2.29 Memory reload verification verifies that each control unit (CU) is capable of reloading memory (bootstrapping) from the tape cartridge in the associated Tape Data Controller (TDC) on the Maintenance Frame.

Caution: The system must not be on-line when these memory reload procedures are performed.

2.30 The system initialization keys located on the System Status Panel (SSP) are used to cause the bootstrap to occur.

J. Memory Reload Verification

2.31 The procedures listed in Table N must be followed to verify a memory reload.

K. Troubleshooting Aids

2.32 If memory reload was not verified (by Table N procedures) it is assumed that the CU stopped due to some fault that could be a hardware or a software fault.

2.33 The display buffer (DB) LEDs contain the PA + 1 of the FROM address of the last data transfer. **NOTE THE ADDRESS.** Bit 1 of the System Status (STS STAT) register is the Block Hardware Check (BHC) bit. If the BHC bit is 0, the Error Register (ERR) will indicate whether or not the CU stopped due to an error check circuit fault.

2.34 If the BHC bit is 1 or the ERR is 0, the current PA and the FROM PA previously noted should be looked up in the program listings. The comments in the listings must be studied to determine what the program was attempting to do when the fault occurred and the program stopped.

2.35 The references listed in Table 0 may be useful during a verification of the memory reload.

TABLE N

MEMORY RELOAD VERIFICATION PROCEDURES

STEP	PROCEDURE	RESPONSE	REMARKS
1	Verify that the system is in the active mode:		***Caution:*** The system must not be on-line when the memory reload is performed.
	Observe the SSP:		
	SYNC 0 - ACTIVE LED	On (green)	CU 0 is active
	SYNC 1 - STANDBY LED	On (green)	CU 1 in standby
	SYSTEM NORMAL lamp	On (green)	System in normal mode
	Observe the 3A CC Control Panel:		
	STATUS - TEST MODE lamp	Extinguished	
	STATUS - MANUAL key/lamp	Extinguished	
2	Verify that TDC 0 and TDC 1 are available for service		One TDC active and one in standby
3	Verify that both TDCs are loaded with correct generic cartridge		Must have same issue in both TDCs
4	Verify that Maintenance TTY is in service		TTY must be available.
5	On the SSP System Emergency Manual Control:		
	Depress SELECT 0 key	On (red)	
	Depress FORCE key	On (red)	CU 0 forced on-line
	Observe TTY:	tt REPT CU STAT UAL	

TABLE N (Contd)

MEMORY RELOAD VERIFICATION PROCEDURES

STEP	PROCEDURE	RESPONSE	REMARKS
6	If not a VSS application, perform the following IN THE ORDER listed:		
	On the SSP System Initialization:		
	(1) Depress ENABLE key	On (red)	
	(2) Depress MEMORY RELOAD key	On (red)	
	(3) Depress INIT EXECUTE key	On (red)	
	If VSS application:		
	(1) Depress ENABLE key	On (red)	
	(2) Depress MEMORY RELOAD TDC key	On (red)	
	(3) Depress INIT EXECUTE key	On (red)	
	Observe tape movement in the tape cartridge		
7	System bootstrapping for about 3 minutes; the following should be observed:		
	Maintenance TTY bell will sound for about 3 minutes		System is bootstrapping and reading generic into Main Store
	Observe display buffer LEDs (bottom row) on SSP and LOAD AND DISPLAY LEDs on active 3A CC Control Panel	Displays "bouncing ball" effect simultaneously	
	Observe LOAD AND DISPLAY lamps on 3A CC Control Panel	Flicker continuously	Dynamic display of PA + 1 (address) of last data transferred

TABLE N (Contd)

MEMORY RELOAD VERIFICATION PROCEDURES

STEP	PROCEDURE	RESPONSE	REMARKS
8	Observe active and standby 3A CC Control Panel STATUS lamps:		
	ACTIVE lamp on active 3A CC	On (green)	
	NOT ACTIVE lamp on standby 3A CC	On (white)	
9	A group of TTY printouts are generated. Refer to OM 4C001-01 and to application Output Message (OM) for details of the printouts.		

TABLE O

MEMORY RELOAD VERIFICATION REFERENCE DOCUMENTS

DOCUMENT	TITLE
IM-4C001-01	Input Message Manual (EOS) for the Extended Operating System
OM-4C001-01	Output Message Manual (EOS) for the Extended Operating System
TLM-1C900-01	Common Systems Processor Trouble Locating Manual
TLM-4C706-01	Tape Data Cartridge Trouble Locating Manual (CTAPM)

L. Overwrite

2.36 This section provides overwrite procedures for applying patches to generic programs for the EOS 3A Processor.

2.37 Each program problem is identical and corrected via a Broadcast Warning TWX (BWT). The PECC issues BWTs using the Teledat system as a formal software Change Notice (CN). A copy also is sent over the AT&T ADNET system to the Technical Assistance Centers (TAC) or Switching Control Centers (SCC).

2.38 To verify error-free transmissions from the PECC to the region and to the job site, a checksum scheme is used.

2.39 The overwrite programs provide a mechanism for verifying that the overwritten data generated by the application is accurately entered into the 3A Processor at the application location. The accuracy is checked by generating a check number "c" to verify that each line of overwrite data is entered correctly, and a check number to verify that all data has been entered. The overwrite programs have the mechanism for the applications to generate the check numbers on the 3A Processor at the application location.

2.40 All overwrites apply to the latest generic program currently installed in the office and may be applied by a craft person or an installer.

M. Setup Procedure

2.41 The system must be able to run in normal mode. (One CU active, other CU standby as indicated as SSP).

2.42 Both TDCs and the maintenance TTY must be in service.

2.43 All input and output messages should be handled by the maintenance TTY only.

2.44 Duplicate data cartridges should be available and up-to-date.

N. Overwrite Procedure

2.45 Perform the overwrite procedures as indicated in Table P.

Note: Great care must be exercised to verify that correct data is input.

TABLE P

OVERWRITE PROCEDURE — EOS

STEP	PROCEDURE	RESPONSE	REMARKS
1	RST:DEVICE:TDC 0!	IP tt DEVICE REPT TDC 0 STATE AVL x1 x2 x3 x4 (or) OK	Place TDC 0 in service
2	RST:DEVICE:TDC 1!	IP STATE AVL x1 x2 x3 x4 (or) OK	Place TDC 1 in service
3	ALW:TAPEUTIL!	PF tt ALW TAPEUTIL COMPL	Activate tape utilities
4	EX:TDC!	PF tt TAPEUTIL COMPL	Retensions tapes
5	INH:TAPEUTIL!	PF tt TAPEUTIL INH	Inhibit tape utilities
6	DGN:TDC 0!	IP tt DGN:TDC 0 ATP	TDC 0 tested successfully
7	DGN:TDC 1!	IP tt DGN:TDC 1 ATP	TDC 1 tested successfully If the overwrite is to be applied to a new tape, use the procedure in Table W first, then continue at Step 8. The overwrite file must have been initialized with the following message: INIT:OWFILE.
8	ALW:OW!	PF tt ALW OW COMPL	Request activation of overwrite program.
9	IN:GENID:xxxxxxxx!	OK	xxxxxxxx is the generic identification number from BWT.
10	IN:ISSID:zzzzzzzz!	OK	zzzzzzzz is the generic program issue number from BWT.

TABLE P (Contd)

OVERWRITE PROCEDURE — EOS

STEP	PROCEDURE	RESPONSE	REMARKS
11	IN:OW n; TTY!	PF	Overwrite "n" is about to be entered.
			The overwrite request results in a search of the tape for the specified OW number "n".
		IN OW COMPL	Tape contains correct generic and issue but does not contain overwrite (OW) "n".
		IN OW INH	If the specified OW is already on the tape or if either the GENID or the ISSID (entered previously) is different from those on the tape, an IN OW INH error message is returned. Correct the error before proceeding. Most likely the error cause was: (a) GENID or ISSID incorrect or not entered. (b) OW "n" already on the tape. (c) OW number not specified or incorrect.
12	IN:OWDATA:c,s,add,old,new!	OK	The location at absolute address "add" in segment "s" is being changed from "old" to "new". The OK response indicates that the "add" is an equipped address and the check number "n" calculated over the "s", "add", "old", and "new" fields is equal to "c". If it were not, an "NG" response would be returned. The "OK" response indicates that the data is entered into the overwrite buffer.
	〃	〃	
	〃	〃	
	(Repeat for each word.)	〃	
	〃	〃	
		〃	
	IN:OWDATA:c,s,add,old,new!		

TABLE P (Contd)

OVERWRITE PROCEDURE — EOS

STEP	PROCEDURE	RESPONSE	REMARKS
13	VFY:OWDATA:c!	OK	This request verifies that all of the IN:OWDATA input messages associated with this patch have been entered. The "c" is the check number. An "NG" response indicates that an IN:OWDATA statement is missing. Without an "OK" response from this message, the overwrite cannot be written out to the tape or loaded into memory.
14	VFY:OW:OLD!	PF	Retrieve the current contents of the locations identified in the buffer and compare it to the old data entered via the IN:OWDATA messages.
		VFY OW COMPL	All the data is compared. If a mismatch is detected, a VFY OW ERR message is returned to identify the error followed by the VFY OW INH response.
15	OP:OW:TAPE!	PF	Appends the overwrite in the buffer to the end of the overwrite file on the tape. The overwrite status at this point is inactive. Consequently, if a system initialization results in a program reload at this point, this overwrite will not be used.
		OP OW COMPL	The tape overwrite was successful. An overwrite failure response will be OP OW INH. An overwrite failure response will be returned if the check number mismatches.
16	IN:OW n; TAPE!	PF	This step is functionally superfluous, but is included so that the data tested is actually the data on the tape. The overwrite buffer is loaded with the contents of the overwrite file "n" off the cartridge tape.

TABLE P (Contd)

OVERWRITE PROCEDURE — EOS

STEP	PROCEDURE	RESPONSE	REMARKS
		IN OW COMPL	The tape read was successful. The failure response is IN OW INH.
17	Operate LOCK key on SSP.		This prevents a control unit switch while the off-line store is being loaded. A switch would almost certainly be "fatal" because the store, containing half an overwrite, would be inconsistent.
18	LOD:OW:NEW!	PF	Request that the new data be used to overwrite the off-line store (resident) or the off-line tape (nonresident).
		LOD OW COMPL	The overwrite was successful. A failure response is LOD OW INH. A failure can be caused by tape operation problems or check number mismatch.
19	Release LOCK key on SSP.		
20	VFY:OW:NEW!	PF	Verify that the new contents of store matches the new data in the overwrite buffer.
		VFY OW COMPL	The overwrite was successful.
21	SW:CU!	OK	Switch to the control unit with the overwritten data.
	(Test data)		The test should exercise the overwritten data. If the test fails, a switch to the original control unit should be requested and the following LOW OW message should be qualified with "OLD" instead of "NEW" to remove the overwrite.

TABLE P (Contd)

OVERWRITE PROCEDURE — EOS

STEP	PROCEDURE	RESPONSE	REMARKS
22	Depress LOCK key on SSP.		
	LOD:OW:NEW!	PF	Overwrite the second store or cartridge tape unit.
		LOD OW COMPL	The overwrite operation was successful.
23	Release LOCK key on SSP.		The new data is now active in the system, but a program reload initialization will still result in its elimination from store. The data still exists on the cartridge tape in the inactive state.
	ACT OW n!	PF	Mark the overwrite active in the overwrite file so that subsequent program reload initializations will include this overwrite.
		ACT OW COMPL	Activation was successful. The failure response is ACT OW INH.
	UPD:OW!	PF	Update the CHECKSUM file on tape to reflect the overwrite "n".
		UPD OW COMPL	The update was successful. The failure response is UPD OW INH.
	INH:OW!	OK	Deactivate the overwrite program.

O. Overwrite File Administration

2.46 Overwrite file status may be requested and printed out on the TTY. Overwrites may be listed as activated, deactivated, or removed.

2.47 Table Q provides a procedure for determining overwrite status.

2.48 Table R provides a procedure for activating an overwrite.

2.49 Table S provides a procedure for deactivating an overwrite.

2.50 Table T provides a procedure for removing a deactivated overwrite.

2.51 Table U provides a procedure for listing the data associated with an existing overwrite.

2.52 Table V provides a procedure for putting a generic and issue header on a new tape.

2.53 Table W provides a procedure for putting a new GENID and ISSID on the tape header.

2.54 Table X provides a procedure for loading the old or new data associated with an overwrite from tape and Table Y describes the generation of overwrite check numbers.

TABLE Q

DETERMINING OVERWRITE STATUS

STEP	PROCEDURE	RESPONSE	REMARKS
1	Perform steps 1-7 of Table V.		Not necessary if performed earlier in overwrite.
2	ALW:OW!	PF	Request activation of overwrite program. Craft person need not perform this step if overwrite is already active.
		ALW OW COMPL	Overwrite program is activated.
3	OP:OWFILE!	PF tt OP OWFILE	
		GENID xxxxxxxx ISSID zzzzzzzz OW 0000 s mmdd yyhh nnss	xxxxxxxx = Generic ID zzzzzzzz = Issue ID 0000 = Overwrite number s = Overwrite status (0 = inactive, 1 = active, 3 = dead, 4 = active — entered without check numbers. mmdd = month and date overwrite entered yyhh = year and hour overwrite entered nnss = minute and second overwrite entered
		tt OP OWFILE COMPL	Overwrite completed.
4	INH:OW!	PF tt ALW OW INH	Deactivates (inhibits) the overwrite program. Overwrite program inhibited.

TABLE R

ACTIVATE AN OVERWRITE

STEP	PROCEDURE	RESPONSE	REMARKS
1*	Perform steps 1-7 of Table V.		
2†	ALW:OW!	PF tt ALW OW COMPL	Request activation of overwrite program.
3	ACT:OW n! (n= overwrite number)	PF tt ACT OW COMPL	Activates overwrite "n". If an ACT OW INH message is generated, check to see if the overwrite is already active or not on tape. Use procedures in Tables P or U.
4	UPD:OW!	PF tt UPD OW COMPL	Updates checksum file on tapes.
5	INH:OW!	PF tt ALW OW INH	Deactivates overwrite program.

* Step 1 is not necessary if it was performed earlier in the overwrite procedure.

† Step 2 need not be performed if the overwrite program is already active.

TABLE S

DEACTIVATE AN OVERWRITE

STEP	PROCEDURE	RESPONSE	REMARKS
1*	Perform steps 1-7 of Table V.		
2†	ALW:OW!	PF tt ALW OW COMPL	Requests activation of overwrite program.
3	CNL:OW n! (n= overwrite number)	PF tt CNL OW COMPL	Changes status to inactive. If a CNL OW INH output message is generated, the overwrite number is not on the tape or may already be deactivated or dead. Use procedures in Tables P or U to check.
4	UPD:OW!	PF tt UPD OW COMPL	Updates checksum file on tapes.
5	INH:OW!	PF tt ALW OW INH	Deactivates overwrite program.

* Step 1 is not necessary if it was performed earlier in the overwrite procedure.

† Step 2 need not be performed if the overwrite program is already active.

TABLE T

REMOVE A DEACTIVATED OVERWRITE

STEP	PROCEDURE	RESPONSE	REMARKS
1*	Perform steps 1-7 of Table V.		
2†	ALW:OW!	PF tt ALW OW COMPL	Requests activation of overwrite program.
3	RMV:OW n! (n= overwrite number)	PF tt RMV OW COMPL	Removes overwrite "n". If a RMV OW INH message is generated, the overwrite number is not on tape or is already deactivated. Use procedures in Table P or U to check. An NG or RL response may indicate that the OW has not been canceled. Use procedures in Table S to cancel it.
4	UPD:OW!	PF tt UPD OW COMPL	Updates checksum file on tapes.
5	INH:OW!	PF tt ALW OW INH	Deactivates overwrite program.

* Step 1 is not necessary if it was performed earlier in the overwrite procedure.

† Step 2 need not be performed if the overwrite program is already active.

TABLE U

LIST OVERWRITE DATA

STEP	PROCEDURE	RESPONSE	REMARKS
1*	Perform steps 1-7 of Table V		
2†	ALW:OW!	PF	Requests activation of overwrite program
		tt ALW OW COMPL	
3	IN:OW n;TAPE!	PF	"n" = overwrite number. Overwrite data is moved from tape to overwrite buffer.
	(or)		
	IN:OW n;TTY[,NOCHECK]!	PF	Initiates loading the overwrite buffer via IN:OWDATA TTY input messages. Overwrites are entered from the buffer via OP:OW, VFY:OW, and LOD:OW input TTY messages. If keyword NOCHECK is present, IN:OW message then checks involving check numbers in IN:OWDATA and VFY:OWDATA are ignored.
		tt IN OW COMPL	Copies overwrite data into the overwrite buffer. If response is INH rather than COMPL, data was not copied into buffer. If response is RL, another program is executing. Repeat later. If response is NG the TTY of TAPE keyword was not entered or the message was out of sequence.

* Step 1 is not necessary if it was performed earlier in the overwrite procedure.

† Step 2 need not be performed if the overwrite program is already active.

TABLE U (Contd)

LIST OVERWRITE DATA

STEP	PROCEDURE	RESPONSE	REMARKS
4	OP:OW;TAPE!	PF	Copies overwrite buffer contents onto the tape
	(or)		
	OP:OW;TTY!	PF	Formats and prints overwrite buffer contents on the TTY
		ttIN OW n	Outputs overwrite "n" to tape or to TTY
		IN OWDATA cc ss aa oo nn	Overwrites "n" data cc = Check number of line ss = Location segment number aa = Absolute address of location oo = Old contents nn = New contents
		IN OWDATA cc ss aa oo nn tt OP OW COMPL	Output complete
5	INH:OW	PF tt ALW OW INH	Deactivates overwrite program

TABLE V

GENERIC AND ISSUE HEADER INSERTION

STEP	PROCEDURE	RESPONSE	REMARKS
	See Note*		
1	RST:DEVICE:TDC 0!	IP tt DEVICE REPT TDC 0 STATE AVL x1 x2 x3 x4 (or) OK	Place TDC 0 in service
2	RST:DEVICE:TDC 1!	IP tt DEVICE REPT TDC 1 STATE AVL x1 x2 x3 x4 (or) OK	Place TDC 1 in service
3	ALW:TAPEUTIL!	PF tt ALW TAPEUTIL COMPL	Activate tape utilities
4	EX:TDC!	PF tt TAPEUTIL COMPL	Retensions tapes
5	INH:TAPEUTIL!	PF tt TAPEUTIL INH	Inhibit tape utilities
6	DGN:TDC 0!	IP tt DGN TDC 0 ATP	TDC 0 tested successfully
7	DGN:TDC 1!	IP tt DGN:TDC 1 ATP	TDC 1 tested successfully
8	ALW:OW!	PF tt ALW OW COMPL	Requests activation of overwrite program
9	IN:GENID:xxxxxxxx!	OK	xxxxxxxx = New GENID to be written on the tape
10	IN:ISSID:zzzzzzzz!	OK	zzzzzzzz = New ISSID to be written on the tape

Note: The procedures in steps 1 through 7 need not be performed if the new cartridge was just inserted.

TABLE V (Contd)

GENERIC AND ISSUE HEADER INSERTION

STEP	PROCEDURE	RESPONSE	REMARKS
11	INIT:OWFILE! ***Caution:*** This message wipes out the entire OW file and writes the new GENID and ISSID on the tape. NOT TO BE USED ON A KNOWN GOOD TAPE	PF tt INIT OWFILE COMPL	Initializes overwrite file
12	UPD:OWFILE!	PF tt UPD OWFILE COMPL	Updates header information on first block of overwrite file on tape
13	INH:OW!	PF tt ALW OW INH	Deactivates overwrite program

TABLE W

REPLACE GENID AND ISSID

STEP	PROCEDURE	RESPONSE	REMARKS
1*	Perform steps 1-7 of Table P		
2†	ALW:OW!	PF tt ALW OW COMPL	Requests activation of overwrite program
3	IN:GENID:xxxxxxxx!	OK	xxxxxxxx = New GENID to be entered on tape
4	IN:ISSID:zzzzzzzz!	OK	zzzzzzzz = New ISSID to be entered on tape
5	UPD:OWFILE!	PF tt UPD OWFILE COMPL	Updates header information on first block of overwrite file on tape
6	INH:OW!	PF tt ALW OW INH	Deactivates overwrite program

* Step 1 is not necessary if it was performed earlier in the overwrite procedure.

† Step 2 need not be performed if the overwrite program is already active.

TABLE X

LOADING NEW OR OLD DATA

STEP	PROCEDURE	RESPONSE	REMARKS
1*	Perform steps 1 thru 7 of Table P.		
2†	ALW:OW!	PF tt ALW OW COMPL	Requests activation of overwrite program.
3	IN:OW n;TAPE!	PF tt IN OW COMPL	Loads overwrite "n" from tape to overwrite buffer.
4	Operate LOCK key on SSP	tt REPT CU STAT UAV	Prevents a control unit switch while loading overwrite.
5	LOD:OW:xxx!	PF tt LOD OW COMPL	Overwrites data in off-line main store with the data either in the overwrite buffer for resident programs or off-line tape for nonresident programs. xxx = OLD if old data. Overwrites the present program data with the old data in the overwrite buffer (used to remove an overwrite). xxx = NEW if new data. Overwrites the present program data with the new data in the overwrite buffer (used to enter an overwrite).

* Step 1 is not necessary if it was performed earlier in the overwrite procedure.

† Step 2 need not be performed if the overwrite program is already active.

TABLE X (Contd)

LOADING NEW OR OLD DATA

STEP	PROCEDURE	RESPONSE	REMARKS
			If INH returned rather than COMPL, the load failed. Failure may be caused by a tape operation problem or by a check number mismatch. Check that VFY:OW-DATA was successful.
6	VFY:OW:xxx!	PF tt VFY OW COMPL	Compares data in store or on tape with contents of overwrite buffer xxx = OLD if old data xxx = NEW if new data
7	Release LOCK key on SSP	tt REPT CU STAT AVL	Control unit returned to available status
8	SW:CU!	OK tt SW CU COMPL x	Switch to other control unit x = on-line control unit
9	Repeat Steps 4-7		
10	If the overwrite is to be deactivated and/or removed, use the procedures in Table S and/or T at this time		
11	INH:OW!	PF tt ALW OW INH	Deactivates overwrite program

TABLE Y

GENERATING OVERWRITE CHECK NUMBERS

STEP	PROCEDURE	RESPONSE	REMARKS
1	ALW:OW!	PF	Requests activation of overwrite program.
		ALW OW COMPL	Overwrite program is activated.
2	IN:GENID:xxxxxxxx!	OK	Identifies the generic ID to which overwrite applies.
3	IN:ISSID:zzzzzzzz!	OK	Identifies the generic issue ID to which overwrite applies.
4	IN:OW n;TTY ,NOCHECK!	PF	Overwrite "n" is about to be entered via the TTY. The NOCHECK keyword inhibits check number verification.
		IN OW COMPL	The overwrite header information has been formatted in the overwrite buffer. It has been verified that the tape contains issue "zzzzzzzz" of generic "xxxxxxxx", and it does not contain overwrite "n".
			If the check fails, the response is IN OW INH.
5	IN:OWDATA:cc,ss,aa,oo,nn!	OK	The location at absolute address "aa" in segment "ss" is being changed from old "oo" to new "nn". The OK response indicates that address "aa" is an equipped address. If "aa" is not equipped the response is NG. The data is entered into the overwrite buffer.
6	IN:OWDATA:cc,ss,aa,oo,nn!	OK	The data is entered into the overwrite buffer.
7	IN:OWDATA;cc,ss,aa,oo,nn!	OK	The data is entered into the overwrite buffer.
8	VFY:OW:OLD!	PF	Retrieve the current contents of the locations identified in the buffer and compare it to the old data entered via the IN:OWDATA messages.
		VFY OW COMPL	The data is compared. If a mismatch is detected, a VFY OW ERR message is returned to identify the error fed by the VFY OW INH response.

TABLE Y (Contd)

GENERATING OVERWRITE CHECK NUMBERS

STEP	PROCEDURE	RESPONSE	REMARKS
9	OP:OW;TAPE!	PF	Append the overwrite data in the buffer to the end of the overwrite file on tape. The overwrite status at this point is inactive. Consequently, if a system initialization results in a program reload at this point, this overwrite will not be used.
		OP OW COMPL	The tape write was successful.
			The failure response is OP OW INH.
10	IN:OW n;TAPE!	PF	This step is functionally superfluous, but is included so that the data tested is actually the data on the tape. The overwrite buffer is loaded with the contents of the overwrite file "n" from the cartridge tape.
		IN OW COMPL	The data was read from the tape successfully.
			The failure response is IN OW INH.
11	Operate LOCK key on SSP.		This prevents a control unit switch while the off-line store is being loaded. A switch would almost certainly be "fatal" because the store, containing half an overwrite, would be inconsistent.
12	LOD:OW:NEW!	PF	Requests that the new data be used to overwrite the off-line store (resident) or the off-line tape (nonresident).
		LOD OW COMPL	The overwrite operation was successful.
			The failure response is LOAD OW INH.
13	Release LOCK key on SSP		

TABLE Y (Contd)

GENERATING OVERWRITE CHECK NUMBERS

STEP	PROCEDURE	RESPONSE	REMARKS
14	VFY:OW:NEW!	PF	Verifies that the new contents of store matches the new data in the overwrite buffer.
15	SW:CU!	VFY OW COMPL OK	The store was loaded successfully. Switches to the control unit with the overwritten data.
	(Test data)		The test should exercise the overwritten data. In particular, the execution of an overwritten nonresident program should be requested. If the test fails, a switch to the original control unit should be requested and the following LOD OW message should be qualified with OLD rather than NEW to remove the overwritten data.
16	Operate LOCK key on SSP.		The test passed. This prevents a control unit switch.
17	LOD:OW:NEW!	PF	Overwrites the second store or cartridge tape unit.
		LOD OW COMPL	The overwrite operation was successful.
			The failure response is LOD OW INH.
18	Release LOCK key on SSP.		The new overwrite data is now active in the system, but a program reload initialization will still result in its elimination from store. The data still exists on the cartridge tape in the inactive state.

TABLE Y (Contd)

GENERATING OVERWRITE CHECK NUMBERS

STEP	PROCEDURE	RESPONSE	REMARKS
19	ACT:OW n!	PF	Marks the overwrite "n" active in the overwrite file so that subsequent program reload initializations will include overwrite "n".
		ACT OW COMPL	Activation was successful.
			The failure response is ACT OW INH.
20	UPD:OW!	PF	Updates the checksum file on the cartridge tape to reflect overwrite "n".
		UPD OW COMPL	The checksum file update was successful.
			The failure response is UPD OW INH.
21	OP:BWT!*	PF	Prints out the overwrite data including check numbers via the TTY.
22	INH:OW!	OK	Deactivates the overwrite program.

* A typical output resulting from the input message OP:BWT is shown below.

```
06 IN OW 1
   IN OWDATA 60 0 09000 8EBA 8EBA
   IN OWDATA 70 0 09001 AB20 AB20
   IN OWDATA 73 0 09002 4EBF 4EBF
   VFY OWDATA 203
06 OP BWT COMPL
```

P. Manual Operation Procedures

Prerequisites

2.55 Generally, the power must be applied.

2.56 Activation of the TEST MODE switch permits panel operations on the ***on-line*** 3A CC. Activation of the MANUAL switch permits panel operations on the **off-line** 3A CC.

2.57 For most of the manual procedures associated with the 3A CC Control Panel (those that require use of the COMMAND EXECUTE switch), bit 13 of the Interrupt Mask Register must be cleared (logical zero) to permit panel interrupts. (See paragraph 2.59.)

2.58 Normally all 3A CC Control Panel toggle switches should be in the DOWN position **before** beginning **any** of the manual procedures. One exception to this general case could be the HALT switch, which may or may not have already been activated due to the fact that the 3A CC may have been halted because of hardware, hardware/software, or operator manipulation. **The operator may have to use the halt switch during or before the manual procedures in order to obtain proper results. Operator discretion is required in such cases.**

Q. Panel Interrupts

2.59 The 3A CC panel interrupt is obtained by operating the COMMAND EXECUTE switch when **either** of the following conditions are present:

(a) ***Condition 1***—The MANUAL switch is activated and the 3A CC is off-line.

(b) ***Condition 2***—The TEST MODE switch is activated and the 3A CC is **on-line.**

Warning: Operation of the TEST MODE switch in the on-line 3A CC may cause interruption of service.

2.60 The panel interrupt is effective when **both** the following conditions are present:

(a) Bit 13 of the Interrupt Mask Register is logical zero.

(b) The Block Interrupts Flip-Flop is logical zero.

Note: Tables Z through AN provide practical information relating to manual operation procedures.

TABLE Z

DISPLAY A GENERAL REGISTER

STEP	SWITCH(ES)	REGISTER SELECTION	SWITCH POSITION(S) *	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL		GENERAL (D)	GENERAL
2	REGISTER SELECT			
	8 4 2 1	†a	8 4 2 1	
		GR 0	D D D D	0
		GR 1	D D D U	1
		GR 2	D D U D	2
		GR 3	D D U U	3
		GR 4	D U D D	4
		GR 5	D U D U	5
		GR 6	D U U D	6
		GR 7	D U U U	7
		GR 8	U D D D	8
		GR 9	U D D U	9
		GR 10	U D U D	10
		GR 11	U D U U	11
		GR 12	U U D D	12
		GR 13	U U D U	13
		GR 14	U U U D	14
		GR 15	U U U U	15
3	REGISTER DISPLAY		UP	
4	COMMAND EXECUTE		momentary DOWN	‡b

* U = UP, D = DOWN
† GR = General Register
‡ The command is executed if the COMMAND REJECT lamp does **not** come on.

TABLE AA

LOAD AND DISPLAY A GENERAL REGISTER

STEP	SWITCH(ES)	REGISTER SELECTION	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL		GENERAL (D)	GENERAL
2	REGISTER SELECT			
	8 4 2 1	†	8 4 2 1	
		GR 0	D D D D	0
		GR 1	D D D U	1
		GR 2	D D U D	2
		GR 3	D D U U	3
		GR 4	D U D D	4
		GR 5	D U D U	5
		GR 6	D U U D	6
		GR 7	D U U U	7
		GR 8	U D D D	8
		GR 9	U D D U	9
		GR 10	U D U D	10
		GR 11	U D U U	11
		GR 12	U U D D	12
		GR 13	U U D U	13
		GR 14	U U U D	14
		GR 15	U U U U	15
3	REGISTER LOAD		UP	
4	REGISTER DISPLAY		UP	
5	LOAD AND DISPLAY (19-0)		binary data ‡	LOAD AND DISPLAY (19-0)§
6	COMMAND EXECUTE		momentary DOWN	¶

* U = UP, D = DOWN
† GR = General Register
‡ Set the switches to the binary equivalent of the DATA to be loaded (logical 0 = DOWN, logical 1 = UP).
§ The lamps corresponding to UP switches are on.
¶ The command is executed if the COMMAND REJECT lamp does **not** come on.

TABLE AB

LOAD A GENERAL REGISTER WITH INCORRECT PARITY

STEP	SWITCH(ES)	REGISTER SELECTION	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL		GENERAL (D)	GENERAL
2	REGISTER SELECT 8 4 2 1	† GR 0 GR 1 GR 2 GR 3 GR 4 GR 5 GR 6 GR 7 GR 8 GR 9 GR 10 GR 11 GR 12 GR 13 GR 14 GR 15	8 4 2 1 D D D D D D D U D D U D D D U U D U D D D U D U D U U D D U U U U D D D U D D U U D U D U D U U U U D D U U D U U U U D U U U U	 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
3	REGISTER LOAD		UP	
4	REGISTER DISPLAY		UP	
5	LOAD AND DISPLAY (19-0)		binary data ‡	LOAD AND DISPLAY (19-0) §
6	ENABLE MANUAL PAR		UP	ENABLE MANUAL PAR
7	PL		¶	PL if switch UP
8	PH		**	PH if switch UP
9	EXECUTE		momentary DOWN	††

* U = UP, D = DOWN
† GR = General Register
‡ Set the switches to the binary equivalent of the DATA to be loaded (logical 0 = DOWN, logical 1 = UP).
§ The lamps corresponding to UP switches are on.
¶ The number of LOAD AND DISPLAY (7-0) lamps on: odd = UP, even = DOWN.
** The number of LOAD AND DISPLAY lamps (19-8) on: odd = UP, even = DOWN.
†† The command is executed if the COMMAND REJECT lamp does **not** come on.

TABLE AC

DISPLAY A SPECIAL REGISTER

STEP	SWITCH(ES)	REGISTER SELECTION	SWITCH POSITION(S)*	VERIFICATION LAMP(S)	BIT TABLE
1	SPECIAL/GENERAL		SPECIAL (U)	SPECIAL	
2	REGISTER SELECT 8 4 2 1		8 4 2 1		
		Microcontrol Status Reg.	D D D D	MCTL STAT	AC
		Timing Counter	D D D U	TIM	
		System Status Reg.	D D U D	SYS STAT	AD
		Store Address Reg.	D D U U	ST ADRS	AE
		Program Address Reg.	D U D D	PROG ADRS	
		Maintenance State Reg.	D U D U	MTCE STA	AF
		Main Memory Status Reg.	D U U D	M. MEM STAT	AG
		Maintenance Channel Buffer	D U U U	MCH BUFR	
		Interrupt Set Reg.	U D D D	INT SET	AH
		Interrupt Mask Reg.	U D D U	INT MASK	
		Hold Get Reg.	U D U D	HOLD GET	
		Error Reg.	U D U U	ERR	AI
		Data Mask Reg.	U U D D	DATA MASK	
		Data Input Reg.	U U D U	DATA IN	
		Address Mask Reg.	U U U D	ADR MASK	
4	COMMAND EXECUTE		momentary DOWN	†	

* U = UP, D = DOWN

† The command is executed if the COMMAND REJECT lamp does **not** come on.

TABLE AD

LOAD AND DISPLAY A SPECIAL REGISTER

STEP	SWITCH(ES)	REGISTER SELECTION	SWITCH POSITION(S)*	VERIFICATION LAMP(S)	BIT TABLE
1	SPECIAL/GENERAL		SPECIAL (U)	SPECIAL	
2	REGISTER SELECT 8 4 2 1		8 4 2 1		
		Microcontrol Status Reg.	D D D D	MCTL STAT	AC
		Timing Counter	D D D U	TIM	
		System Status Reg.	D D U D	SYS STAT	AD
		Store Address Reg.	D D U U	ST ADRS	AE
		Program Address Reg.	D U D D	PROG ADRS	
		Maintenance State Reg.	D U D U	MTCE STA	AF
		Main Memory Status Reg.	D U U D	M. MEM STAT	AG
		Maintenance Channel Buffer	D U U U	MCH BUFR	
		Interrupt Set Reg.	U D D D	INT SET	AH
		Interrupt Mask Reg.	U D D U	INT MASK	
		Hold Get Reg.	U D U D	HOLD GET	
		Error Reg.	U D U U	ERR	AI
		Data Mask Reg.	U U D D	DATA MASK	
		Data Input Reg.	U U D U	DATA IN	
		Address Mask Reg.	U U U D	ADR MASK	
5	LOAD AND DISPLAY (19-0)		binary date †	LOAD AND DISPLAY (19-0) ‡	
6	COMMAND EXECUTE		momentary DOWN	§	

* U = UP, D = DOWN

† Set the switches to the binary equivalent of the DATA to be loaded (logical 0 = DOWN, logical 1 = UP).

‡ The lamps corresponding to UP switches are on.

§ The command is executed if the COMMAND REJECT lamp does **not** come on.

TABLE AE

LOAD A SPECIAL REGISTER WITH INCORRECT PARITY

STEP	SWITCH(ES)	REGISTER SELECTION	SWITCH POSITION(*)	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL		SPECIAL (U)	SPECIAL
2	REGISTER SELECT 8 4 2 1		8 4 2 1	
		Microcontrol Status Reg.	D D D D	MCTL STAT
		Timing Counter	D D D U	TIM
		System Status Reg.	D D U D	SYS STAT
		Store Address Reg.	D D U U	ST ADRS
		Program Address Reg.	D U D D	PROG ADRS
		Maintenance State Reg.	D U D U	MTCE STA
		Main Memory Status Reg.	D U U D	M. MEM STAT
		Maintenance Channel Buffer	D U U U	MCH BUFR
		Interrupt Set Reg.	U D D D	INT SET
		Interrupt Mask Reg.	U D D U	INT MASK
		Hold Get Reg.	U D U D	HOLD GET
		Error Reg.	U D U U	ERR
		Data Mask Reg.	U U D D	DATA MASK
		Data Input Reg.	U U D U	DATA IN
		Address Mask Reg.	U U U D	ADR MASK
3	REGISTER LOAD		UP	
4	REGISTER DISPLAY		UP	
5	LOAD AND DISPLAY (19-0)		binary data †	LOAD AND DISPLAY (19-0) ‡
6	ENABLE MANUAL PARITY		UP	ENABLE MANUAL PARITY
7	PL		§	PL if switch UP
8	PH		¶	PH if switch UP
9	COMMAND EXECUTE		momentary DOWN	**

* U = UP, D = DOWN
† Set the switches to the binary equivalent of the DATA to be loaded (logical 0 = DOWN, logical = UP).
‡ The lamps corresponding to UP switches are on.
§ The number of LOAD AND DISPLAY (7-0) lamps on: odd = UP, even = DOWN.
¶ The number of LOAD and DISPLAY lamps (19-8) on: odd = UP, even = DOWN.
** The command is executed if the COMMAND REJECT lamp does **not** come on.

TABLE AF

DISPLAY CONTENTS OF STORE

STEP	SWITCH(ES)	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL	SPECIAL (UP)	SPECIAL
2	REGISTER SELECT 8 4 2 1	8 4 2 1 D D U U	ST ADRS
3	REGISTER LOAD	UP	
4	REGISTER DISPLAY	UP	
5	LOAD AND DISPLAY (19-0)	binary data †	LOAD AND DISPLAY (19-0) ‡
6	COMMAND EXECUTE	momentary DOWN	§
7	REGISTER LOAD	DOWN	
8	REGISTER DISPLAY	DOWN	
9	MEMORY DISPLAY	UP	
10	COMMAND EXECUTE	momentary DOWN	§

* U = UP, D = DOWN

† Set the switches to the binary equivalent of the ADDRESS to be displayed (logical 0 = DOWN, logical 1 = UP).

‡ The lamps corresponding to UP switches are on.

§ The command is executed if the COMMAND REJECT lamp does **not** come on.

TABLE AG

DISPLAY CONSECUTIVE CONTENTS OF STORE

STEP	SWITCH(ES)	SWITCH POSITION(S) *	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL	SPECIAL (UP)	SPECIAL
2	REGISTER SELECT 8 4 2 1	8 4 2 1 D D U U	ST ADRS
3	REGISTER LOAD	UP	
4	REGISTER DISPLAY	UP	
5	LOAD AND DISPLAY (19-0)	binary data †	LOAD AND DISPLAY (19-0) ‡
6	COMMAND EXECUTE	momentary DOWN	§
7	REGISTER LOAD	DOWN	
8	REGISTER DISPLAY	DOWN	
9	MEMORY DISPLAY	UP	
10	COMMAND EXECUTE	momentary DOWN	§
11	MEMORY INCR ADR	UP	
12	COMMAND EXECUTE	momentary DOWN	
13	Repeat step 12 for each word to be displayed.		

* U = UP, D = DOWN

† Set the switches to the binary equivalent of the ADDRESS to be displayed (logical 0 = DOWN, logical 1 = UP).

‡ The lamps corresponding to UP switches are on.

§ The command is executed if the COMMAND REJECT lamp does **not** come on.

TABLE AH

WRITE CONTENTS OF STORE

STEP	SWITCH(ES)	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL	SPECIAL (UP)	SPECIAL
2	REGISTER SELECT 8 4 2 1	8 4 2 1 D D U U	ST ADRS
3	REGISTER LOAD	UP	
4	REGISTER DISPLAY	UP	
5	LOAD AND DISPLAY (19-0)	binary data †	LOAD AND DISPLAY (19-0) ‡
6	COMMAND EXECUTE	momentary DOWN	
7	REGISTER LOAD	DOWN	
8	REGISTER DISPLAY	DOWN	
9	LOAD AND DISPLAY	binary data ¶	LOAD AND DISPLAY (19-0) ‡
10	MEMORY STORE	UP	
11	MEMORY DISPLAY	UP	
12	COMMAND EXECUTE	momentary DOWN	§

* U = UP, D = DOWN

† Set the switches to the binary equivalent of the ADDRESS to be loaded (logical 0 = DOWN, logical 1 = UP).

‡ The lamps corresponding to UP switches are on.

§ The command is executed if the COMMAND REJECT lamp does **not** come on.

¶ Set the switches to the binary equivalent of the DATA to be written into the previously selected ADDRESS (logical 0 = DOWN, logical 1 = UP).

TABLE AI

WRITE CONSECUTIVE CONTENTS OF STORE

STEP	SWITCH(ES)	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL	SPECIAL (UP)	SPECIAL
2	REGISTER SELECT 8 4 2 1	8 4 2 1 D D U U	ST ADRS
3	REGISTER LOAD	UP	
4	REGISTER DISPLAY	UP	
5	LOAD AND DISPLAY (19-0)	binary data †	LOAD AND DISPLAY (19-0) ‡
6	COMMAND EXECUTE	momentary DOWN	
7	REGISTER LOAD	DOWN	
8	REGISTER DISPLAY	DOWN	
9	LOAD AND DISPLAY	binary data ¶	LOAD AND DISPLAY (19-0) ‡
10	MEMORY STORE	UP	
11	MEMORY DISPLAY	UP	
12	MEMORY INCR ADR	UP	
13	COMMAND EXECUTE	momentary DOWN	§
14	LOAD AND DISPLAY (19-0)	binary data **	LOAD AND DISPLAY (19-0) †
15	COMMAND EXECUTE	momentary DOWN	§
16	Repeat steps 14 and 15 until all words have been written.		

* U = UP, D = DOWN

† Set the switches to the binary equivalent of the ADDRESS to be loaded (logical 0 = DOWN, logical 1 = UP).

‡ The lamps corresponding to UP switches are on.

§ The command is executed if the COMMAND REJECT lamp does **not** come on.

¶ Set the switches to the binary equivalent of the DATA to be written into the previously selected ADDRESS (logical 0 = DOWN, logical 1 = UP).

** Set the switches to the binary equivalent of the DATA to be written into the NEXT word.

TABLE AJ

COMPARE ADDRESS

STEP	SWITCH(ES)	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL	SPECIAL (UP)	SPECIAL
2	REGISTER SELECT 8 4 2 1	8 4 2 1 U U U D	ADR MASK
3	REGISTER LOAD	UP	
4	REGISTER DISPLAY	UP	
5	LOAD AND DISPLAY (19-0)	ALL DOWN	LOAD AND DISPLAY (19-0) †
6	COMMAND EXECUTE	momentary DOWN	
7	REGISTER LOAD	DOWN	
8	REGISTER SELECT 8 4 2 1	8 4 2 1 U D D U	INT MASK
9	COMMAND EXECUTE	momentary DOWN	‡
10	LOAD AND DISPLAY (19-0)	match lamps §	
11	LOAD AND DISPLAY (switch 3)	DOWN	
12	REGISTER LOAD	UP	
13	COMMAND EXECUTE	momentary DOWN	‡
14	REGISTER SELECT 8 4 2 1	8 4 2 1 U U U U	ADR IN

* U = UP, D = DOWN
† All lamps are off.
‡ The command is executed if the COMMAND REJECT lamp does **not** come on.
§ Set the switches according to their corresponding lamps (ie, lamp on = UP, lamp off = DOWN)

TABLE AJ (Contd)

COMPARE ADDRESS

STEP	SWITCH(ES)	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
15	LOAD AND DISPLAY (19-0)	binary data ¶	LOAD AND DISPLAY (19-0) **
16	COMMAND EXECUTE	momentary DOWN	‡
17	REGISTER LOAD	DOWN	
18	REGISTER DISPLAY	DOWN	
19	COMPARE ADR	UP	

* U = UP, D = DOWN

‡ The command is executed if the COMMAND REJECT lamp does **not** come on.

¶ Set the switches to the binary equivalent of the ADDRESS to be compared (logical 0 = DOWN, logical 1 = UP).

** The lamps corresponding to UP switches are on.

TABLE AK

COMPARE DATA

STEP	SWITCH(ES)	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL	SPECIAL (UP)	SPECIAL
2	REGISTER SELECT 8 4 2 1	8 4 2 1 U U D D	DATA MASK
3	REGISTER LOAD	UP	
4	REGISTER DISPLAY	UP	
5	LOAD AND DISPLAY (19-0)	ALL UP	LOAD AND DISPLAY (19-0) †
6	COMMAND EXECUTE	momentary DOWN	
7	REGISTER LOAD	DOWN	
8	REGISTER SELECT 8 4 2 1	8 4 2 1 U U D U	DATA IN
9	REGISTER LOAD	UP	
10	LOAD AND DISPLAY (19-0)	binary data §	LOAD AND DISPLAY (19-0) ¶
11	COMMAND EXECUTE	momentary DOWN	‡
12	REGISTER LOAD	DOWN	
13	REGISTER DISPLAY	DOWN	
14	COMPARE DATA	UP	

* U = UP, D = DOWN
† All lamps are on.
‡ The command is executed if the COMMAND REJECT lamp does NOT come on.
§ Set the switches to the binary equivalent of the DATA to be compared (logical 0 = DOWN, logical 1 = UP).
¶ The lamps corresponding to UP switches are on.

TABLE AL

COMPARE ADDRESS AND DATA

STEP	SWITCH(ES)	SWITCH POSITION(S) *	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL	SPECIAL (UP)	SPECIAL
2	REGISTER SELECT 8 4 2 1	8 4 2 1 U U U D	ADR MASK
3	REGISTER LOAD	UP	
4	REGISTER DISPLAY	UP	
5	LOAD AND DISPLAY (19-0)	ALL DOWN	LOAD AND DISPLAY (19-0) †
6	COMMAND EXECUTE	momentary DOWN	
7	REGISTER LOAD	DOWN	
8	REGISTER SELECT 8 4 2 1	8 4 2 1 U D D U	INT MASK
9	COMMAND EXECUTE	momentary DOWN	‡
10	LOAD AND DISPLAY (19-0)	match lamps §	
11	LOAD AND DISPLAY (switch 3)	DOWN	
12	REGISTER LOAD	UP	
13	COMMAND EXECUTE	momentary DOWN	‡
14	REGISTER SELECT 8 4 2 1	8 4 2 1 U U U U	ADR IN

Note: An interrupt will occur when **either** compare is found; **not both.**

* U = UP, D = DOWN

† All lamps are off.

‡ The command is executed if the COMMAND REJECT lamp does **not** come on.

§ Set the switches according to their corresponding lamps (ie, lamp on = UP, lamp off = DOWN)

TABLE AL (Contd)

COMPARE ADDRESS AND DATA

STEP	SWITCH(ES)	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
15	LOAD AND DISPLAY (19-0)	binary data ¶	LOAD AND DISPLAY (19-0) **
16	COMMAND EXECUTE	momentary DOWN	‡
17	REGISTER LOAD	DOWN	
18	REGISTER DISPLAY	DOWN	
19	COMPARE ADR	UP	
20	REGISTER SELECT 8 4 2 1	8 4 2 1 U U D D	DATA MASK
21	REGISTER LOAD	UP	
22	REGISTER DISPLAY	UP	
23	LOAD AND DISPLAY (19-0)	ALL UP	LOAD AND DISPLAY (19-0) ††
24	COMMAND EXECUTE	momentary DOWN	†
25	REGISTER LOAD	DOWN	
26	REGISTER SELECT 8 4 2 1	8 4 2 1 U U D U	DATA IN
27	REGISTER LOAD	UP	

Note: An interrupt will occur when **either** compare is found; **not both.**

* U = UP, D = DOWN

‡ The command is executed if the COMMAND REJECT lamp does **not** come on.

¶ Set the switches to the binary equivalent of the DATA to be written into the previously selected ADDRESS (logical 0 = DOWN, logical 1 = UP).

†† All lamps are on.

** The lamps corresponding to UP switches are on.

TABLE AL (Contd)

COMPARE ADDRESS AND DATA

STEP	SWITCH(ES)	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
28	LOAD AND DISPLAY (19-0)	binary data §§	LOAD AND DISPLAY (19-0) **
29	COMMAND EXECUTE	momentary DOWN	†
30	REGISTER LOAD	DOWN	
31	REGISTER DISPLAY	DOWN	
32	COMPARE DATA	UP	

† The command is executed if the COMMAND REJECT lamp does **not** come on.
** The lamps corresponding to UP switches are on.
§§ Set the switches to the binary equivalent of the DATA to be compared (logical 0 = DOWN, logical 1 = UP).

TABLE AM

EXECUTE A PROGRAM

STEP	SWITCH(ES)	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL	SPECIAL (UP)	SPECIAL
2	REGISTER SELECT 8 4 2 1	8 4 2 1 D U D D	PROG ADRS
3	REGISTER LOAD	UP	
4	REGISTER DISPLAY	UP	
5	LOAD AND DISPLAY (19-0)	binary data †	LOAD AND DISPLAY (19-0) ‡
6	COMMAND EXECUTE	momentary DOWN	§
7	REGISTER LOAD	DOWN	
8	REGISTER DISPLAY	DOWN	
9	MODE HALT	DOWN	¶
11	COMMAND EXECUTE	momentary DOWN	§

* U = UP, D = DOWN
† Set the switches to the binary equivalent of the ADDRESS of the first word of the program to be executed (logical 0 = DOWN, logical 1 = UP).
‡ The lamps corresponding to UP switches are on.
§ The command is executed if the COMMAND REJECT lamp does **not** come on.
¶ The HALTED lamp extinguishes.

TABLE AN

EXECUTE A PROGRAM STEP-BY-STEP

STEP	SWITCH(ES)	SWITCH POSITION(S)*	VERIFICATION LAMP(S)
1	SPECIAL/GENERAL	SPECIAL (UP)	SPECIAL
2	REGISTER SELECT 8 4 2 1	8 4 2 1 D U D D	PROG ADRS
3	REGISTER LOAD	UP	
4	REGISTER DISPLAY	UP	
5	LOAD AND DISPLAY (19-0)	binary data †	LOAD AND DISPLAY (19-0) ‡
6	COMMAND EXECUTE	momentary DOWN	
7	REGISTER LOAD	DOWN	
8	REGISTER DISPLAY	DOWN	
9	MODE STEP	UP	
10	MODE HALT	DOWN	¶
11	COMMAND EXECUTE	momentary DOWN	§
12	Repeat step 11 for each instruction to be executed.		

* U = UP, D = DOWN

† Set the switches to the binary equivalent of the ADDRESS of the first word of the program to be executed (logical 0 = DOWN, logical 1 = UP).

‡ The lamps corresponding to UP switches are on.

§ The command is executed if the COMMAND REJECT lamp does NOT come on.

¶ The HALTED lamp extinguishes.

R. Automatic Operations

2.61 Several operations that are accomplished manually via the control panel can also be accomplished by software via appropriate TTY input messages or commands. These operations involve dumping (displaying) and loading the contents of registers and store. Table AO lists these TTY commands. For detailed information on the usage of the TTY commands consult the EOS Input Manual IM-4C001-01. Table AP provides a broad listing of reference documents pertaining to the 3A Central Control.

S. Register Bit Assignments

2.62 The following tables (AQ through AW) show the bit assignments of the system registers.

TABLE AO
TTY COMMANDS

COMMAND	FUNCTION
DMP:REG OFL	Dumps contents of **both** General and Special Registers in the off-line 3A CC
DMP:ST	Dump block of store
LOD:INDIR	Load store indirectly
LOD:REG	Load General Register
LOD:ST	Load store

TABLE AP
3A CENTRAL CONTROL
REFERENCE DOCUMENTS

DOCUMENT	SUBJECT
IM-2H200-04	Input Message Manual, No. 2B Electronic Switching System (ESS)
OM-2H200-04	Output Message Manual, No. 2B Electronic Switching System (ESS)
IM-3H300-01	Input Message Manual, No. 3 Electronic Switching System (ESS)
OM-3H300-01	Output Message Manual, No. 3 Electronic Switching System (ESS)
IM-4C001-01	Input Message Manual (EOS) for the Extended Operating System
OM-4C001-01	Output Message Manual (EOS) for the Extended Operating System
TLM-1C900-01	Common Systems Processor Trouble Locating Manual
TLM-4C706-01	Tape Data Cartridge TLM (CTAPM) Trouble Locating Manual
232-100-100	No. 2B Electronic Switching System (ESS)
233-000-003	No. 3 Electronic Switching System (ESS)
254-340-001	3A Processor Extended Operating System
254-300-110	3A Central Control, Description
254-300-120	3A Central Control, Theory of Operation
FA-1034	Console and 3A CC Interface
1C901-01	Schematic Diagram and Circuit Description

TABLE AQ

MICROCONTROL STATUS REGISTER BIT ASSIGNMENTS

BIT	MNEMONIC	FUNCTION
0-1	CF	**Conditional Flip-Flop** bits are used to pass status information to the main program; ie, to notify a program of results of a logical comparison of an operand set, etc.
2-3	DS	**Data Manipulation Logic Status** bits store results of certain DML operations; ie, address overflow, all ones in a find-low-zero test, etc.
4-5	TR1	**Test Register 1** bits are used for general purpose status by microprogram control to indicate some state occurred; ie, which RA has memory address, was read or write requested, etc.
6-7	TR2	Same as TR1.
8-9	DR	**Data Ready** bits are used to indicate that the last-initiated main memory operator is complete.
10-11	RU	**RAR Update** bits control the updating junction of the return address register used in conjuction with micoprogram subroutines. When set, RAR contents are saved, not updated as new MAR addresses are developed, to provide a return address after a microsubroutine is completed.
12-13	IFF	I — bits applies to applications of 3A CC where main memory words exceed 16 bits in length. When activated, extensions of SIR and SDR are utilized to buffer the enlarged memory words. I—bit also determines from which portion of the SIR the next OP code is to be obtained. THESE BITS ARE NOT UTILIZED IN 3A CC APPLICATIONS WITHIN A NO. 3 ESS.
14-15	OPF	**Op Code FIL** bits apply to applications of the 3A CC where the number of operational codes is expanded up to 256 codes. When clear, microstore area 256,384 is referenced by a new op code; when set, microstore area 2048 to 2176 is referenced by a new opcode. THESE BITS ARE NOT UTILIZED IN 3A CC APPLICATIONS WITHIN A NO. 3 ESS.
16-17	MARP	**Microstore Address Register Parity** bits fulfill an internal check function instead of a control function as the other Microcontrol Status bits; it reflects the status of the MAR parity.
18		
19		
PL	PL	Parity Low
PH	PH	Parity High

TABLE AR

SYSTEM STATUS REGISTER BIT ASSIGNMENTS

BIT	MNEMONIC	FUNCTION
0	AME	**Address Match Enable:** Enables address matching between Store Address Register and Address Input Register.
1	BHC	**Block Hardware Check:** Disables Error Register output which would cause processors to switch on-line status.
2	BIN	**Block Interrupt:** Inhibits recognition of any interrupts.
3	BTC	**Block Timer Check:** Inhibits inputs and outputs of program timer.
4	DME	**Data Match Enable:** Enables data matching between Store Data Register and Data Input Register.
5	HLT	**Halt:** Indicates that the 3A CC is not executing an instruction.
6	ISC1	**Initialization Sanity Check 1:** Verifies hardware initialization routine; when failure occurs, the ISC1 bit is set (logical one) and the off-line 3A CC is switched on-line.
7	ICS2	**Intialization Sanity Check 2:** Further check of the initialization routine. ISC1 ISC2 0 0 Normal initialization of on-line 3A CC 1 0 Stop and switch to off-line 3A CC 1 1 Bootstrap
8	LOF	**Lock Off-Line:** Disables the I/O channel so that the off-line 3A CC cannot interfere with the on-line processor; LOF can also be manually set from the System Status Panel.
9	LON	**Lock On-Line:** Prevents on-line 3A CC from being switched off-line; LON can also be manually set from the System Status Panel.

TABLE AR (Contd)

SYSTEM STATUS REGISTER BIT ASSIGNMENTS

BIT	MNEMONIC	FUNCTION
10	MAN	**Manual:** Places the 3A CC in manual mode and lights the MANUAL lamp on the control panel; set by operation of the MANUAL switch on the control panel.
11	MINT	**Microinterpret Mode:** Enables gating of contents of Store Instruction Register to Microstore Instruction Register in order to allow execution of microinstructions from MAS.
12	CC	**Central Control:** Indicates whether the 3A CC is on-line (CC = logical one) or off-line (CC = logical zero). Other functions are enabled to prevent interference from the off-line 3A CC.
13	REJ	**Reject:** Lights the REJECT lamp on the control panel to indicate that a requested panel action has been rejected.
14	STOP	**Stop:** Loads a maintenance routine address into the Microstore Address Register, which causes all zeroes to be read out of miscrostore.
15	DISA	**Disable:** Reads state of disable flip-flop in I/O enable and disable logic.
16	PRI	**Privilege:** Used for certain applications of the 3A CC that require a privilege mode for instruction execution; NOT USED IN NO. 3 ESS.
17	DISP	**Display:** Enables gating of the contents of Program Register to the Display Buffer.
18	BPC	**Block Bus Parity Check:** Inhibits Program Gating Bus parity check circuits.
19	IPLTRK	**Initiate Program Load Track:** Used by the microcode in the sequence that initiates a program reload from tape. The state of this bit determines which of two tracks on the tape will be read.
PL, Ph	CC0, CC1	**Central Control 0, Central Control 1:** Hard wired to determine which 3A CC is CC0 (PL = logical one and PH = logical zero) and which is CC1 (PL = logical zero and PH = logical one).

TABLE AS

STORE ADDRESS REGISTER BIT ASSIGNMENTS

BIT	MNEMONIC	FUNCTION
0	SAO	Bits 0 through 4 are used to select one of 32 rows of memory cell/chip (0-31).
1	SA1	
2	SA2	
3	SA3	
4	SA4	
5	SA5	Bits 5 through 9 are used to select one of 32 columns of memory cell/chip (0-31).
6	SA6	
7	SA7	
8	SA8	
9	SA9	
10	SA10	Bits 10 and 11 are used to select one of 4 memory chips (DIPS 0-3).
11	SA11	
12	SA12	Bits 12 through 14 are used to select one of 8 rows of dual in-line packages of memory (DIPS 0-7).
13	SA13	
14	SA14	
15	SA15	Bits 15 through 17 are used to define which one of 8 memory modules (0-7) within the MAS is be accessed.
16	SA16	
17	SA17	
18	SA18	Bits 18 and 19 are used to select the MAS (0-3) to be accessed.
19	SA19	
PL	SAPL	Parity low
PH	SAPH	Parity high

TABLE AT

MAINTENANCE STATE REGISTER BIT ASSIGNMENTS

BIT	MNEMONIC	FUNCTION
0	OVLOF	Override LOCK OFF-LINE
1	CLK 1	Clock Test Conditions
2	CLK 2	
3	CLK 3	
4	STRGO	Ground My Store Go Lead
6	FREEZ	Utility Freeze
7	MCMPT	Ground My Store Complete Lead, My Store Busy Lead, and inhibit Other Store Complete Lead
8	OCMPT	Ground Other Store Complete Lead, Other Store Busy Lead, and inhibit My Store Complete Lead
9	XYGATE	Enable IB (X, Y) to MIR when stopped and partially inhibit from check
10	MCADCMP	Enable RAR-MAR match independent of RU Flip-Flop plus divert Store Go Flip-Flops into Store Write Protect error bits
11	DISMARP	Hold MAR parity
12	DISTO	Disable to Field Decoder
13	COM 1	Code Merger Test 1
14	COM 2	Code Merger Test 2
15	STRIS	Jam Store Control Lead 3 = 1

TABLE AU

MAIN MEMORY STATUS REGISTER BIT ASSIGNMENTS

BIT	MNEMONIC	FUNCTION
0-1	MM1	**Memory Maintenance:** Used with MM2 and RW to formulate the command sent in a memory operation
2-3	MM2	**Memory Maintenance:** Used with MM1 and RW to formulate the command sent in a memory operation
4-5	RW	**Read or Write:** Indicates whether memory is to perform a read (logical one) or a write (logical zero) operation
6	IDL	**Idle:** If set, disables all communications to the other 3A CC memory
7	IDL	**Idle:** Complement of bit 6. If set, disables all communication from other 3A CC memory
8-9	UPD	**Update:** Indicates whether or not to update the off-line memory
10-11	ISO	**Isolate:** Prevents the other 3A CC from accessing the memory of this 3A CC
12-13	BDSR	**Block Double Store Read:** Inhibits double store read
14	CW	**Complement Write:** Activates complement write lead of MAS bus; controller will have last word, and store in the complement in the last read address
15	BEC	**Block Error Recovery:** Inhibits all error recovery procedures within the 3A CC associated with incorrect store read data
16	CW	Same as bit 14
17	BEC	Same as bit 15

TABLE AV

INTERRUPT SET REGISTER BIT ASSIGNMENTS

BIT	MNEMONIC	FUNCTION	SOFTWARE INTERRUPT
0	*	INTP A	
1	UTILI	Utility Interrupt (External) INTP B	INTe
2	*	INTP C	
3	ADMI	Address or Data Match	
4	*	INTP D	INTK
5	ERRI	Error Register (Internal)	
6	*	INTP E	INTj
7	OCCI	Other CC (External)	
8	5MSI	Hardware Interrupt (Timing Counter 5)	
9	TCI	Hardware Interrupt (Timing Counter 10)	
10	TTYEI	TTY and Tape-Even (External)	INTa/INTb
11	TTYOI	TTY and Tape-Odd (External)	INTc/INTd
12	*	INTP F	INTh
13	MANI	Manual Panel Execute	
14	*	INTP G	INTq
15	I	INTP H	INTf

* INTP A through H are assigned by application software.

TABLE AW

ERROR REGISTER BIT ASSIGMENTS

BIT	MNEMONIC	FUNCTION	ACTION
0	TODER	TO Decoder Error	
1	FRMDER	FROM Decoder Error	
2	IBER	IB X, Y Field Error	
3	BUSER	BUS Parity Error	
4	DMLER	DML Match Error	causes
5	MARER	MAR Parity Error	PU
6	CLKER	Clock Error	switch
7	MSTRER	My Store Error A	
8	MADER	MAR - RAR Match Error	
9	FRER	Function Register Parity Error	
10	SRPE	Store Read Parity Error (Error C)	causes double store read
11	MSTWRP	My Store Write Protect Error (Error B)	causes initialization
12	MFSTER	My Store Fast Time-Out Error	
13	BAER	Branch Allowed Error	
14	OWRTER	Other Store Write Protect Error	
15	OSTRER	Other Store Error	
16	OFSTM	Other Store Fast Time-Out Error	causes
17	IOMLTER	I/O Multiple Channel Select Error	interrupt
18	PTRER	PT Reset Received by On-Line CC Error	
19	SWER	Switch Received by On-Line CC Error	
PL	IOER	I/O Channel Error	
PH	IOPARER	I/O Bad Parity Received Error	

T. Data Cartridge Insertion and Removal

2.63 These procedures are provided as a reference and an aid in inserting and removing the data cartridge for the EOS, No. 2B ESS, and No. 3 ESS.

> ***Note:*** EOS supports the use of both 300-foot and 450-foot cartridges, but an application may not mix the use of these two tape lengths in the same generic; ie, the user cannot use a 300-foot and a 450-foot cartridge with the same generic.

U. Insertion of Data Cartridge

2.64 Insert the data cartridge according to the procedures in Tables AX through AZ.

V. Removal of Data Cartridge

2.65 Remove the data cartridge according to the procedures in Tables BA and BB.

> ***Caution: Failure to follow the procedure may result in a major alarm or endanger the data recorded on the tape, or both.***

W. Generic Program Restarts

2.66 The procedures in Table BC must be followed when changing the issue of the EOS Generic Program.

X. References

2.67 The reference documents listed in Table BD may contain useful information relating to the operation of the Tape Data Controller and the Cartridge Tape Transport.

TABLE AX

DATA CARTRIDGE INSERTION - EOS

STEP	PROCEDURE	RESPONSE	REMARKS
1	At the TDC observe the TDC POWER lamps.	TDC POWER lamps must be lighted.	
2	At the SSP observe the TDC LED.	TDC LED must be lighted.	TDC POWER and TDC LED must be lighted before inserting data cartridge.
3	At the TDC: Insert the data cartridge.		Data cartridge must have the same issue as the generic cartridge. Check also that the cartridge length (300 or 450 foot length) is correct for the generic.
4	Type on the TTY: INIT:DEVICE:TDC a!	Tape will move. COMPL	a = TDC number 0 or 1. TDC initialized.
5	Repeat Step 4 four times if tape was previously inactive.		Restores proper tape tension.

TABLE AX (Contd)

DATA CARTRIDGE INSERTION - EOS

STEP	PROCEDURE	RESPONSE	REMARKS
6	Type on the TTY:		
	DGN:DEVICE TDC a!	ATP	a = TDC number 0 or 1. Performs diagnostics. ATP = all tests passed.
	ALW:TAPEUTIL!	COMPL	Activates utilities.
		OK	Utilities activated.
	COPY:FILE(a,b), ADD 0, PATCH!	COMPL	a = TDC file copied from. b = TDC file to receive copy. ***Caution:*** Do **NOT** perform any procedure requiring tape reading, unless response **OK** is obtained from CONFIRM:COPY.
	CONFIRM:COPY!	OK	Copy confirmed.
7	If NEW cartridge was inserted, type:		
	OP:DATA, CURRENT a,ALL!	OK	a = TDC number 0 or 1. Copies all translation file and backdate file.
8	If UPDATING data cartridge, type:		
	OP:DATA, CURRENT a!	OK	Copies new translations.
	OP:DATA,OLD a!	OK	Copies backdate file.
9	Type on the TTY:		
	RST:DEVICE:TDC a!	OK	a = TDC number 0 or 1. TDC restored to service.

TABLE AY

DATA CARTRIDGE INSERTION - No. 2B ESS

STEP	PROCEDURE	RESPONSE	REMARKS
1	At the TDC observe the TDC POWER lamps.	TDC POWER lamps must be lighted.	
2	At the SSP observe the TDC LED.	TDC LED must be lighted.	TDC POWER and TDC LED must be lighted before inserting data cartridge.
3	At the TDC: Insert the data cartridge into cartridge tape transport (CTT).		Data cartridge must have the same issue as the generic cartridge.
4	Type on the TTY: INIT:TAPE!	 Tape will move. COMPL	 TDC initialized.
5	Repeat Step 4 four times if tape was previously inactive.		Restores proper tape tension.
6	Type on the TTY: DGN:TDC a, TST b;c!	 DGN:TAPE ATP	 a = TDC number 0 or 1 b = test number c = action option (blank, RPT, or STEP). ATP = all tests passed. Diagnostics performed successfully.
	ALW:TAPEUTIL!	COMPL ATI LED on SSP lighted.	Activates utilities.
	AUDIT:TAPE(a,b), TRKc;CORR!	AUDIT TAPE MATCH 0 TAPEUTIL STOPPED	a = TDC file copied from b = TDC file to be audited or updated c = track number where audit is to start.

TABLE AZ

DATA CARTRIDGE INSERTION - No. 3 ESS

STEP	PROCEDURE	RESPONSE	REMARKS
1	At the TDC observe the TDC POWER lamps.	TDC POWER lamps must be lighted.	
2	At the SSP observe the TDC LED.	TDC LED must be lighted.	TDC POWER and TDC LED must be lighted before inserting data cartridge.
3	At the TDC: Insert the data cartridge into cartridge tape transport (CTT).		Data cartridge must have the same issue as the generic cartridge.
4	Type on the TTY: INIT:TAPE!	Tape will move. COMPL	TDC initialized.
5	Repeat Step 4 four times if tape was previously inactive.		Restores proper tape tension.
6	Type on the TTY: DGN:TAPE A, TST b;c!		a = TDC number 0 or 1 b = test number c = action option (blank, RPT, or STEP).
		ATP	ATP = all tests passed. Diagnostics performed successfully.
	ALW:TAPEUTIL!	COMPL	Activates utilities.
	AUDIT:TAPE(a,b),TRKc;CORR!	AUDIT TAPE MATCH 0 TAPEUTIL STOPPED	a = TDC file copied from b = TDC file to be audited or updated c = track number where audit is to start.

TABLE BA

DATA CARTRIDGE REMOVAL - EOS

STEP	PROCEDURE	RESPONSE	REMARKS
1	Observe SSP lamps.	ATI, MAS, MISC MAN FORCED lamps are extinguished.	
2	Type on the TTY: RMV:DEVICE:TDC a!	OK	a = TDC number 0 or 1. TDC removed from service.
	Observe if tape moves.	TDC LED lighted on SSP.	
	If tape does not move go to Step 4.		
3	If tape moved while Step 2 message was typed, type on the TTY:		
	INIT:DEVICE:TDC a!	COMPL	
4	At cartridge tape transport (CTT):		
	Depress REW key.	Tape rewinds and moves forward to beginning of tape (BOT) mark and moves forward to load point.	
5	Depress UNLD key.	Tape rewinds to BOT mark and stops.	
6	Remove data cartridge.		

TABLE BB

DATA CARTRIDGE REMOVAL - NO. 2B AND NO. 3 ESS

STEP	PROCEDURE	RESPONSE	REMARKS
1	Observe SSP lamps.	ATI, MAS, MISC MAN FORCED lamps are extinguished.	
2	Type on the TTY: RMV:TAPE a!	OK	a = TDC number 0 or 1. TDC removed from service.
	Observe if tape moves.	TDC LED lighted on SSP.	
	If tape does not move go to Step 4.		
3	If tape moved while Step 2 message was typed, type on the TTY:		
	INIT:TAPE a!	COMPL	
4	At cartridge tape transport (CTT):		
	Depress REW key.	Tape rewinds and moves forward to beginning of tape (BOT) mark and moves forward to load point.	
5	Depress UNLD key.	Tape rewinds to BOT mark and stops.	
6	Remove data cartridge.		

TABLE BC

GENERIC PROGRAM RESTARTS—EOS

STEP	PROCEDURE	RESPONSE	REMARKS
1	Observe TDC 0, when tape is not moving, type on the TTY:		
	RMV:DEVICE:TDC 0!	OK	Removes TDC 0 from service.
2	At the tape transport:		
	Depress REW key	Tape rewinds and moves forward to beginning of tape (BOT) mark and moves forward to load position.	
	Depress UNLD key.	Tape rewinds to BOT mark and stops.	
3	Remove data cartridge from TDC 0.		Prior to inserting data cartridge, TDC POWER lamp must be lighted and the TDC LED on the SSP must be lighted.
4	Insert new generic cartridge in TDC 0.		
5	Type on the TTY:		
	INIT:DEVICE TDC 0!	Tape moves.	
		COMPL	TDC 0 initialized.
6	Repeat Step 5 four times.		Restores tape tension.

TABLE BC (Contd)

GENERIC PROGRAM RESTARTS—EOS

STEP	PROCEDURE	RESPONSE	REMARKS
7	Type on the TTY:		
	OP:DATA,CURRENT 0, ALL!	OK	Writes translation file on TDC 0 tape.
	OP:DATA,OLD 0!	OK	Writes backdate file on tape.
	LOD:OMAS:TAPE 0!	OK	Loads generic and translations files into off-line store.
8	Type on the TTY:		
	SW:CU:UCL!		Off-line store now on-line.
9	Remove cartridge from TDC 1.		
10	Insert new cartridge into TDC 1.		
11	Type on the TTY:		
	INIT:DEVICE:TDC 1!	Tape moves.	
		COMPL	TDC 1 initialized.
12	Repeat Step 11 four times.		Restores tape tension.
13	Type on the TTY:		
	OP:DATA CURRENT 1, ALL!	OK	Writes translation file on TDC 1 tape.
	OP:DATA,OLD 1!	OK	Writes backdate file on tape.
	LOD:OMAS:TAPE 1!	OK	Loads generic and translation files into off-line store.
14	Type on the TTY:		
	SW:CU!		Switches control units.

TABLE BD
DATA CARTRIDGE REFERENCE DOCUMENTS

DOCUMENT	SUBJECT
IM-2H200-04	Input Message Manual, No. 2B Electronic Switching System (ESS)
OM-2H200-04	Output Message Manual, No. 2B Electronic Switching System (ESS)
IM-3H300-01	Input Message Manual, No.3 Electronic Switching System (ESS)
OM-3H300-01	Output Message Manual, No. 3 Electronic Switching System (ESS)
IM-4C001-01	Input Message Manual (EOS) for the Extended Operating System
OM-4C001-01	Output Message Manual (EOS) for the Extended Operating System
TLM-1C900-01	Common Systems Processor Trouble Locating Manual
TLM-4C706-01	Tape Data Cartridge TLM (CTAPM)
232-100-100	No. 2B Electronic Switching System (ESS)
233-000-003	No. 3 Electronic Switching System (ESS)
254-340-001	3A Processor Extended Operating System
254-300-170	Tape Data Controller, Description and Theory - Common Systems
254-300-180	System Status Panel, SSP Controller, and SSP Panel Relay Unit, Description and Theory of Operation - Common Systems
254-300-190	Teletypewriter and Teletypewriter Controller, Description and Theory of Operation
TLM 4C706-01	Trouble Locating Manual - Tape Data Cartridge

Y. 3A CC Diagnostic Test Sequence

2.68 Table BE shows the 3A CC general diagnostic command formats, test sequencing, and diagnostic test programs pertaining to the tests.

TABLE BE

3A CC DIAGNOSTIC TEST SEQUENCE

TEST PROGRAM	TEST NUMBER	DESCRIPTION
CDGMCH (PR-1C912)	1	MCH—Maintenance Channel
	2	BUS—Gating Bus
	3	CLOCK—System Clock
	4	INITIAL—Verification of Initialization by Monitor
CDGTO (PR-1C913)	5	TO—"TO" Decoder
	6	FROM—"FROM" Decoder
CDGMLT (PR-1C914)	7	MULFRXP—Test for Multiple Firing "FROM" Crosspoints
	8	MULTOXP—Test for Multiple Firing "TO" Crosspoints
CDGREG (PR-1C915)	9	GATEGEN—General Registers
	10	GATESP—Special Registers
CDGMIC (PR-1C916)	11	MICMEM—Micromemory
CDGFN (PR-1C917)	12	LOADFR—Function Register
	13	ADDER—Add Function
	14	DMLCMP—Matcher for Duplicate DML
	15	BOOLEAN—Boolean Logic Functions
	16	FLZ—Find Low Zero Function
	17	ROTATE—Rotate Function
	18	PACK—Pack and Unpack Gating Operation and DML Parity Generator
CDGMC1 (PR-1C919)	19	MICSEQ—Microcontrol Part 1
	20	MICSEQ2—Microcontrol Part 2
	21	MICSEQ3—Microcontrol Part 3
	22	MICSEQ4—Microcontrol Part 4
CDSPA1 (PR-1C920)	23	DSFLOP—DS Flip-Flop
	24	PAPLUS1—Address Increment Adder
CDGMSQ (PR-1C921)	25	MAINSEQ—Store Bus Controller Part 1
	26	MNSEQ2—Store Bus Controller Part 2
CDGSIO (PR-1C922)	27	STI01—Unlock and Test On-Line CC I/O Access to Off-Line Store
	28	STI02—Store Controllers I/O Order Decoder
CDGSMX (PR-1C923)	29	STMX1—One Half of Store Controller Multiplex Circuits
	30	STMX2—Other Half of Store Controller Multiplex Circuits
	31	STMX3—One Half of Store Controller Check Circuits
	32	STMX4—Other Half of Store Controller Check Circuits
CDGSBS (PR-1C924)	33	STBS1—Store Command Portion of Store Bus
	34	STBS2—Store Address Portion of Store Bus
	35	STBS3—Store Data Portion of Store Bus
	36	STBS4—Store Data Portion of Store Bus

TABLE BE (Contd)

3A CC DIAGNOSTIC TEST SEQUENCE

TEST PROGRAM	TEST NUMBER	DESCRIPTION
CDGSCP (PR-1C934)	37	STCP1—Bus Control Circuitry
	38	STCP2—Data Parity Control Circuitry
	39	STCP3—Data Parity Control Circuitry
	40	STCP4—Data Parity Check Circuitry
CDGSFA (PR-1C925)	41	STFB1—Refresh Select Signals to Fanout Boards
	42	STFB2—Normal Select Signals to Fanout Boards
	43	STFB3—Store Address Signals Through Fanout Boards
	44	STFB4—Store Address Signals Through Fanout Boards
CDGSFB (PR-1C926)	45	STFB5—Fanout Board Address Parity Checkers
	46	STFB6—Fanout Board Address Parity Checkers
	47	STFB7—Store Timing Signals Through Fanout Boards
	48	STFB8—Store Timing Signals Through Fanout Boards
CDGSWP (PR-1C927)	49	STWP1—Write Protect Reads and Writes
	50	STWP2—Write Protect Reads and Writes
	51	STWP3—Write Protect Check Circuits
CDGSON (PR-1C928)	52	STON1—Store Bus From On-Line CC to Off-Line CC
CDGSDF (PR-1C935)	53	STDF1—Data Register To/From Memory Modules
	54	STDF2—Data Register To/From Memory Modules
	55	STDF3—Data Register To/From Memory Modules
	56	STDF4—Data Register To/From Memory Modules
CDGSD (PR-1C929)	57	STDT1—Memory Module 0
	58	STDT2—Memory Module 1
	59	STDT3—Memory Module 2
	60	STDT4—Memory Module 3
	61	STDT5—Memory Module 4
	62	STDT6—Memory Module 5
	63	STDT7—Memory Module 6
	64	STFT8—Memory Module 7

TABLE BE (Contd)

3A CC DIAGNOSTIC TEST SEQUENCE

TEST PROGRAM	TEST NUMBER	DESCRIPTION
CDGMI (PR-1C930)	65	MINTERP—Microinterpret Operation
	66	MTMSCXP—Test for Multiple Firing Miscellaneous Crosspoints
	67	DMLPR—DML Parity Generator
	68	BUSPAR—Bus Parity Check
	69	POXYPAR—IB Register X- and Y-Field Parity Generator and Parity Checker
CDGNTI (PR-1C931)	70	TIMERS—Program Timer, Timing Counter
	71	INTRUPT—Interrupts
	72	ADMTCH—Panel Address Matcher
	73	DTMTCH—Panel Data Matcher
	74	IO—I/O Channels
CSTATS (PR-1C932)	75	STATUS—Status Bits, Initialization
	76	STATUS2—Status Bits, Time-Outs
	77	DGSSP—System Status Panel
CDGDSR (PR-1C911)	78	DSRDG—Double Store Read
Spare	79	
TWOMIC (PR-2H351)	80	2B Microstore Content (No. 2B ESS Only)
MODEDEC (PR-2H350)	81	2B I/O Channel Select (No. 2B ESS Only)
REGCHEK (PR-2H350)	82	Register Access (No. 2B ESS Only)
RUNFF (PR-2H350)	83	2B I/O Run Flip-Flop (No. 2B ESS Only)
OLDRUNFF (PR-2H350)	84	2B I/O On-Line Access To Off-Line Run Flip-Flop (No. 2B ESS Only)
PULSGEN (PR-2H350)	85	2B I/O CPD Pulses (No. 2B ESS Only)
EAXPUA (PR-2H350)	86	2B I/O EA To PUA Translators (No. 2B ESS Only)
CPDTST (PR-2H350)	87	2B I/O CPD Crosspoint Translator and Output Current Control (No. 2B ESS Only)
DPTST (PR-2H350)	88	2B I/O Dial Pulse Timing (No. 2B ESS Only)
PWRMISC (PR-2H350)	89	2B I/O External Orders and Power Test (No. 2B ESS Only)
TRBLSHT (PR-2H350)	90	2B I/O Failing Order Sequences. This is not a test but a utility debugging aid.

3. INPUT/OUTPUT

A. Physical Layout

3.01 Figures 12 through 15 depict the primary I/O hardware elements.

B. Remote Serial Interface (RSI)

Verification

3.02 Table BF describes the sequence of tests to be run to verify proper operation of the RSI.

Diagnostics

3.03 See Table BG for diagnostic request formats.

3.04 Table BH is a list of the various RSI diagnostic test numbers and what they do.

References

3.05 Table BI is a list of references that can aid in the maintenance of the RSI.

TABLE BF

RSI VERIFICATION PROCEDURE

STEP	PROCEDURE	RESPONSE	REMARKS
1	RMV:DEVICE:RSI n!*	OK IP tt DEVICE REPT RSI n STATE MAN x1 x2 x3 x4	RSI n removed from service.
2	DGN:RSI n!	tt DGN RSI N ATP	RSI n tested successfully
3	SW:CU!	OK tt SW CU COMPL x (x = newly on-line CU number)	Switch to other CU.
4	DGN:RSI n!	tt DGN RSI n ATP	RSI n tested successfully
5	RST:DEVICE:RSI n!	IP tt DEVICE REPT RSI n STATE AVL x1 x2 x3 x4	Restore RSI to service.
6	Repeat steps 1-5 on all remaining RSI units equipped in the system using appropriate device unit numbers.		

* n = device unit number.

TABLE BG

DIAGNOSTIC REQUEST FORMATS

DIAGNOSTIC	TEST PERFORMED
DGN:DEVICE UNIT! (Note 1)	Prints out first failure encountered and aborts test.
DGN:DEVICE UNIT:UCL!	Runs all tests and prints out all failures encountered.
DGN:DEVICE UNIT;n! (Note 2)	Runs test specified by n and prints out a pass/fail indication.
DGN:DEVICE UNIT;RPT:n! (Note 2)	Runs test specified by n repetitively until aborted by an input message. A pass/fail printout is generated after the first run. Thereafter, a printout is generated only if the test results change. The test status is also maintained on the PASS/FAIL lamps of the System Status Panel (SSP).
DGN:DEVICE UNIT;STEP:n! (Note 2)	Runs test specified by n and prints out a pass/fail message. Thereafter, the test is run only when the EXECUTE button on the SSP is depressed. A new test pass/fail message will be printed out only if the test results have changed from the previous results. The test status is also maintained on the PASS/FAIL lamps of the SSP. This diagnostic mode will continue until aborted by an input message.
ABT:PDGN!	This message will abort the RPT and STEP diagnostic modes.
DGN:CU;ADD:n,xxx!	Runs test n on memory not defined by the system; used to test growth memory; xxx defines highest address of memory to be tested (used by 3A CC only).

Note 1: Default value of unit number "UNIT" is 0.

Note 2: See device sections for lists of test numbers (n = test number).

TABLE BH

RSI DIAGNOSTIC TEST NUMBERS
(DGNRSI PR-4C708)

TEST NO.	FUNCTION
01	This test verifies the serial channel used by the RSI.
02	This test sends an acknowledge (ACKII) command to the serial peripheral interface and checks for responses.
03	This test first sends all zeros and then all ones to the bus terminator (BT) and checks for proper responses.
04	This test sets the BT to all ones and then switches to all zeros, one bit at a time. The test is repeated by setting all zeros to ones a bit at a time and checking for proper response in each case.
05	This test checks the address decoders on the serial peripheral interface (SPI), the BT, and four RSI ports.
06	This test verifies communication with the RSI port. It also verifies the sanity of the PBI interface and basic command decoders.
07	This test exercises all the mode flip-flops of the RSI. It also verifies operation of the command decoders.
08	This test verifies the basic send and receive capabilities of the universal asynchronous receiver transmitter (UART).
09	This test checks the first-in/first-out (FIFO) and both sides of the UART by transmitting 256 unique characters at the maximum baud (information bits per second) rate.
10	This test is similar to test 09 except that all four electronic industry association (EIA) voltage level outputs are switched off and on as rapidly as possible during the conduct of the test.
11	This test checks the majority of the interrupt logic in the RSI port, with the exception of the EIA change interrupt circuits.
12	This test exercises a modulator/demodulator (MODEM) when the port is equipped. When the test is run it is assumed that the analog loopback test button on the MODEM has been depressed. The EIC detector is also tested.
13	This test verifies that the RSI port can run at the baud rate specified in the device control block (DVCB).
14	This test verifies that a character-ready-send (CRS) bit is returned during a write-data operation when the send buffer is not full.
15-19	Vacant.
20	This test verifies that a data set/MODEM with dial-up capability can respond to the switched telephone network.

TABLE BI

RSI REFERENCE DOCUMENTS

DOCUMENT	SUBJECT
254-340-080	Maintenance Overview, Extended Operating System, 3A Processor
254-340-088	Processor Diagnostics, Extended Operating System, 3A Processor
254-340-090	Peripheral Diagnostics, Extended Operating System, 3A Processor
IM/OM 4C001-01	Input/Output Message Manuals — EOS
TLM 4C708-01	Trouble Locating Manual — RSI
PR-4C708	Remote Serial Interface Diagnostic Program

C. Parallel Channel Interface (PCH)

Verification

3.06 Table BJ describes the sequence of tests to be run to verify the proper operation of the PCH.

Diagnostics

3.07 See Table BG for diagnostic request formats.

3.08 Table BK is a list of the various PCH diagnostic test numbers and what they do.

References

3.09 Table BL is a list of references that can aid in the maintenance of the PCH.

TABLE BJ

PCH VERIFICATION PROCEDURES

STEP	PROCEDURE	RESPONSE	REMARKS
1	DGN:PCH!	tt DGN PCH 0000 ATP tt UPD OMAS COMPL	Off-line PCH unit 0 tested successfully.
3	SW:CU!	ATP tt UPD OMAS COMPL OK tt SW CU COMPL x (x = newly on-line CU)	Switch to other CU.
4	DGN:PCH!	tt DGN PCH 0000 ATP tt UPD OMAS COMPL	Off-line PCH unit 0 tested successfully.
5	DGN:PCH 1!	tt DGN PCH 0001 ATP tt UPD OMAS COMPL	Off-line PCH unit 1 tested successfully.

TABLE BK

PCH DIAGNOSTIC TEST NUMBERS
(DGNPCH PR-4C705)

TEST NO.	FUNCTION
1	Test low-byte maintenance flag
2	Test high-byte maintenance flag
3	Test low-byte information (IFL) flag
4	Test high-byte information (IFH) flag
5	Test PCH enable (ENA) flag
6	Test PCHENA flag
7	Test address sent flag (AFO)
8	Test command sent flag (CFO)
9	Test INF signal loop-around register (low-byte)
10	Test INF signal loop-around register (high-byte)
11	Test INF parity low bit
12	Test INF parity high bit
13	Test AC bus driver and receiver (low-byte)
14	Test AC bus driver and receiver (high-byte)
15	Test AC bus driver and receiver parity low (PL) bit
16	Test AC bus driver and receiver parity high (PH) bit
17	Test multiple command check circuit
18	Test multiple SPCH check circuit
19	Test AC bus of SPCH
20	Test INF lead from AC bus
21	Test ACKI command lead from parallel bus
22	Test DBS init lead from parallel bus
23	Test interrupt lead from parallel bus

TABLE BL

PCH REFERENCE DOCUMENTS

DOCUMENT	SUBJECT
254-340-080	Maintenance Overview, Extended Operating System, 3A Processor
254-340-088	Processor Diagnostics, Extended Operating System, 3A Processor
254-340-090	Peripheral Diagnostics, Extended Operating System, 3A Processor
IM/OM 4C001-01	Input/Output Message Manuals — EOS
TLM 4C705	Trouble Locating Manual — PCH
PR-4C705	Parallel Channel Diagnostic Program

D. Direct Memory Access (DMA)

Verification

3.10 Table BM describes the sequence of tests to be run to verify proper operation of the DMA.

Diagnostics

3.11 See Table BG for diagnostic request formats.

3.12 Table BN is a list of the various DMA diagnostic test numbers and what they do.

References

3.13 Table BO is a list of references that can aid in the maintenance of the DMA.

TABLE BM

DMA VERIFICATION PROCEDURE

STEP	PROCEDURE	RESPONSE	REMARKS
1	DGN:DMA!	tt DGN DMA 0000 ATP tt UPD OMAS COMPL	Off-line DMA unit tested successfully.
2	SW:CU!	OK tt SW CU COMPL x (x = newly on-line CU)	Run diagnostics on mate DMA.
3	DGN:DMA!	tt DGN DMA 0000 ATP tt UPD OMAS COMPL	Off-line DMA unit tested successfully.

TABLE BN

DMA DIAGNOSTIC TEST NUMBERS
(DGDMA 4C-703)

TEST NO.	FUNCTION
1	Test interface to CU, internal bus, and register sequence
2	Test register loading
3	Test parity generator/checker
4	Test address comparator (present and final)
5	Test present address counter
6	Test address comparator (present and next)
7	Test DMA store bus
8	Test DMA store access
9	Dummy test
10	Test MPCH mode-enabling signals
11	Test low-byte maintenance flag
12	Test high-byte maintenance flag
13	Test low-byte information (IFL) sent flag
14	Test high-byte information (IFH) sent flag
15	Test PCH enable (ENA) flag
16	Test PCHENA flag
17	Test address sent flag (AFO)
18	Test command sent flag (CFO)
19	Test INF signal loop-around register (low-byte)
20	Test INF signal loop-around register (high-byte)
21	Test INF parity low bit
22	Test INF parity high bit
23	Test AC bus driver and receiver (low-byte)
24	Test AC bus driver and receiver (high-byte)
25	Test AC bus driver and receiver parity low (PL) bit
26	Test AC bus driver and receiver parity high (PH) bit
27	Test multiple command check circuit
28	Test multiple SPCH check circuit
29	Test AC bus of SPCH
30	Test INF lead from AC bus
31	Test ACKI command lead from parallel bus
32	Test DBS init lead from parallel bus
33	Test interrupt lead from parallel bus
34	Test DMA device communication ability while in regular DMA mode
35	Test priority encoding circuit
36	Test DMA data transfer sequence
37	Test maintenance mode, DBS mode, and data parity checker
38	Test on-line DMA capability to access off-line store

TABLE BO

DMA REFERENCE DOCUMENTS

DOCUMENT	SUBJECT
254-340-080	Maintenance Overview, Extended Operating System, 3A Processor
254-340-088	Processor Diagnostics, Extended Operating System, 3A Processor
254-340-090	Peripheral Diagnostics, Extended Operating System, 3A Processor
IM/OM 4C0001-01	Input/Output Message Manuals — EOS
TLM 4C702-01	Trouble Locating Manual — DMA
PR-4C703	DMA Diagnostic Program

E. CTI Unit

Verification

3.14 Table BP describes the sequence of tests to be run to verify proper operation of the CTI unit.

Diagnostics

3.15 See Table BG for diagnostic request formats.

3.16 Table BQ is a list of the various CTI unit diagnostic test numbers and what they do.

References

3.17 Table BR is a list of references that can aid in the maintenance of the CTI unit.

TABLE BP

CTI UNIT VERIFICATION PROCEDURE

STEP	PROCEDURE	RESPONSE	REMARKS
1	DGN:CTI!	tt DGN CTI 0000 ATP tt UPD OMAS COMPL	Test CTI unit
2	SW:CU!	OK tt SW CU COMPL x (x = newly on-line CU)	Switch to other CU
3	DGN:CTI!	tt DGN CTI 0000 ATP tt UPD OMAS COMPL	Test CTI unit

TABLE BQ

CTI UNIT DIAGNOSTIC TEST NUMBERS
(DGNCTI PR-4C704)

TEST NO.	FUNCTION
1	Perform a write/read transfer and check for stuck bits in the CSB.
2	Using loop-around, check for stuck at error, inability to reset, stuck at idle, stuck at clear, or stuck reset.
3	Using loop-around, check for stuck bits in the processor interface.
4	Test for stuck bits in the MCS register.

TABLE BR

CTI UNIT REFERENCE DOCUMENTS

DOCUMENT	SUBJECT
IM/OM 4C001-01	Input/Output Message Manuals — EOS
TLM 4C704-01	Trouble Locating Manual — CTI
PR-4C704	CTI Diagnostic Program

4. MAIN STORE (MAS)

A. Physical Layout

4.01 Figure 16 depicts the primary hardware elements of the MAS and Table BS provides typical designations and functions of the MAS bus leads.

B. MAS Verification Procedures

4.02 ***Equipment Specification:*** Either the 4K (Code JL2) or 16K (Code JL16) type MAS circuit packs must be correctly defined via the main store type word MASTYPE in OSTABS (for EOS Systems). In MASTYPE the low 4 bits are set to 1 for the 16K type and zero for the 4K type. Default is for the 4K type. CU diagnostic test 41 will fail if the circuit pack type in MASTYPE is incorrectly defined.

4.03 ***Main Store Audits:*** The main store audits are executed automatically as a low priority real-time function after each memory update is completed, regardless of how the update is initiated. Tables BT, BU, and BV provide information pertinent to MAS audit control, manual requests, and audit results.

C. MAS Utility Functions

4.04 ***Common MAS Utility Functions:*** The common system utility programs provide a means for dumping, loading, or monitoring main store word locations. The utility functions involved in reload, overwrite, and updating the MAS are described in Part 3.

4.05 Tables BW and BX give information relative to MAS utilities and MAS error recovery. Table BY is a list of MAS reference documents given for supplementary information.

TABLE BS

TYPICAL DESIGNATIONS AND FUNCTIONS OF THE MAIN STORE BUS LEADS

LEAD				FUNCTION
SC3	SC2	SC1	SC0	**Store Command Leads 0-3:** These leads are used by the 3A CC to issue a 2-out-of-4 command code to the memory. The assignments of the codes are:
1	1	0	0	**Read:** The contents of memory at the location defined on the address leads are returned on the data leads (also lock feature used to request exclusive use of SC0-SC3).
0	0	1	1	**Write:** The 16 data bits and 2 parity bits on the data leads are written in the store at the location defined on the address leads (also lock feature to request exclusive use of SC0-SC3).
1	0	0	1	**Load Write Protect:** This operation returns the contents of one write protect (WP) register in the store controller to the 3A CC.
0	1	1	0	**Store Write Protect:** This operation loads one of the WP registers in the store controller.
0	1	0	1	**Blind Write:** This operation is the same as the write command, but it writes data regardless of whether the location is write protected.
1	0	1	0	
SPARE				
SREQ				**Store Request Lead:** This signal is used by a lower priority 3A CC to request sole use of the MASB for a multiple cycle operation. This signal is necessary to prevent interwrite problems with multiple users on a MASB. It is not necessary for a higher priority user to inform the low priority user of a multiple cycle operation, since the high priority user has the ability to prevent a store access by a lower priority user.
SGO				**Store Go:** This signal is present on the bus to inform the store that a store operation has been requested. It is removed after the 3A CC has received the store complete (SCM) signal. In the case of a read operation, the address and command information is present on the bus. In the case of a write operation, the data, as well as the address and command information, is present on the bus.
SCM				**Store Complete Lead:** This signal is sent by the store to indicate that the read-out information is present on the bus for read operations. It is also sent on a write operation to indicate that the command, data, go, and address information may be removed from the bus.
SBY				**Store Busy Lead:** This signal is sent by the store to indicate that the store is busy processing a request.

TABLE BT

MAS AUDIT CONTROL

INPUT	SYSTEM RESPONSE(s)	REMARKS
INH:MASAU!		Temporarily inhibits MAS audits. Condition exists until next memory update or until an ALW:MASAU! input request.
ALW:MASAU!		Allows execution of an audit (AU:MAS!) when it has been inhibited by a TTY request or maintenance action.

TABLE BU

MAS MANUAL REQUESTS

INPUT	SYSTEM RESPONSE(s)	REMARKS
AU:MAS!	PF (List of faulty memory planes)	Requests Main Store audit of off-line CU. This request must be preceded by ALW:MASAU!.
AU:MAS;UCL!		Audit Main Store Unconditionally. Required when off-line processor is out-of-service. Off-line errors are not identified.

TABLE BV

MAS AUDIT RESULTS

INPUT	SYSTEM RESPONSE(s)	REMARKS
Manual	RCOVRY MAS ERR LIST: (Up to 8 faults listed.)	A list of recent MAS faults from MASLIST is listed. Provided on input of a request.
Manual	AU MAS COMPL	Main Store Audit Complete. One manual audit cycle has successfully completed. Message is not output when automatic audits are performed.
Auto/Manual	REPT MAS COMP	Reports a Main Store Word in complement-corrected form has been detected by the MAS audit. On an automatic audit the printing is suppressed after the first occurrence. All complement-corrected words may be found by initiating a manual audit (AU:-MAS!).
Auto/Manual	REPT MAS TRBL	Reports Main Store Trouble. The audit is unable to complement-correct a fault location in main store. This message is accompanied by a major alarm (IMMEDIATE ACTION REQUIRED). Subsequent audits will attempt to correct the fault location. If correction is made the message will change to REPT MAS COMP. In automatic audits the print suppression may block the display of the change. May appear during an off-line MAS update, indicating that update of the location was not performed.
Auto/Manual	REPT MAS MISMATCH	Report a logical difference between the on-line and off-line main store while in double store read mode. Disables double store read. Memory contents are not changed until next update. Attempt should be made to determine the correct side and shift the system there. Can indicate a double parity problem. Should use a manual audit or CU diagnostic to investigate the problem.

TABLE BV (Contd)

MAS AUDIT RESULTS

INPUT	SYSTEM RESPONSE(s)	REMARKS
DUMP:ST MASFLIST!	8 most recent MAS faults	The main store fault list format: Word 0 Bit 15 = CU number Bit 14-12 = Data Present (1s) Bits 11-4 = Bit No. of fault Bits 3-0 = Bits 19-16 MAS address Word 1 Bits 15-0 = MAS address bits

TABLE BW

MAS UTILITIES

INPUT	SYSTEM RESPONSE(s)	REMARKS
DUMP:ST aa,nn;ops!	Displays store data words starting at address aa, block length nn. Default length is 8 words.	ops = options ONC-On condition of data or address match. Need SET:MATCH first.
LOD:ST aa;ops:dd,mm!	Displays 8 consecutive store words starting from address aa. First word is changed by data dd using mask mm (if specified). After first printing will print only on changes. First word only is displayed on panel.	ops = options ONC-On condition of data or address match. Need SET:MATCH first. SGL-Execute only once RDT LAMPS-Display on panel
MON:ST aa ops!	Displays 8 consecutive store words starting from address aa. First word only is displayed on the panel.	ops = options Same as LOD:ST

TABLE BX

MAS ERROR RECOVERY

MESSAGE	SOURCE
RCOVRY MAS ERR CU address gooddata baddata bit MAS MOD PACK DIP A 99 response means that more than one bit is bad. See IM-OM.	This message indicates that the audit has successfully corrected a MAS error. Source of the correction is given in case: (blank) Corrected by off-line MAS data DSR Double Store Read COMP Complement Correction LIST From MAS fault list

TABLE BY

MAS REFERENCE DOCUMENTS

DOCUMENT	SUBJECT
254-340-014	Memory Organization, Extended Operating System, 3A Processor
254-340-080	Maintenance Overview, Extended Operating System, 3A Processor
254-340-088	Processor Diagnostics, Extended Operating System, 3A Processor
254-340-082	System Utilities, Extended Operating System, 3A Processor
IM/OM 4C001-01	Input/Output Message Manuals — EOS
TLM 1C900-01	Common Systems Trouble Locating Manual-Processor
PR-4C617	CBLM-Common Base Level Monitor
PR-4C623	CNRUTL-Common Nonresident Utilities
PR-4C621	CTSD-Common System Data Layout
PR-4C622	CUTIL-Common System Utility Programs
PR-4C611	MASACS-Mainstore Audit Program

TABLE BZ

EOS SSP KEY BUFFERS — BIT ASSIGNMENTS

BIT	KEY BUFFER	SSP FUNCTIONAL NAME	SSP FUNCTIONAL AREA
0	0	ENABLE*	System Emergency Manual Control (SEMC)
1		LOCK	Select SYC (or CU) 0 or 1
2		SELECT 0	SEMC
3		SELECT 1	SEMC
4		TTY INIT	SEMC
5		EXECUTE	TEST CONTROL
6		MEMORY RELOAD*	SEMC
7		Spare	SEMC
0	1	LOCK P	
1		FORCE	SEMC
2		FAIL	TEST CONTROL
3		PASS	TEST CONTROL
4		DISABLE REMOTE ACCESS	SEMC
5		ALT BUS	PANEL POWER
6		SERVICE LOSS	Status Lamp
7		INIT EXECUTE*	SEMC
0	2	CRITICAL	Status Lamp
1		PANEL TIME-OUT	Autonomous Timer
2		Spare	
3		Spare	
4		Spare	
5		MINOR	ALARMS (Audible Bell)
6		MAJOR	ALARMS (Audible Gong)
7		CRITICAL	ALARMS (Audible Gong)
0	3	EMER LINE TRFR	SEMC
1		Spare	
2		INHIBIT BUILDING ALARM	ALARM CONTROL
3		ALARM TRFR	ALARM CONTROL
4		ALARM RELEASE	ALARM CONTROL
5		STABLE CALLS*	SEMC
6		PAST OFFICE DATA*	SEMC
7		BACKDT OFFICE DATA*	SEMC

* Used for system initialization

TABLE CA

EOS SSP STATUS BUFFER — BIT ASSIGNMENTS

BIT	STATUS BUFFER	SSP NAME	FUNCTIONAL AREA
0	0	ACTIVE (SYC 0)	System Control
1		STANDBY (SYC 0)	
2		OUT OF SERVICE (SYC 0)	
3		UNAVAILABLE (SYC 0)	
4		ACTIVE (SYC 1)	
5		STANDBY (SYC 1)	
6		OUT OF SERVICE (SYC 1)	
7		UNAVAILABLE (SYC 1)	
0	1	Building Power	Major Equipment
1		SYC	
2		Spare (critical indicator)	
3		Peripheral A	
4		Peripheral B	
5		SERVICE LIMIT	
6		TRAFFIC LIMIT	
7		Spare	
0	2	Miscellaneous (MISC)	Major Equipment
1		Auto Message Accounting (AMA)	
2		Ringing & Tone Plant (RT)	
3		Peripheral Pulse Distr. (PPD)	
4		Scan Controller (SC)	
5		Network Controller (NWC)	
6		Control Unit (CU)	
7		FORCED	
0	3	SYSTEM NORMAL	Major Equipment
1		MAJOR EQUIPMENT LOSS	
2		ALARM CIRCUIT	
3		MAJOR POWER	
4		MINOR POWER	
5		MINOR	
6		MAJOR	
7		FUSE	
0	4	Building (BLDG)	Other
1		Dynamic Service Protect (DSP)	
2		Overload Announce (OVLD ANN)	
3		Spare (Nonresident Program Active)	
4		Tape Data Controller (TDC)	
5		TTY Controller (TTYC)	
6		Service Limit (SVC LIM)	
7		Trunk Limit (TRK LIM)	
7-0	5		Status Display, LED 7-0
7-0	6		Status Display, LED 15-8
7-0	7		Status Display, LED 23-16

TABLE CB

SYSTEM STATUS AND CONTROL

INDICATOR	CONDITIONS	NOTES
ALT BUS	Power applied via alternate bus	Occurs when momentary contact switch is held depressed or when the SSP detects a power failure and automatically switches to the alternate bus.
SYC 0 OR SYC 1		
LOCK	Program control of system controller and force functions is enabled	When LOCK key is depressed, the program sets the SYC associated with the on-line unit and then prevents switching to the off-line side.
ACTIVE	On-Line system controller (SYC 0 or SYC 1)	
STANDBY	Off-line SYC is available	SYC is capable of being switched on-line.
OUT OF SERVICE	Off-line SYC is not immediately available	SYC has an uncorrected failure, memory is being updated, the SYC is having an off-line unit diagnosed, or a unit is manually removed.
UNAVAILABLE	Off-line CU is unavailable because FORCE or LOCK key is depressed or power has been removed.	
ALARMS		
CRITICAL	PANEL TIME-OUT is lighted. Software recognition of a critical alarm condition	Extinguished when ALARM RELEASE key is depressed. Audible alarm sounds twice, 1/2 second apart. There is a 1-1/2 second interval before the pattern is repeated. A critical alarm is reported by maintenance software when it detects an equipment outage of critical importance to overall system operation, such as loss of a controller in both the on-line and off-line system controls.
MAJOR	Software recognition of a major alarm condition	Extinguished when ALARM RELEASE key is depressed. Audible alarm sounds at 1-1/2 second intervals. Reports partial loss of system capability.
MINOR	Software recognition of a minor alarm condition	Extinguished when ALARM RELEASE key is depressed. Audible alarm is a continuous tone.
MAJOR POWER	Scan point indicates a major power failure	Extinguished when scan points return to normal state. A major audible alarm sounds.
FUSE	Scan point indicates blown fuse	Extinguished when scan points return to normal state. Applicable MAJOR or MINOR lamp is lighted and major or minor audible alarm is sounded.

TABLE CB (Contd)

SYSTEM STATUS AND CONTROL

INDICATOR	CONDITIONS	NOTES
	ALARMS (Contd)	
ALARM CIRCUIT	Scan point indicates a power failure in alarm circuit	Extinguished when scan points return to normal state.
SERVICE LOSS	System initialization generated manually or by program control	Extinguished about three minutes later, provided no more system initializations occur during that time.
	ALARM CONTROL	
INHIBIT BUILDING ALARM	Audible building alarms not sounded. TTY messages not printed except for fire alarm	TTY messages indicate whether building alarms are allowed or inhibited.
	TEST CONTROL	
EXECUTE	Diagnostic test in progress	
PASS	Successful completion of diagnostic test sequence	
FAIL	Unsuccessful diagnostic test sequence	
	MISCELLANEOUS	
SYSTEM NORMAL	Extinguished when a PANEL TIMEOUT occurs, an SCC critical indicator becomes active (except for FORCED and BLDG INH), or certain SSP indicators are enabled.	Normal condition is illuminated.
PANEL TIME-OUT	Controlled by output of independent timer in SSP	The SSP timer must be reset every 2 seconds by program to prevent timeout from occurring. When indicator is lighted, the system is not functioning correctly, and is incapable of resetting the SSP timer.
ALARM RELEASE	Restoration of critical, major and minor alarms requested.	Extinguished when alarms are retired.
ALARM TRFR	Alarms and TTY messages are transferred to and displayed at SCC.	Critical, major, and minor alarms are retired after 5 seconds. Transfer is controlled by the panel key or by TTY input message.

TABLE CC

SYSTEM EMERGENCY MANUAL CONTROL — CONTROLS/INDICATORS

INDICATOR	CONDITIONS	NOTES
SYSTEM INITIALIZATION		
ENABLE	Permits manual control of system initialization.	Extinguished when the INIT EXECUTE key is depressed.
STABLE CALLS	Selection of an initialization which clears all stable and transient calls.	Extinguished by program control when initialization action is complete.
MEMORY RELOAD	Selection of an initialization which loads from tape into main memory a copy of the generic program and the first copy of office data.	All stable and transient calls are cleared. The first copy of office data is updated from memory after each sequence of recent changes. It will normally agree with the memory. Extinguished by program control when initialization action is complete.
PAST OFFICE DATA	Selection of an initialization which loads the more recent of the two backup files of office data from the memory backup tape into memory.	Lamp remains lighted after initialization to provide a visual reminder that information in memory may be out-of-date (recent changes made after the last tape update will not be included). Program informs any future "bootstrap" initialization to use the most recent file of office data instead of the normally used first copy. When MEMORY RELOAD and PAST OFFICE DATA keys are both depressed (in order) initialization loads the generic program as well as the most recent file of office data. All stable and transient calls are cleared. Extinguished by program control when the memory backup tape is updated.

TABLE CC (Contd)

SYSTEM EMERGENCY MANUAL CONTROL — CONTROLS/INDICATORS

INDICATOR	CONDITIONS	NOTES
	SYSTEM INITIALIZATION (Contd)	
BACKDT OFFICE DATA	Selection of an initialization which loads the older of the two backup files of office data from the memory backup tape into memory.	Lamp remains lighted after initialization to provide a visual reminder that information in memory is out-of-date. Program informs any future "bootstrap" initialization to use the older backup file for office data instead of the normally used most recent file. When both the MEMORY RELOAD and BACKDT OFFICE DATA keys are depressed, initialization loads the generic program as well as the oldest backup file of office data. All stable and transient calls are cleared. Extinguished by program control when the memory backup tape is updated. When both the PAST OFFICE DATA and BACKDT OFFICE DATA keys are depressed, they are released by program control.
INIT EXECUTE	System initialization is in progress.	ENABLE lamp is extinguished. A single initialization signal (MRF pulse) is sent to both control units (CUs). Program interrogates the state of the other SSP system initialization switches to determine initialization level.
TTY INIT	Initialization is in progress.	Depression of the key enables a program to initialize all TTY controllers and to clear all TTY buffers. Program extinguishes the lamp upon completion of its function.
	EMERGENCY ACTION	
EMER LINE TRFR	Operates a relay that provides contact closure to appropriate central office equipment.	Relay closure allows the manual transfer of important lines to an emergency switchboard upon failure of the No. 3 ESS.
DISABLE REMOTE ACCESS	SCC remote control of the SSP is disabled.	This does not affect the SCC monitoring of the SSP.

TABLE CC (Contd)

SYSTEM EMERGENCY MANUAL CONTROL — CONTROLS/INDICATORS

INDICATOR	CONDITIONS	NOTES
FORCE SYC ACTIVE		
SELECT 0	System controller 0 is to be forced on-line when FORCE key is depressed.	
SELECT 1	System controller 1 is to be forced on-line when FORCE key is depressed.	
FORCE	Forces the selected CU (and consequently the entire SYC) to the active state and the other CU to the unavailable state.	When the on-line SYC is selected, the system is prevented from switching. When the off-line SYC is selected, a switch is forced and the level of initialization occurs depending upon the SYSTEM INITIALIZATION keys depressed on the SYSTEM EMERGENCY MANUAL CONTROL panel on the SSP. When released, system is restored to normal software control.

TABLE CD

SSP REFERENCE DOCUMENTS

DOCUMENT	NUMBER	SUBJECT
BSP	254-300-180	System Status Panel
SD/CD	1C906-01	System Status Panel

TABLE CE

TDC CARTRIDGE REMOVAL PROCEDURE

STEP	PROCEDURE	RESPONSE	REMARKS
1	RMV:DEVICE:TDC x! (See Note)	OK (or) IP tt DEVICE REPT TDC x STATE MAN x1 x2 x3 x4	Remove TDC from Service.
2	If tape was moving when previous message was typed: INIT:DEVICE:TDC x! and repeat Step 1.	IP tt DEVICE REPT TDC x STATE AVL x1 x2 x3 x4	Initializes TDC x.
3	Depress REW button on the minirecorder.		Verify tape is rewinding.
4	When tape motion has stopped, depress UNLD button on minirecorder.		Tape is positioned for cartridge removal.
5	When tape motion has stopped, remove cartridge from unit.		DO NOT remove power from the TDC unit prior to removing the tape.

Note: x = TDC unit number.

TABLE CF

TDC CARTRIDGE INSERTION PROCEDURE

STEP	PROCEDURE	RESPONSE	REMARKS
1	If power was removed from the TDC: INIT:DEVICE:TDC x! (See Note)	IP tt DEVICE REPT TDC x STATE AVL x1 x2 x3 x4	Initializes TDC x.
2	Insert cartridge.		
3	RST:DEVICE:TDC x!	IP tt DEVICE REPT TDC x STATE AVL x1 x2 x3 x4	Restores TDC x to service.
4	ALW:TAPEUTIL!	PF tt ALW TAPEUTIL COMPL	Enables tape utilities.
5	EX:TDC!	PF tt TAPEUTIL COMPL	Retensions tape.
6	Perform Step 5 three times.		
7	INH:TAPEUTIL!	PF tt TAPEUTIL INH	Disables tape utilities.
8	DGN:TDC x!	IP tt DGN TDC x ATP	Tests TDC x.

Note: x = TDC unit number.

TABLE CG

TDC VERIFICATION PROCEDURE

STEP	PROCEDURE	RESPONSE	REMARKS
1	RST:DEVICE:TDC 0!	OK (or) IP tt DEVICE REPT TDC 0 STATE ALV xxxx xxxx xxxx xxxx	Places TDC 0 in service.
2	RST:DEVICE:TDC 1!	OK (or) IP tt DEVICE REPT TDC 1 STATE ALV xxxx xxxx xxxx xxxx	Places TDC 1 in service.
3	ALW:TAPEUTIL!	tt ALW TAPEUTIL COMPL	Enables tape utilities.
4	EX:TDC! (Repeat 3 times)	tt TAPEUTIL COMPL	Retensions tape.
5	INH:TAPEUTIL!	tt TAPEUTIL INH	Disables tape utilities.
6	DGN:TDC 0!	tt DGN TDC 0 ATP	Tests TDC 0.
7	DGN:TDC 1!	tt DGN TDC 1 ATP	Tests TDC 1.
8	SW:CU!	OK tt SW CU COMPL x (x= newly on-line CU)	Switches to other CU.
9	DGN:TDC 0!	tt DGN TDC 0 ATP	Tests TDC 0.
10	DGN:TDC 1!	tt DGN TDC 1 ATP	Tests TDC 1.

TABLE CH

TDC DIAGNOSTIC TEST NUMBERS (CTAPM PR-4C706)

TEST NO.	FUNCTION
01	This test verifies that bad parity in the serial sequence will be detected. An initialization of the entire device is then requested and verified. It sends an all 0s word and all 1s word and then checks that each is correctly returned. A series of 16 orders is sent to shift a 1 through a field of 0s. This verifies that data can be transferred through the interface to the bus terminator (BT) and returned.
02	This test initializes and sets the buffer states to known levels. It sends a load state order to the buffer. It then tests the capability of the 1024-bit shift registers to shift data accurately. The ready flag, clear flag, overflow conditions, and shift register bit count are all tested and verified.
03	This test is performed by issuing and verifying 15 of the 18 cartridge tape transport controller orders.
04	For this test the cartridge must be in place and write-enabled. A read-a-block command is issued for each track. Each block selected will require a backspace action in order to complete correctly. A continuous read command is issued for one track; when complete, the unit should return to the idle state.
05	This test verifies all non-read/write functions of the unit. Tests include fast forward, fast reverse, stop, beginning of tape (BOT), end of tape (EOT) sensors, and the backspace function.
06	This test requires that the other unit be in service. A block is read from the other unit, modified, and then written on the unit being tested. The test block is then read back and verified.

TABLE CI

CTT CONTROLLER COMMANDS AND FUNCTIONS

OCTAL	COMMAND	FUNCTION
00	TSTOP	This command stops the tape. If the read head is crossing a data block, the stop order will be issued at the next interblock gap (IBG).
01	TRWD	This command moves the tape in the reverse direction at 90 IPS until BOT is reached and then stops, starts, and proceeds forward at 30 IPS to Load Point and stops. This command performs the same function whether initiated by software or hardware. It also aborts any other operation.
02	TSCRC	This command causes 16 bits of the cyclic redundancy check character to be shifted from the check circuit to the BUF. After the CRC has been shifted, a fill on-line buffer command will be issued, and the CRC word will be adjusted to the beginning of the buffer, which will automatically switch off-line.
03	TWIB1-4	This command writes an interblock gap on the selected track. It is normally terminated by a tape stop command.
04	TSTAT	This command is issued when the status of the CTTC and tape is desired.
05	TFF1-4	This command starts the tape moving forward at 90 IPS. Data is ignored, but data detect bit 11 monitors the data blocks and may be used to count the number of blocks crossed on the selected track. This command is normaly terminated by a tape stop command.
06	TWSTP	This command enables the CTTC to stop a write operation at the end of the data coming from the current on-line shift register. The CTTC adds the postamble, creates a portion of the IBG, and then stops the transport. The track address is not affected by this command and write stop clears automatically following the sequence. The write stop command should only be used during a write operation.

TABLE CI (Contd)

CTT CONTROLLER COMMANDS AND FUNCTIONS

OCTAL	COMMAND	FUNCTION
07	TRB1-4	This command reads one block of data from a selected track. The transport will stop the read head in the IBG following the block being read. If the shift register beng filled by the CTTC is not full at the end of the data block, a fill on-line buffer command will be issued. This causes a right-adjust of the shift register so that it can be properly unloaded by the 3A CC. (Note: There is no indication that a fill operation has occurred, so the 3A CC has to know how much data was in that word, or an end-of-file word should be used.) A CRC check is done as data is transferred to the shift register. CRC status can be checked at the end of the operation by issuing a buffer status command and the status will be returned with the proper start code. Start code 011 indicates that the CRC check passes while start code 101 indicates that the check failed.
10	TMAINT	This command disables the CTT by deselecting it. In this mode, any command except rewind may be sent to the CTTC. RDY will be set to 0 (not ready). While in this mode, the reply from a rewind command will be STOP. (Note: In this mode, the read, write, and CRC circuits may be exercised. The CTTC may also be completely exercised.)
11	TRF1-4	This command moves the tape in the reverse direction at 90 IPS. Data is ignored, but data detect bit 11 monitors the data blocks and may be used to count the number of blocks crossed on the selected track. (Note: This operation is normally terminated by a tape stop command.)
12	TCWS	This command resets the write stop flag and is generally used only in a maintenance situation to cancel a tape write stop command.

TABLE CI (Contd)

CTT CONTROLLER COMMANDS AND FUNCTIONS

OCTAL	COMMAND	FUNCTION
13	TWT1-4	This command initiates the writing of one block of data on a selected track. This data is phase-encoded and is taken from the BUF registers. The CTTC generates and adds a preamble and postamble to the data block. The preamble and postamble are deleted during a read operation. The end of data to be written is indicated by issuing a tape write stop command to the CTTC. This command causes a postamble to be generated and written on the tape following the end of data from the on-line shift register. It will also cause the transport to stop after writing a portion of the IBG. The write command initiates a read-after-write sequence within the CTTC during which the data being read back from the tape is compared to what is being written on the tape by the CRC circuit.
14	TCCRC	This command clears the CRC register. This command is functional only while in the maintenance mode.
15	TBS1-4	This command moves the tape in the reverse direction at 30 IPS across one data block on any track to an IBG. If the read head is sitting on a data block (ie, after a fast-forward operation) when the command is issued, the tape will move in the reverse direction at 30 IPS to the preceding IBG.
16	TCMTC	This command clears or resets the maintenance and maintenance stop modes. (Note: This command should not be issued unless the CTTC is in the stop mode.)
17	TRT1-4	This command initiates a continuous read operation from a preselected track until a stop command is issued. A CRC check is done as the data is transferred to the shift registers. A CRC error status may be checked during any IBG after a time lapse of 200 microseconds into the IBG. By issuing a CTTC secondary status command, the CTTC secondary status reply will be returned with the proper start code. Start code 011 indicates that the CRC check passed, and start 101 indicates that the CRC check failed during the previous data block read.

TABLE CI (Contd)

CTT CONTROLLER COMMANDS AND FUNCTIONS

OCTAL	COMMAND	FUNCTION
00	TMSTOP	This command functions as follows: (a) Completely disables the transport (b) Stops any operation in progress (c) Motion commands are not accepted by the transport (d) Transpot is deselected (e) RDY is set to 0 (not ready) (f) CTT circuit goes into the maintenance state. (Note: This command may be cleared by issuing the general INIT command to the SPI, the tape reset maintenance command, or the tape transport initialize command.)
16	TINIT	This command clears all internal flags, then a rewind operation is initiated.

TABLE CJ TO BE PROVIDED

6. PROGRAMMABLE MAGNETIC TAPE SYSTEM

A. Physical Layout

6.01 Figures 28 through 30 depict the primary hardware elements of the Programmable Magnetic Tape System (PROMATS).

B. Verification and Diagnostics

6.02 Table CK describes the sequence of tests to be run to verify proper operation of the PROMATS.

6.03 See Table BG for diagnostic request formats.

6.04 Table CL is a list of the various PROMATS diagnostic test numbers and what they do.

References

6.05 Table CM is a list of references that can aid in the maintenance of the PROMATS.

TABLE CK

PROMATS VERIFICATION PROCEDURE

STEP	PROCEDURE	RESPONSE	REMARKS
1	RMV:DEVICE:PROMATS n!	OK (or) IP	Place PROMATS n out of service to allow diagnostics to run.
2	DGN:PROMATS n!	tt DEVICE REPT PROMATS n STATE MAN xxxx xxxx xxxx xxxx tt DGN PROMATS 0000	
		ATP	PROMATS n tested successfully.
3	SW:CU!	OK	Prepare to run diagnostics from mate CC.
4	DGN:PROMATS n!	tt SW CU COMPL x (x = newly on-line CU number) tt DGN PROMATS 0000	
		ATP	PROMATS n tested successfully.
5	RST:DEVICE:PROMATS n!	IP tt DEVICE REPT PROMATS n STATE AVL xxxx xxxx xxxx xxxx	Restore PROMATS n to service.
6	Repeat Steps 1-5 for all remaining PROMATS equipped in the office using appropriate device numbers.		

TABLE CL

PROMATS DIAGNOSTIC TEST NUMBERS
(DGNPRO PR-4C707)

TEST NO.	FUNCTION
01	Tests interfacing channels including DBS, parallel subchannel (SPCH), direct memory access (DMA), and main parallel channel between PROMATS and the 3A CC. The interrupt and DMA request (DMAR) paths are included.
02	Tests initialization by placing a command present (CP) signal on the parallel bus interface and checking for required responses, eg, SYNC, ER, and BUSY from the bus interface unit (BIU).
03	Tests all interface signals again, the address portion of status word 0 (SW0), and the BIU address decoder by a series of send status (SST) commands to verify that PROMATS can recognize the proper address and can respond to the CP and SST commands.
04	Tests the information (INF) leads between the PROMATS BIU and the DBS. The BIU data registers are then tested.
05	Switches the DMA request off and on and then uses the DBS maintenance status word to perform a direct check.
06	Uses a BIU loop-around to test INF leads. The leads are first cleared, then all leads are set to "1" one at a time. The leads are then set to "0" one at a time. Checks for crossed leads.
07	Tests channel and BIU for sensitivity to noise and bit drops by looping around different bit patterns.
08	This test sends an emergency stop (ESTP) command and verifies that the CONFORM program is sane enough to respond by returning the command complete (CMDC) signal.
09	This test sends an INIT command to PROMATS and verifies all return responses.
10	This test verifies the interrupt system by first disabling it and verifying that no interrupts are received. The system is then enabled and verifies that an interrupt can be recognized.
11	This test verifies the capability to access status words 1, 2, and 3, which are normally invisible in CONFORM. The test verifies portions of the microcode, internal bus bits, and several gates and flip-flops.

TABLE CL (Contd)

PROMATS DIAGNOSTIC TEST NUMBERS
(DGNPRO PR-4C707)

TEST NO.	FUNCTION
12	This test exercises the built-in microcode diagnostic sequences (maintenance steps).
13	This test performs a direct tape command by writing a string of zeros (ID burst) onto tape and verifying the results.
14	This test confirms the write command by writing data, consisting of 256 words, onto tape. This provides an actual test of a DMA data transfer to PROMATS.
15	This test verifies the backspace command by backspacing of the data entered in test 14. No data is transferred.
16	This test verifies the read forward command. The test reads the data written in test 14 and backspaced in test 15 and compares the data array with that written in test 14.
17	This test performs a statistical read/write check of the tape by writing, then reading back 50 test blocks of 256 words per block.
18	This test checks the command repertoire and timeout detection. It sends a series of commands: read, fast forward, emergency stop, rewind, preempt, and verifies beginning of tape (BOT) markers.
19	This test writes an ID burst to isolate read system errors. The test is run only when an earlier test indicates read system errors.
20	This test is a continuation of test 19 to isolate read system errors indicated from other tests. This test can, if necessary, direct the replacement of every circuit pack in every group of the read system.

TABLE CM

PROMATS REFERENCE DOCUMENTS

DOCUMENT	SUBJECT
254-340-080	Maintenance Overview, Extended Operating System, 3A Processor
254-340-088	Processor Diagnostics, Extended Operating System, 3A Processor
254-340-090	Peripheral Diagnostics, Extended Operating System, 3A Processor
IM/OM 4C001-01	Input/Output Message Manuals - EOS
TLM 4C707-01	Trouble Locating Manual - PROMATS
PR-4C707	Programmed Magnetic Tape System Diagnostic Program

7. TELETYPEWRITER AND TELETYPEWRITER CONTROLLER VERIFICATION

A. Physical Layout

7.01 Figure 31 through 33 depict the primary hardware elements of the teletypewriter (TTY) and the teletypewiter controller (TTYC).

B. TTY and TTYC Verification and Diagnostics

7.02 Table CN contains the procedure for verifying the proper operation of the TTYC. To execute the verification procedure, the system should be in a base level loop. Before proceeding with the test, do the following:

(a) Verify that power is applied to the TTYC(s) and associated TTY(s).

(b) Verify that all TTYCs equipped with AR17 packs have a TTY connected to the associated ports. If not, unseat the AR17 packs.

Diagnostics

7.03 The diagnostics for testing the TTYCs are defined in Table CO.

References

7.04 Table CP contains a list of documents that will be helpful in troubleshooting the TTYs and TTYCs. Table CQ lists TTY responses.

Conversion Tables

7.05 Tables CR through CU are provided as aids in troubleshooting 3A Processors.

TABLE CN

TTY AND TTYC VERIFICATION

STEP	PROCEDURE OR TYPE-IN	SYSTEM RESPONSE	REMARKS
1	RMV:DEVICE:TTYC a! (a = TTYC number 1-7)	OK (or) IP tt DEVICE REPT TTYC a STATE MAN x1 x2 x3 x4	Remove TTYC a from service. (Note: TTYC 0 is the maintenance TTY Controller and must not be removed from service. Therefore, it cannot be tested using these procedures.)
2	DGN:TTYC a!	PF tt DGN TTYC a ATP	TTYC a tested successfully.
3	SW:CU !	OK tt SW CU COMPL x (x = newly on-line CU number)	Prepare to run diagnostics from mate CC.
4	DGN:TTYC a!	PF tt DGN TTYC a ATP	TTYC a tested successfully.
5	RST:DEVICE:TTYC a!	IP tt DEVICE REPT TTYC a STATE AVL x1 x2 x3 x4	Restore TTYC a to service.
6	Repeat Steps 1-5 on all remaining TTY Controllers equipped in the system using appropriate controller number(s).		

TABLE CN (Contd)

TTY AND TTYC VERIFICATION

STEP	PROCEDURE OR TYPE-IN	SYSTEM RESPONSE	REMARKS
7	SET:CLK:TIME(hh,mm,ss), DATE(mo,dd,yy)!	OK	Substitute numbers for lower case letters for current time and date. hh = hour (00-23) mm = minute (00-59) ss = second (00-59) mo = month (1-12) dd = day (1-31) yy = year (00-99)
8	(a) OP:POSTMORT!	tt OP POSTMORT aal (message begins)	
	(b) Before printout stops, depress TTY INIT key on SSP for one second and release it.	tt DEVICE ON LINE (This message will be printed on each equipped TTY including the maintenance TTY)	POSTMORT printout stops.

TABLE CO

TTYC DIAGNOSTIC TEST SEQUENCE

TEST PROGRAM	TEST NUMBER	DESCRIPTION
DGNTC (PR-4C709)	1	TIME_TST--Tests the communication channel interface, timing accuracy of the clock and sequencers, TTYC state transition, and TTYC loop-around capability.
	2	STAT_TST--Confirms that port status alarm status can be altered, and that "Who Are You" (WRU) circuitry is operative.
	3	PAR_TST--Confirms the capability of the controller to recompute the parity on TTY messages, from odd to even.

TABLE CP

TTY and TTYC REFERENCE DOCUMENTS

DOCUMENT	SUBJECT
IM-4C001-01	Input Message Manual for Extended Operating System
OM-4C001-01	Output Message Manual for Extended Operating System
TLM-4C709-01	Teletypewriter Controller TLM
254-300-190	Teletypewriter and Teletypewriter Controller, Description and Theory of Operation, Common Systems
254-340-090	Peripheral Diagnostics, Extended Operating System, 3A Processor

TABLE CQ

TTY RESPONSES

RESPONSE	DESCRIPTION
FIRST RESPONSE TO INPUT MESSAGES	
?A	Error In Action Field
?C	Wrong TTY Channel
?D	Error In Data Field
?E	Inconsistency In Format
?F	Format Error
?I	Error In Identification Field
?O	TTY Channel Out-of-Service (Hit Break Key)
?P	TTY Parity Error
?T	Timeout
?X	Channel In Paper Tape Mode
??	System Reinitialized During Message
#	TTY Buffer Is Currently Full
IP	In Progress
NA	No Acknowledgement, Control of Message Has Been Lost and Correct Acknowledgement Is Not Possible
NB	The Entire 2B Buffer Is Full
NG	No Good
OK	Message Accepted and Acted Upon
PF	Printout Follows
RL	Repeat Later

TABLE CQ (Contd)

TTY RESPONSES

RESPONSE	DESCRIPTION
OUTPUT MESSAGE-PRIORITY FIELD	
*C	Critical Alarm-Immediate Action Required
**	Major Alarm-Immediate Action Required
*	Minor Alarm-Action Required
M	Message Is Result of Manual Action
A	Message Is Result of Action Taken By The System Automatically

TABLE CR

BINARY/DECIMAL CONVERSION TABLE

BIT POSITION	VALUE
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1 024
11	2 048
12	4 096
13	8 192
14	16 384
15	32 768
16	65 536
17	131 072
18	262 144
19	524 288
20	1 048 576

EXAMPLES:

BINARY - DECIMAL EXAMPLE: 0010110 = 0+0+16+0+4+2+0 = 22

DECIMAL - BINARY EXAMPLE: decimal 642 =

"VALUE" nearest equivalent to 642 but not larger ----> 642 − 512 = 130 Equivalent "BIT POSITION" = 9

"VALUE" nearest equivalent to 130 but not larger ----> 130 − 128 = 2 Equivalent "BIT POSITION" = 7

2 Equivalent "BIT POSITION" = 1

1010000010

Bit position 9 contains 1
Bit position 7 contains 1
Bit position 1 contains 1

TABLE CS

OCTAL/DECIMAL CONVERSION TABLE

DIGIT OCTAL VALUE	DIGIT POSITION						
	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
1	262144	32768	4096	512	64	8	1
2	524288	65536	8192	1024	128	16	2
3	786432	98304	12288	1536	192	24	3
4	1048576	131072	16384	2048	256	32	4
5	1310720	163840	20480	2560	320	40	5
6	1572864	196608	24576	3072	384	48	6
7	1835008	229376	28672	3584	448	56	7

EXAMPLES:

OCTAL - DECIMAL EXAMPLE:

0046721 = 0 + 0 + 16,384 + 3,072 + 448 + 16 + 1 = 19,921

DECIMAL - OCTAL EXAMPLE:

35,128 =

		35128
Decimal no. from table nearest equivalent to 35128 but not greater	---->	−32768
		2360
		2360
Decimal no. from table nearest equivalent to 2360 but not greater	---->	−2048
		312
		312
Decimal no. from table nearest equivalent to 312 but not greater	---->	−256
		56

	DIGIT POSITION FROM TABLE	DIGIT OCTAL VALUE FROM TABLE	OCTAL NO.
			0104470
32768	5	1	
2048	3	4	
256	2	4	
56	1	7	

TABLE CT

HEXADECIMAL/DECIMAL CONVERSION TABLE

DIGIT HEX VALUE	DIGIT POSITION				
	4	3	2	1	0
0	0	0	0	0	0
1	65536	4096	256	16	1
2	131072	8192	512	32	2
3	196608	12288	768	48	3
4	262144	16384	1024	64	4
5	327680	20480	1280	80	5
6	393216	24576	1536	96	6
7	458752	28672	1792	112	7
8	524288	32678	2048	128	8
9	589824	36864	2304	144	9
A	655360	40960	2560	160	10
B	720896	45056	2816	176	11
C	786432	49152	3072	192	12
D	851968	53248	3328	208	13
E	917504	57344	3584	224	14
F	983040	61440	3840	240	15

EXAMPLES:

HEX - DECIMAL EXAMPLE:

003A8 = 768 + 160 + 8 = 936

EXAMPLES: (Contd on following page)

TABLE CT (Contd)

HEXADECIMAL/DECIMAL CONVERSION TABLE

DECIMAL - HEX EXAMPLE:

41,246 =

Decimal no. from table nearest equivalent to 41246 but not greater ---->	41246 −40960 286
Decimal no. from table nearest equivalent to 286 but not greater ---->	286 −256 30
Decimal no. from table nearest equivalent to 30 but not greater ---->	30 −16 14

DIGIT HEX VALUE FROM TABLE		DIGIT POSITION FROM TABLE	HEX NO.
40960	A	3	0A11E
256	1	2	
16	1	1	
14	E	0	

TABLE CU

ASCII HEX/OCTAL CONVERSION TABLE

ASCII CHARACTERS	BIT 8=1 EVEN PARITY	HEX	OCTAL	ASCII CHARACTERS	BIT 8=1 EVEN PARITY	HEX	OCTAL
NUL		00	000	1	*	31	061
SOH	*	01	001	2	*	32	062
STX	*	02	002	3		33	063
EXT		03	003	4	*	34	064
EOT	*	04	004	5		35	065
ENQ		05	005	6		36	066
ACK		06	006	7	*	37	067
BEL	*	07	007	8	*	38	070
BS	*	08	010	9		39	071
HT		09	011	:	*	3A	072
LF		0A	012	;		3B	073
VT	*	0B	013	<	*	3C	074
FF		0C	014	=	*	3D	075
CR	*	0D	015	>		3E	076
SO	*	0E	016	?		3F	077
S1		0F	017	@	*	40	100
DLE	*	10	020	A		41	101
DC1		11	021	B		42	102
DC2		12	022	C	*	43	103
DC3	*	13	023	D		44	104
DC4		14	024	E	*	45	105
NAK	*	15	025	F	*	46	106
SYN	*	16	026	G		47	107
ETB		17	027	H		48	110
CAN		18	030	I		49	111
EM	*	19	031	J	*	4A	112
SUB	*	1A	032	K		4B	113
ESC		1B	033	L	*	4C	114
FS	*	1C	034	M		4D	115
GS		1D	035	N		4E	116
RS		1E	036	O	*	4F	117
US	*	1F	037	P		50	120
SP (space)	*	20	040	Q	*	51	121
!		21	041	R	*	52	122
"		22	042	S		53	123
%	*	25	045	T	*	54	124
&		26	046	U		55	125
'		27	047	V		56	126
(		28	050	W	*	57	127
)	*	29	051	X	*	58	130
*	*	2A	052	Y		59	131
+		2B	053	Z		5A	132
,	*	2C	054	[	*	5B	133
-		2D	055	\		5C	134
.		2E	056	]	*	5D	135
/	*	2F	057	^	*	5E	136
0		30	060	_		5F	137
				`		60	140
				a	*	61	141
				b	*	62	142
				c		63	143
				d	*	64	144
				e		65	145

TABLE CU (Contd)

ASCII HEX/OCTAL CONVERSION TABLE

ASCII CHARACTERS	BIT8 =1 EVEN PARITY	HEX	OCTAL
f		66	146
g	*	67	147
h	*	68	150
i		69	151
j		6A	152
k	*	6B	153
l		6C	154
m	*	6D	155
n	*	6E	156
o		6F	157
p	*	70	160
q		71	161
r		72	162
s	*	73	163
t		74	164
u	*	75	165
v	*	76	166
w		77	167
x		78	170
y	*	79	171
z	*	7A	172
}		7B	173
¦	*	7C	174
{ (ALT MODE)		7D	175
~		7E	176
DEL (RUB OUT)	*	7F	177

8. POWER

A. Physical Layout

8.01 Figures 34 through 39 depict the primary hardware of the 3A Processor power system.

B. Frame Power Distribution

8.02 The maintenance frame contains four power buses: two for +24 volt power and two for -48 volt power. With the exception of the System Status Panel (SSP), its associated units, and alarm circuits, the power buses are connected to separate sides of equipment. Bus A of +24V and -48V is associated with side 0. Bus B of +24V and -48V is associated with side 1. Either bus A or bus B can supply the SSP and the alarm circuits by means of relay switching.

8.03 Tables CV through CY provide pertinent information relating to power distribution fuses.

TABLE CV

KS-21104 POWER CONVERTER FUSES

FUSE DESIG.	AMPERAGE	VOLTAGE	UNIT SUPPLIED
F1	8A	+15	KS-26571
F2	8A	−15	KS-26571
F3	25A	−24.5	KS-26571
F4	6A	+15	KS-26571
F5*	5A	+5.3	KS-26571
F6*	2A	−15	KS-26571

TABLE CW

PROCESSOR FRAME FUSE ASSIGNMENT
3A CC AND MAS

FUSE DESIGNATION AND AMPERAGE		EQUIPMENT						
-48V	+24V	TYPE	UNIT	FRAME	VOLT	3A CC PANEL AND MAS MEMORY		
		J87389J +5V	02-05	08-05	+5	3A CC panel LEDs and MAS memory termination circuits		
						3A CC CIRCUIT PACKS		
AO			02-09	08-09	+3v	QUAN	TYPE	POSITION
	AA10				1	FC21	06-01	
						1	FA1031	06-04
3A	3/4A					3	FB6	06-05, 07, 08
						1	FA1034	06-06
						3	FA1010	06-09, 10, 11
	AA11		06-05	12-05	+3v	1	FC21	06-01
						5	FA1010	06-12, 13, 14, 16, 17
	3/4A					1	FC21	02-14
			10-04	16-04		2	FA1030	02-19, 20
						2	FA1029	02-21, 22
						1	FA1046	02-23
A1	AA5	J87389F	10-09	16-09	+3v	1	FC21	02-14
						1	FA1033	02-24
3A	3/4A					1	FA1032	02-25
						1	FC202	02-26
						1	FA1037	02-27
						1	FA1036	02-28
			10-14	16-14	+5V	2	ED4C154	02-41, 06-41
			10-19	16-19	+3V	1	FC21	02-01
						1	FB6	02-03 spare
						1	FB6	02-24
						2	FA1024	02-12, 13
						3	FA1024	02-16, 17, 19
			10-24	16-24	+3V	1	FC21	02-01
						1	FA1031	02-02
						4	FA1024	02-08, 09, 10, 11

See Notes at end of Table.

TABLE CW (Contd)

PROCESSOR FRAME FUSE ASSIGNMENT
3A CC AND MAS

FUSE DESIGNATION AND AMPERAGE		EQUIPMENT						
-48V	+24V	TYPE	UNIT	FRAME	VOLT	3A CC CIRCUIT PACKS		
						QUAN	TYPE	POSITION
			10-29	16-29	+5V	2	ED4C154	02-43 06-43
		J87389F +3V	10-34	16-34	+3V	1 2 1 2	FC21 FA1038 FA1039 FC201	06-02 10-07, 11 10-08 10-09, 10
A2	AA12		10-38 10-42	16-38 16-42	+3V	2 2	ED4C154 ED4C154	02-41, 06-41 02-43, 06-43
3A	3/4A		10-42	16-42	+3V	1 1 1 1 1 1	FA1035 FA1023 FA1022 FA1018 FA1017 FA1016	02-29 02-31 02-32 02 33 02-34 02-35
A3 3A	AA10 3/4A	J87389F +3V	06-09	12-09	+3V	3 2 1	FA1040 FA1035 FC201 FC21	02-05, 06, 07 10-12 10-13, 14 06-02
		J87389J +5V	06-14	12-14	+3V	2 1	ED4C154 FB486	02-37, 06-37 06-29
	AA6		06-10	12-10	+3V	1 1 1 2 1 1	FC21 FA1038 FA1039 FC201 FA1028 FA1027	10-01 10-03 10-04 10-05, 06 10-22 10-23
	3/4A				+3V	2 1	ED4C154 FB486	02-37, 06-37 06-29
		J87389F +3V	06-19	12-19	+3V	1 1 1 2 1 1	FC21 FA1038 FA1039 FC201 FA1028 FA1027	10-01 10-03 10-04 10-05, 06 10-22 10-23
		J87389F	06-24	12-24		2 3	FA1015 FA1012	06-23, 26 06-24, 25, 27

See Notes at end of table.

TABLE CW (Contd)

PROCESSOR FRAME FUSE ASSIGNMENT
3A CC AND MAS

FUSE DESIGNATION AND AMPERAGE		EQUIPMENT						
-48V	+24V	TYPE	UNIT	FRAME	VOLT	3A CC CIRCUIT PACKS		
						QUAN	TYPE	POSITION
	A6	+3V			+3V	2 1 1	Spare TS8 TS9	10-2, 25 10-26 10-27
		J87389J	06-29	12-29	+5V	2	ED4C154	02-39, 06-39
A4 3A	AA4 3/4A	J87389F	06-34	12-34	+3V	1 1 1 1 1 1	FA1010 FA1020 FA1026 FA1013 FA1012 FC21	06-18 06-19 06-20 06-21 06-224 10-29
		J87389F +3V	06-38	12-38	+3V	1 1 1 1 1 1 1 1	FA1014 FB486 FA1025 FA1019 FA1011 FA1045 FA1021 FC21	06-28 06-29 06-31 06-32 06-33 06-34 06-35 06-44
A5	AA3	J87389F +3V	08-29	46-29	+3V	1 2 1 1 1/2	TS2 FA1060 FA1061 FA1063 FC21	08-01 08-05, 09 08-18 08-22 08-35
		J87389F +3V	06-42	12-42	+3V	2 2 1	ED4C154 ED3C154 FC21	02-37, 06-37 02-39, 06-39 06-44
A5 3A	AA13 3/4A	J87389F +3V	08-29	46-29	+3V	TS2 2 1 1 1	TS2 FA1060 FA1061 FA1063 FC21	08-01 08-05, 09 08-18 08-22 08-35
		J87389F +3V	08-34	46-34	-3V	2 1 1	FA1060 FA1064 FC203	08-06 08-19 08-23
						3	FA1060	08-3, 07, 16

See notes at end of table.

TABLE CW (Contd)

PROCESSOR FRAME FUSE ASSIGNMENT
3A CC AND MAS

FUSE DESIGNATION AND AMPERAGE		EQUIPMENT						
-48V	+24V	TYPE	UNIT	FRAME	VOLT	3A CC CIRCUIT PACKS		
						QUAN	TYPE	POSITION
			08-39	46-39	+3V	1 1 1	FA1064 FA1071 FC21	08-20 08-24 08-40
	AAO 3/4A Strt volt	J87389F +3V J87421A	08-44 03-38	46-44 41-38	+3V +5V	2 1 1 1 1	FA1060 FA1062 FA1065 FC262 JK3	08-04, 08 08-17 08-21 08-25 03-02
A6 3A	AA13 3/4A	J87422VB -5V +12C	03-44	41-44	+5V +12C	2 2 2 2 1	JL2 JL2 JL2 JL2 JL2	03-04, 05 03-06,07 03-08, 09 03-10, 11 03-17
		J87421A J87422B	03-44 03-44	41-44 41-44	+5v -5v +12V	1 1 2 2 2 2	JK3 JL2 JL2 JL2 JL2 JL2	03-33 03-19 03-23, 24 03-25, 26 03-27, 28 03-29, 31

Note 1: Fuses A7, A8, and A9 are reserved for modules 2,3; 4,5; and 6,7 respectively with power distribution as shown for A6.

Note 2: When removing fuses ALWAYS remove indicator fuse first. If power fuse is removed first, indicator fuse will blow.

TABLE CX

CTI/POWER UNIT FUSES

FUSE DESIG	AMPERAGE	VOLTAGE	UNIT SUPPLIES
D0/D0P	3A/0.5A	-48	132M Power Converter
D1/D1P	3A/0.5A	-48	132M Power Converter
D2/D2P	3A/0.5A	-48	132M Power Converter
C0/C0P	5A/0.5A	+5	PCH 1 Logic
C1/C1P	5A/0.5A	+5	PCH 1 Logic
C2/C2P*	5A/0.5A	+5	PCH 1 Bus
C3/C3P	5A/0.5A	+5	PCH 1 Logic
C4/C4P	5A/0.5A	+5	PCH 0 Logic
C5/C5P	5A/0.5A	+5	PCH 0 Logic
C6/C6P*	5A/0.5A	+5	PCH 0 Bus
C7/C7P	5A/0.5A	+5	PCH 0 Logic
C8/C8P	5A/0.5A	+5	DMA Logic
C9/C9P	5A/0.5A	+5	DMA Logic
C10/C10P	5A/0.5A	+5	DMA Logic
C11/C11P	5A/0.5A	+5	DMA Bus
C12/C12P	5A/0.5A	+5	DMA Logic
C13/C13P	5A/0.5A	+5	DMA Logic
C14/C14P†	5A/0.5A	+5	CTI Logic
D3P	0.5A	-48	132M Converter Alarm Power

* Fuse value increases to 10A when subparallel channels exceed four.

† C14/C14P fed by DMA converter when equipped, otherwise by PCH 0 converter.

TABLE CY
MAINTENANCE FRAME FUSES

FUSE DESIG.	AMPERAGE	PWR BUS	VOLTAGE	UNIT SUPPLIED
AA0A/AA0AP	2/0.5	A	+24	SSPR
AA0B/AA0BP	2/0.5	B	+24	SSPR
AA1A	0.5	A	+24	ALM Ckts
AA1B	0.5	B	+24	ALM Ckts
AB0A/AB0AP	2/0.5	A	+24	TTYC 0
AB0B/AB0BP	2/0.5	B	+24	TTYC 1
AC0A	0.75	A	+24	TDC 0
AC0B	0.75	B	+24	TDC 1
A1	1.75	A/B	-48	E2A
A0A	2	A	-48	SSPR
A0B	2	B	-48	SSPR
B0A	2	A	-48	TTYC 0
B0B	2	B	-48	TTYC 1
C0B	1.75	B	-48	TDC
C1B	2	B	-48	TDC
C0A	1.75	A	-48	TDC
C1A	2	A	-48	TDC
AA2	0.75	A/B	+24	SSP LEDs
AA3	1.3	A/B	+24	SSP Lamps
AA4	0.5	A/B	+24	E2A

9. SUPPLEMENTARY REFERENCE MATERIAL

9.01 The following index of schematic drawings (SDs) and an index to EOS documents is provided to ensure a total coverage of reference material in this section.

SCHEMATIC DRAWING INDEX

SD1C900-01	3A Central Control	J1C050A
SD1C901-01	3A CC Control Panel	ED4C006-30
SD1C902-03	Main Store Controller & Memory	J1C052C
SD1C903-02	Main Store Memory	J1C052B
SD1C904-01	Tape Data Controller	J1C053A
SD1C905-01	TTY Controller Unit	J1C054A
SD1C906-01	System Status Panel	ED4C007
SD1C907-01	System Status Panel Controller	J1C055A
SD1C908-01	SSP Relay Unit	J1C056A
SD1C909-01	Maintenance Frame Power	J1C061A
SD1C910-02	Processor Frame (2B or 3 ESS)	J1C058B
SD1C911-02	Processor Frame Power	J1C057B
SD1C912-01	Maintenance Frame	J1C060A
SD1C914-01	Supplementary Main Store Power	J1C064A
SD1C915-01	Supplementary Main Store Frame	J1C065A
SD4C005-02	Programmable Read-Only Memory	ED4C154
SD4C007-02	3A Processor Frame	J1C106B
SD4C008-01	Direct Memory Access	J1C106AA
SD4C009-01	Parallel Channel	J1C106AB
SD4C0010-01	CTI/Power Unit	J1C106AC
SD4C012-01	Duplex Bus Selector	J1C107A
SD4C013-01	RS232 Serial Interface	J1C108A
SD4C018-01	Writeable Store Unit	J1C122A
SD4C023-01	Programmable Controller (PROCON)	
SD4C024-02	PROCON 16-Bit Self-Checked	J1C082A
SD73124-01	TNS Application Schematic	
SD28118-01	ETS Application Schematic	

INDEX TO EOS DOCUMENTS

DOCUMENT SUBJECT		DOCUMENT ID NO.
	Extended Operating System Programs	PG-4C001
	MICA3A Microcode (Common Systems)	PK-4C002-02
	MANUALS:	
	Input Message Manual (EOS)	IM-4C001-02
	Output Message Manual (EOS)	OM-4C001-02
	Trouble Locating Manual (EOS)	TLM-4C702-01
	Trouble Locating Manual (EOS)	TLM-4C704-01
	Trouble Locating Manual (EOS)	TLM-4C705-01
	Trouble Locating Manual (EOS)	TLM-4C706-01
	Trouble locating Manual (EOS)	TLM-4C707-01
	Trouble Locating Manual (EOS)	TLM-4C708-01
	Trouble Locating Manual (EOS)	TLM-4C709-01
	Trouble Locating Manual (3A Common)	TLM-1C900-01
	Microcode (Common Systems)	PK-4C002-02
	PROGRAMS: (EOS PG-4C001)	
	KERNEL FUNCTION PROGRAMS:	
DEVATT	Initialize Periphery and Create Device Tables	PR-4C104-01
INTSRV	Interrupt Service Routine	PR-4C113-01
RSTGWG	Return a Restart State	PR-4C129-01
SAVPGG	Save Register and Program State in Process Descriptor	PR-5C133-01
SYSMM	System Memory Management	PR-4C141-01
TCONAU	Convert Binary Time to Character	PR-4C142-01
TIMEAU	Control System Interval Timing in the System	PR-4C144-01
LOSTAB	Lab Operating System Tables	PR-4C147-01
INTRPT	Interrupt Handling Program	PR-4C148-01
CONVTD	Operating System Data Conversion Routines	PR-4C149-01
DISPAT	Operating System Process Dispatcher	PR-4C150-01
EVTDIS	Process Event Dispatcher	PR-4C151-01
EVTMGR	Event Manager	PR-4C152-01
MSGMGR	Message Manager	PR-4C153-01
PCRTRM	Process Creator and Terminator	PR-4C154-01
PROCON	Miscellaneous Process Control	PR-4C155-01
PRSTAT	Process State Transition Manager	PR-4C156-01
AUDIT	Kernel Audit	PR-4C157-01
MINTAB	Minimum Configuration Tables	PR-4C158-01
	INPUT/OUTPUT FUNCTION PROGRAMS:	
ACCMTH	Access Method for Device Handler	PR-4C201-01
ACCOPN	Access Method Directory Reader	PR-4C202-01
CATLOG	Attach, Detach Catalog Files	PR-4C203-01
CATSYS	EOS Catalog	PR-4C204-01

INDEX TO EOS DOCUMENTS (Contd)

INPUT/OUTPUT FUNCTION PROGRAMS: (Contd)

DMA	DMA Scheduler	PR-4C205-01
FILDEV	Device Handler Interface	PR-4C206-01
FILSYS	File System SVC Handler	PR-4C207-01
IOERMS	Output Error Message to the Maintenance Console	PR-4C208-01
JHPROD	PROMATS DMA Driver	PR-4C209-01
OPNTSK	Open Files	PR-4C210-01
PCHMAT	Promats Parallel Channel Driver	PR-4C211-01
RSIDRV	RSI Modem Driver	PR-4C212-01
TAPTSK	Promats State Routine	PR-4C213-01
TDCHND	Basic TDC Base Level Driver	PR-4C214-01
TDCINT	Interrupt Level Driver	PR-4C215-01
TDCSTA	State Level Driver	PR-4C216-01
TERMAD	TTY Terminal Administration	PR-4C217-01
TTSTAT	TTY Scheduler	PR-4C218-01
TTYDRV	TTY Driver	PR-4C219-01
TAPITF	Overwrite Program Interface to File System	PR-4C220-01
SRCON	System Reconfiguration Program	PR-4C221-01
ALZEX	Executive for Input and Output Analyzers	PR-4C222-01
DADBRD	Data Administrator—Writes to Terminals	PR-4C223-01
DADINT	Data Administrator—Initialization	PR-4C224-01
DADOUT	Accepts Client Output Messages	PR-4C225-01
DADRED	Data Administrator—Accepts Terminal Output	PR-4C226-01
DADSUB	Data Administration—Common Subroutines Program	PR-4C227-01
EOSMSG	Client Interface to Data Administrator	PR-4C229-01
ESSALZ	ESS Catalog Search Program	PR-4C230-01
EXPNDR	Output Message Binary to ASCII Converter	PR-4C231-01
PARSER	Input Message Scanner	PR-4C232-01
PRSSUB	Common Subroutine for TTY Package	PR-4C233-01
TTYALZ	Output Analyzer for TTYC Device	PR-4C234-01

MESSAGES AND COMMAND FUNCTION PROGRAMS:

CMDAU	Parse and Process a Command	PR-4C301-01
CMRAID	Insert Breakpoints to Raid at BPADR	PR-4C302-01
CHPROC	Change Priority of a Process or Task	PR-4C303-01
CREADY	Ready State Processor	PR-4C304-01
DIVIDE	Divide Non-Negative Bit by Positive Number	PR-4C305-01
DPROC	Display Active Processes	PR-4C306-01
EOS	TTY Process Initiator	PR-4C307-01
NAMSYS	Print System Name of a Process in Hex	PR-4C308-01
OSWRIT	Write Buffer Onto File Sysout	PR-4C309-01
RDTIME	Print Out Current Date and Time	PR-4C310-01
SETTIM	Set the Time in the System Clock	PR-4C311-01
SPAWN	Spawn a Task	PR-4C312-01
STAT1	Print Out Statistics for Task	PR-4C313-01

RESIDENT APPLICATION TTY TABLES FUNCTION PROGRAMS:

TTYTBL	TTY Data Layout Program	PR-4C401-01
USRTBL	Users TTY Data Layout Program	PR-4C402-01

INDEX TO EOS DOCUMENTS (Contd)

SYSTEM UTILITIES FUNCTION PROGRAMS:

DTACRT	Write a Fully Formatted Cartridge Over Data Link	PR-4C501-01
DGNTD	DBS Diagnostic Utility	PR-4C502-01
MAITST	Maintenance Feature Test Program	PR-4C503-01
RAIDB	Debugging Utility	PR-4C504-01
CRTETS	Fully Formatted Cartridge Writer	PR-4C505-01
INITS	RAIDB Subroutines	PR-4C506-01

SYSTEM MAINTENANCE FUNCTION PROGRAMS:

DGNDBS	DBS Diagnostic	PR-4C602-01
MAICCI	EOS Initialization Program	PR-4C605-01
MAIDTA	Maintenance Data Layouts	PR-4C606-01
MAINT	Maintenance Task	PR-4C607-01
MAISUB	Maintenance Subroutines	PR-4C608-01
MAISVC	Maintenance SVCs	PR-4C609-01
MASACS	Mainstore Audit Program	PR-4C611-01
TTYAPP	ESS-Type Command Interpreter	PR-4C613-01
CSYSUB	Common System Routine	PR-4C615-01
CIPL	Bootstrap Program	PR-4C616-01
CBLM	Base Level Maintenance Monitor	PR-4C617-01
CINIT	CC Initialization Program	PR-4C618-01
CPAGM	Paging Monitor	PR-4C619-01
CTSD	Common System Data Layout	PR-4C621-01
CUTIL	Common System Utility Program	PR-4C622-01
CNRUTIL	Nonresident Patching Program	PR-4C623-01
BANANA	Points to EOS Translations	PR-4C625-01
AUTOMN	Diagnostic Monitor	PR-4C626-01

DIAGNOSTIC FUNCTION PROGRAMS:

BLMMA	CC Diagnostic Transfer Vector	PR-4C701-01
DGDMA	DMA Diagnostic (Part 1)	PR-4C702-01
DGLIU	DMA Diagnostic (Part 2)	PR-4C703-01
DGNCTI	CTI Diagnostic	PR-4C704-01
DGNPCH	Parallel Channel Diagnostic	PR-4C705-01
CTAPM	Common Tape Maintenance	PR-4C706-01
DGNPRO	PROMATS Diagnostic	PR-4C707-01
DGNRSI	RSI Diagnostic	PR-4C708-01
DGNTC	TTYC Diagnostic	PR-4C709-01
CDGNM	Common Diagnostic Monitor	PR-4C910-61
CDGSR	Double Store Read Test	PR-4C911-61
CDGMCH	MCH, Gating Bus, Clock and Register Initialization Test	PR-4C912-61
CDGTC	To and From Field Crosspoint Test	PR-4C913-61
CDGMLT	Multiple Crosspoint Test	PR-4C914-61
CDGREG	Register Gating Test	PR-4C915-61
CDGMIC	Microstore Content Test	PR-4C916-61
CDGFN	Data Manipulation Logic (DML) Test	PR-4C917-61
CDGS3A	Off-line Store Diagnostic Code	PR-4C918-61

INDEX TO EOS DOCUMENTS (Contd)

DIAGNOSTIC FUNCTION PROGRAMS: (Contd)

CDGMC1	Microcontrol Tests	PR-4C919-61
CDSPA1	DS and PA+1 Adder Tests	PR-4C920-61
SDGMSQ	Store Bus Controller Test	PR-4C921-61
CDGSIO	Store I/O Access Test	PR-4C922-61
CDGSMX	Store Multiplex Circuit Test	PR-4C923-61
CDGSBS	Store Bus Communication Test	PR-4C924-61
CDGSFA	Store Fanout Boards Test (Part A)	PR-4C925-61
CDGSB	Store Fanout Boards Test (Part B)	PR-4C926-61
CDGSWP	Store Write Protect Test	PR-4C927-61
CDGSCN	Interprocessor Store Bus Test	PR-4C928-61
CDGSD	Memory Element Test	PR-4C929-61
CDGMI	Micro Interpret Multiple Crosspoint and Parity Check Tests	PR-4C930-61
CDGNTI	Timing Counter Interrupt Address and Data Matcher and I/O Test	PR-4C931-61
CSTATS	System Status Bits, Switching and Panel Tests	PR-4C932-61
CDGNOP	Off-Line Diagnostic Code	PR-4C933-61
CDGSOP	Store Control and Parity Test	PR-4C934-61
CDGSDF	Store Controller Data Register Test	PR-4C935-61

OVERWRITE FUNCTION PROGRAMS:

DTC	Diagnostic Temporary Change Program	PR-4C801-01
EQSOWC	Patch Overwrite Facility	PR-4C802-01

BELL SYSTEM PRACTICES:

Software Subsystem Descriptions:

Extended Operating System (EOS) Overview	254-340-001
Memory Protection and Organization	254-340-014
Processor/Process Management, Creation, Event and Communication Control	254-340-030
Processor/Process Management, Interrupt Handling and Timer Management	254-340-031
Data Administration	254-340-040
Device Handlers	254-340-052
Terminal Administrator	254-340-054
File System	254-340-062
Data Base Organization	254-340-064
Maintenance Overview	254-340-080
System Utilities	254-340-082
Resident Maintenance	254-340-084
Initialization and Recovery	254-340-086
Processor Diagnostics	254-340-088
Peripheral Diagnostics	254-340-090
Introduction to 3A Language	254-340-100
Basic and Extended 3A Processor Instruction Set	254-340-102
Program Listing Organization and Usage	254-340-104
Extended Operating System, Macros and Glossary	254-340-106

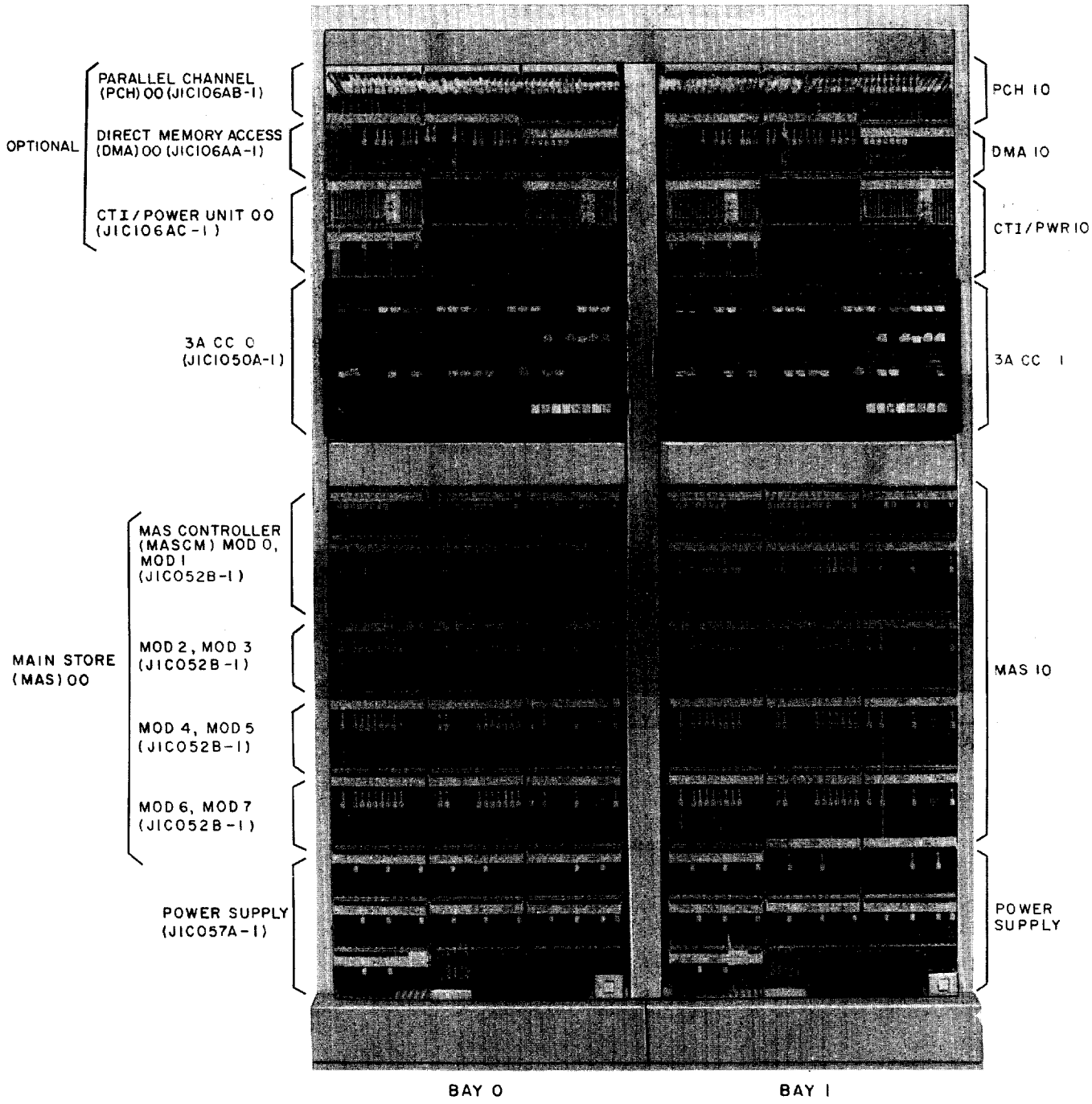


Fig. 1—Duplex 3A Processor Frame

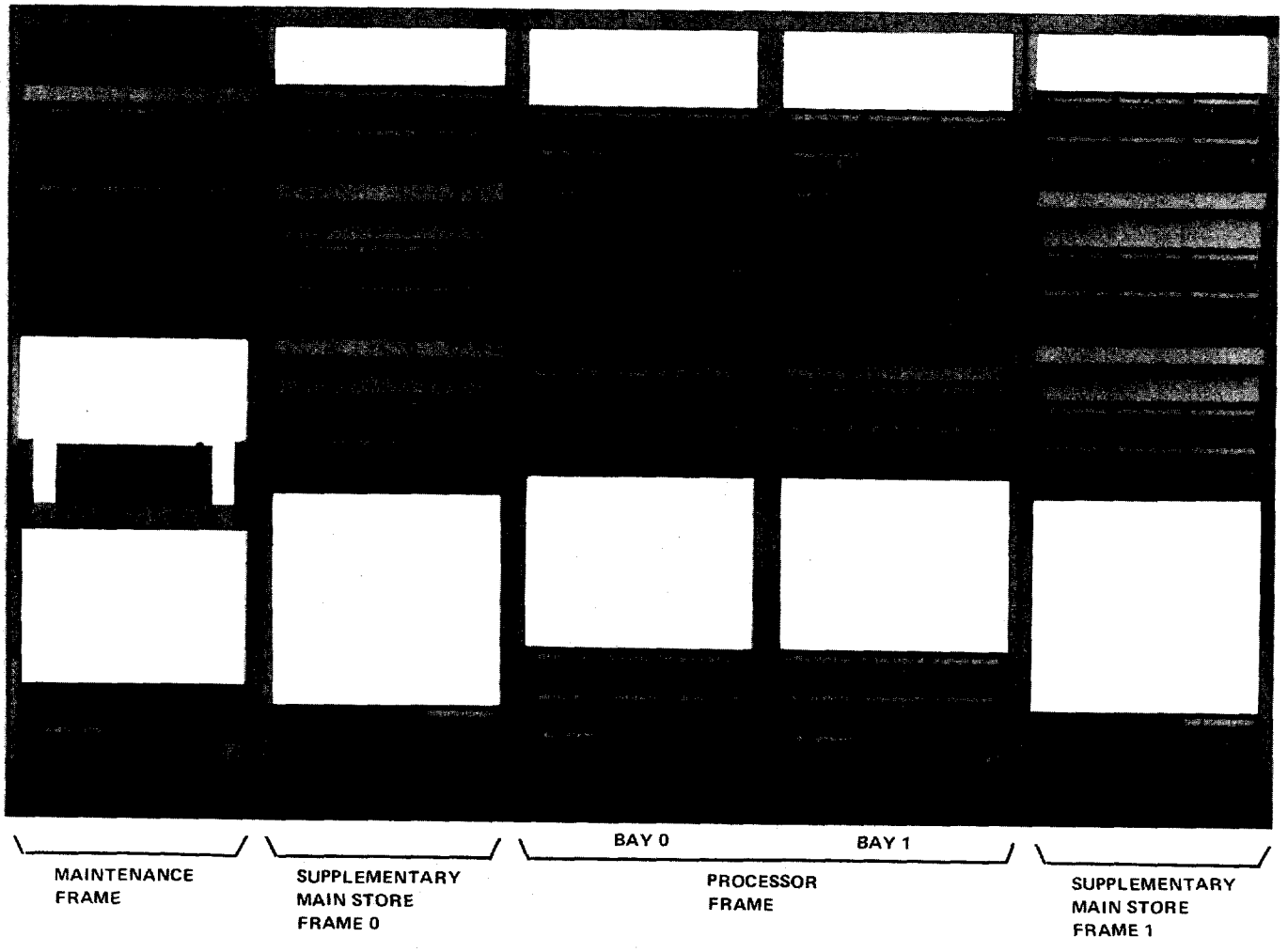
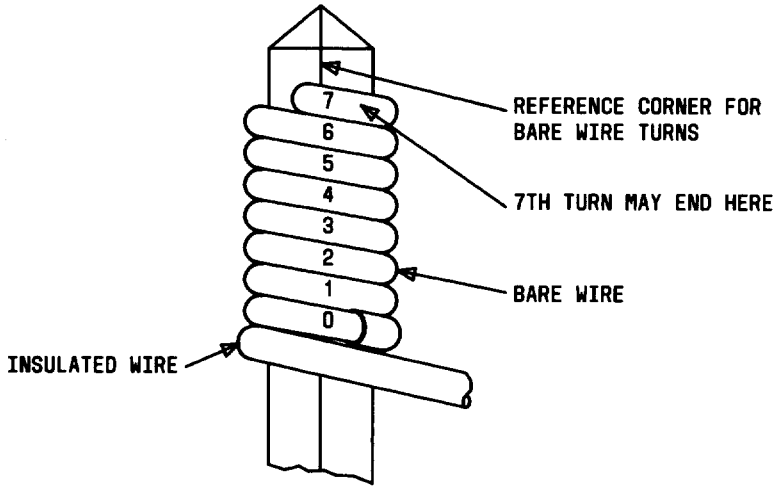


Fig. 2—3A Processor with Supplementary Store

Wiring Requirements

Wire-Wrap Connections (modified wrap)



- Minimum of 7 consecutive nonoverlapping helical turns of bare (uninsulated) wire.
- Insulated portion of the wire should be in contact with from two to four corners of the terminal. The allowable clearance between the insulation wire and the third corner is 0.015 inch.

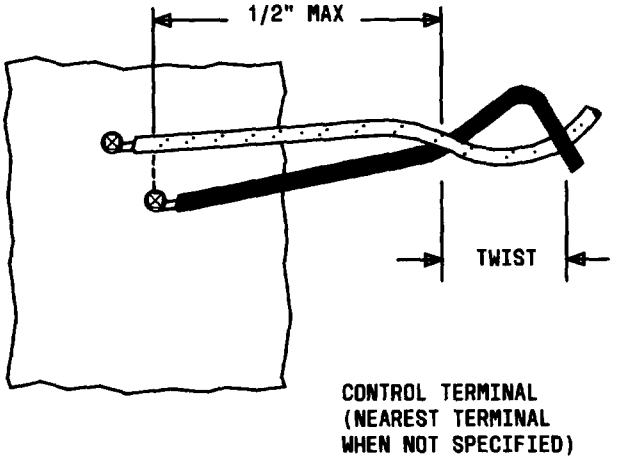
Note:

A wire wrap that does not meet the requirements, is referred to as a nonmodified wire wrap.

Fig. 3—Wire Wrap Repair Procedures (Sheet 1 of 9)

Twisted Leads

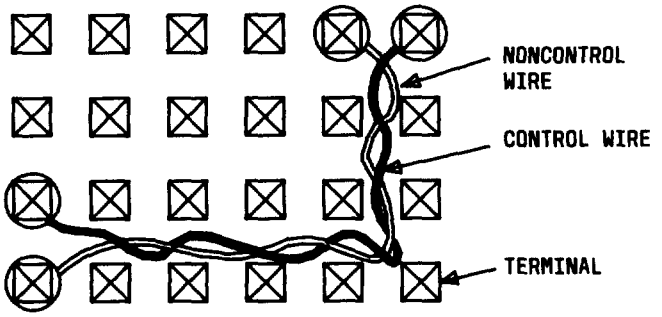
Start of Twist



Notes:

- Twisted leads shall run in definite vertical and horizontal paths.
- Unless otherwise specified, the green wire is the signal (or control) wire and the white wire is the ground (or noncontrol) wire.
- Wire slack should not exceed 0.50 inch.
- When the terminals are not in the same horizontal or vertical path, run the wire:
  - Horizontally from the lower terminals.
  - Vertically to the upper terminals.
- When changing the wire direction, a radial bend should be made around several pins. If a path is blocked, refer to Section 800-612-150 for "blocked surface wire path" rules.
- When the noncontrol wire is terminated further than one terminal spacing from the control terminal, the extended portion of the noncontrol wire is treated as a single wire.

Wiring Path



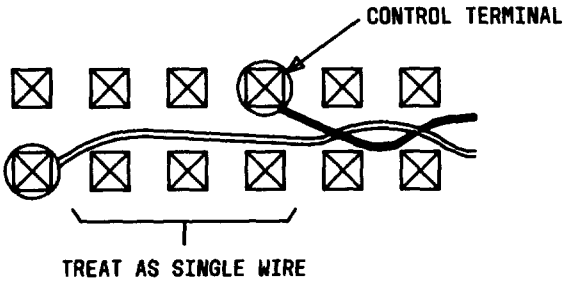
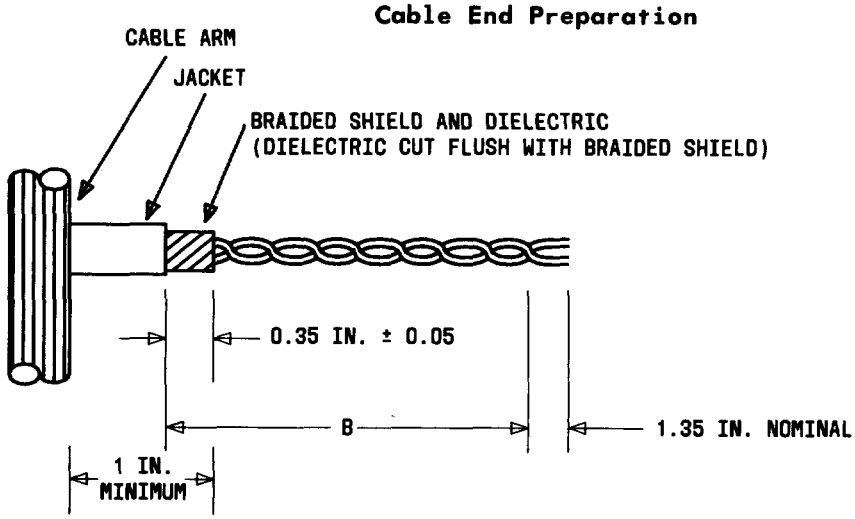


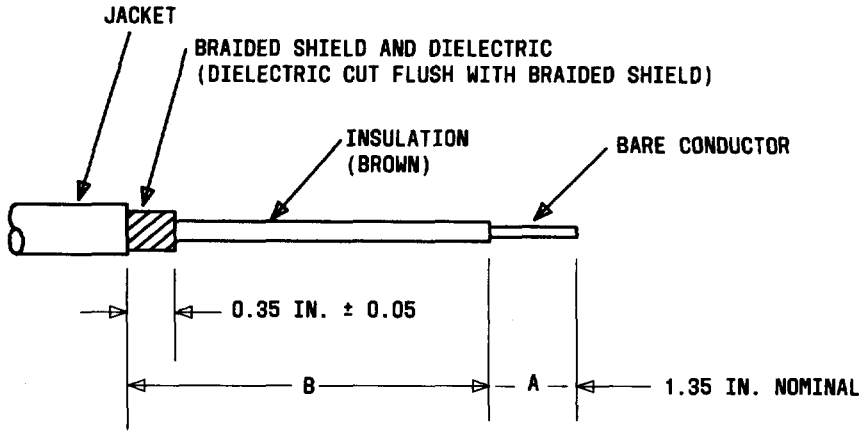
Fig. 3—Wire Wrap Repair Procedures (Sheet 2 of 9)

Cable End Preparation



TERMINATION GROUP	JACKET	DIMENSION (IN.) A*	B
G-1	ORANGE	1.00	1.54
G-2	ORANGE	2.30	2.84

A. KS-21238, Shielded Wire (Single or Twisted Lead)



TERMINATION GROUP	JACKET	COAX CABLE (OHM)	DIMENSION (IN.) A*	B
G-1	WHITE	75	1.00	1.54
G-2	WHITE	75	2.30	2.84
G-3	BLUE	100	1.00	1.54
G-4	BLUE	100	2.30	2.84
G-5**	WHITE	75	3.30	3.84
G-6**	BLUE	100	3.30	3.84

* TERMINATING LEAD LENGTHS

** USE ONLY ON ONE END OF CABLE

B. KS-2112, 75- and 100-Ohm Coax Cable

Fig. 3—Wire Wrap Repair Procedures (Sheet 3 of 9)

Common Wire Defects

The more common types of backplane wire defects and their method of repair are:

WIRE DEFECT	REPAIR PROCEDURE
Exposed conductor - Insulation has been cut causing exposure of the conductor.	See Chart A (Fig. 1, Sheet 5)
Wire deformation - Insulation has been cut, nicked, or scraped. However, conductor is not exposed.	See Chart B (Fig. 1, Sheet 6)
Wire-wrap trail - Piece of wire end that projects from a wire-wrapped terminal.	
Wire stub - Wire that has only one end connected to a terminal.	See Chart C (Fig. 1, Sheet 7)
Nonmodified wire wrap - Wire-wrap connection that does not meet the modified wire-wrap wiring requirements.	
Bent terminal - Terminal that is in contact with or within 0.025 inch of another terminal.	Bend the terminals back into position
Conductive particles in the back plane.	

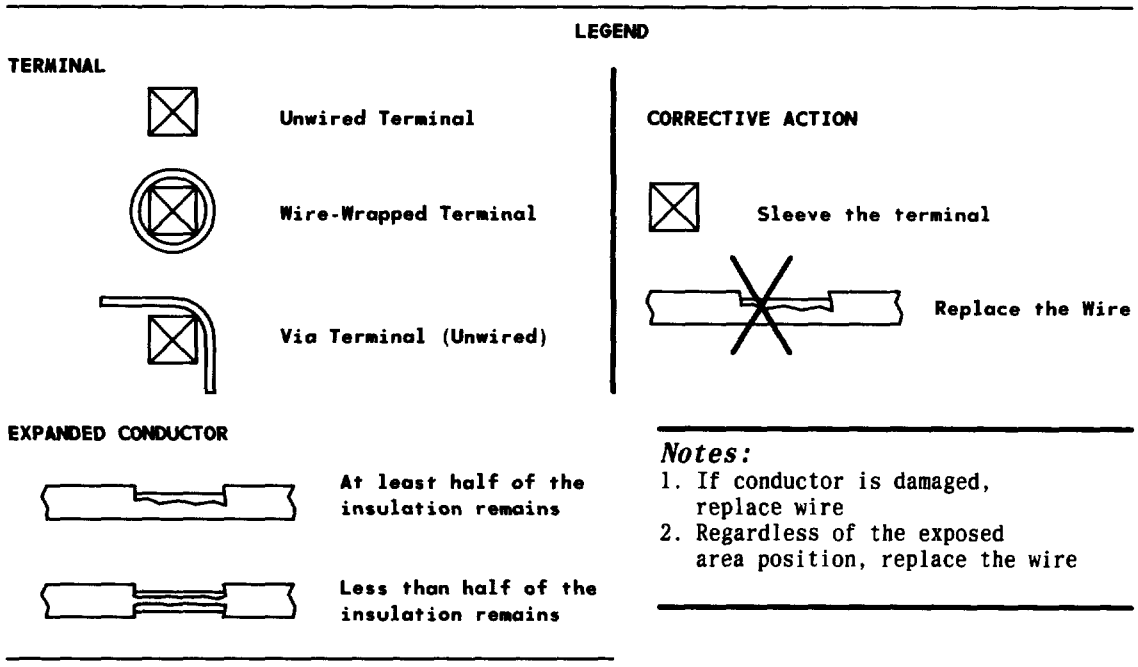


Fig. 3—Wire Wrap Repair Procedures (Sheet 4 of 9)

Chart A - Exposed Conductor Repair

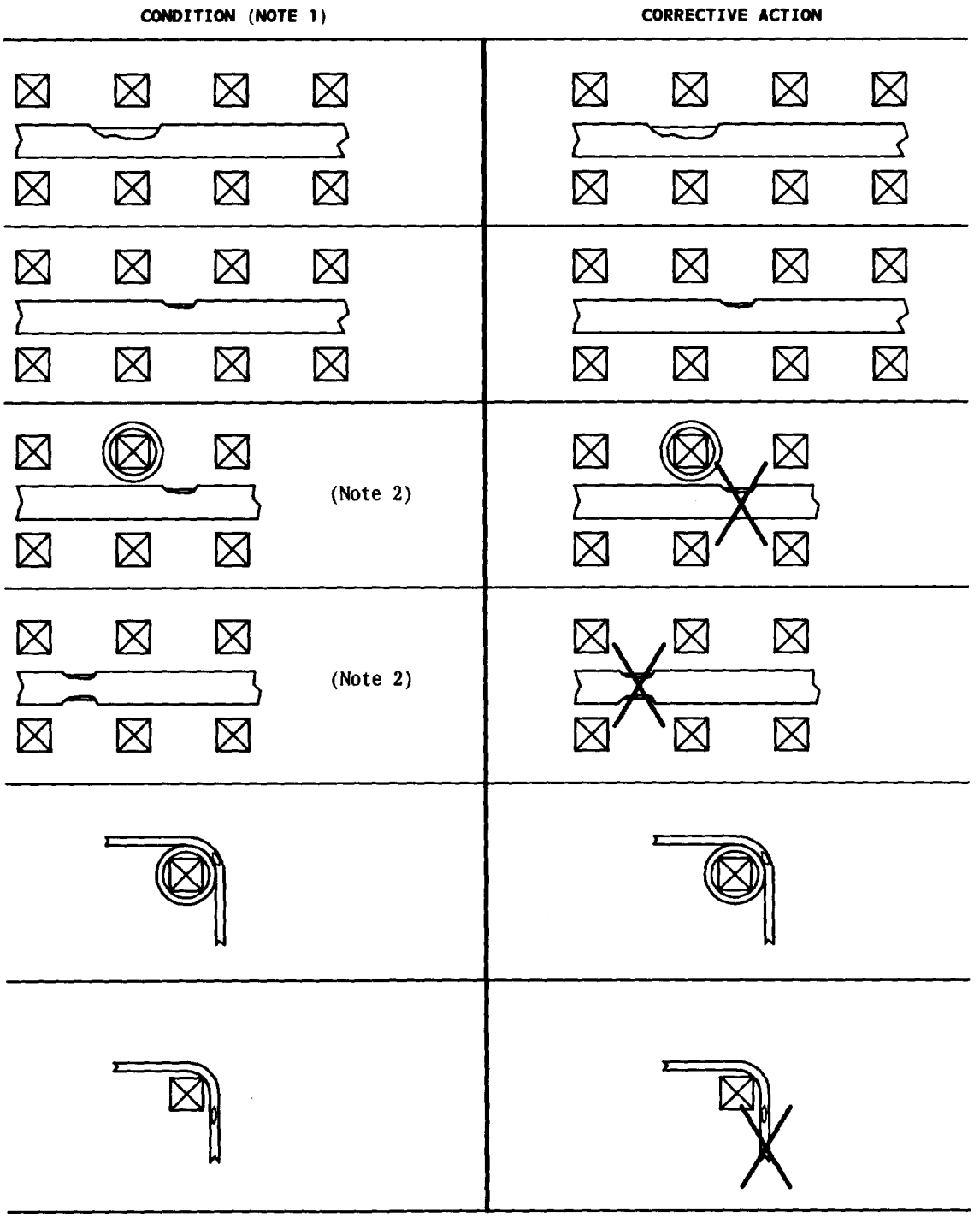


Fig. 3—Wire Wrap Repair Procedures (Sheet 5 of 9)

Chart B – Wire Deformation Repair

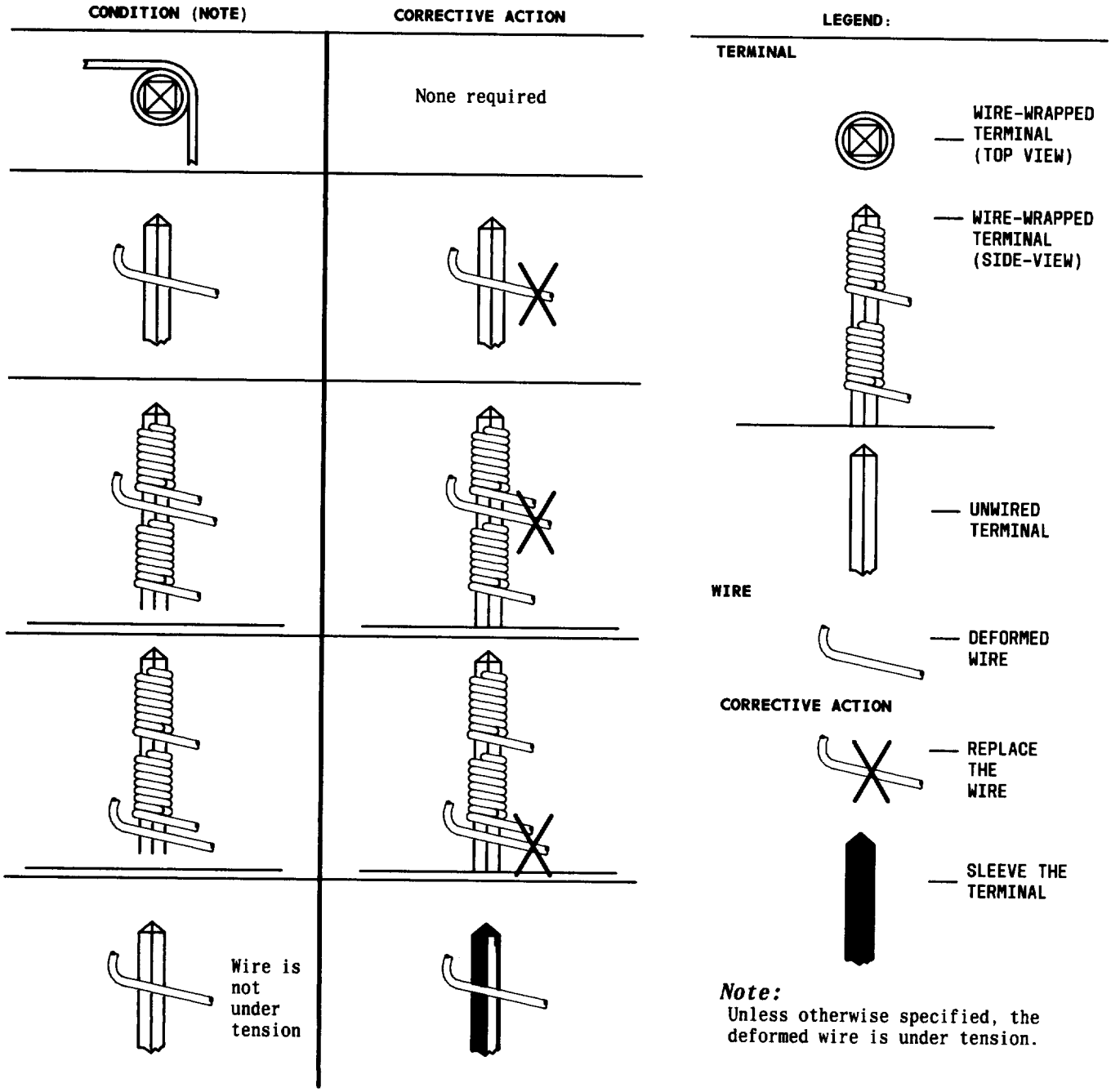


Fig. 3—Wire Wrap Repair Procedures (Sheet 6 of 9)

Chart C - Wire-Wrap Trails, Wire Stubs, and Nonmodified Wire-Wrap Repair

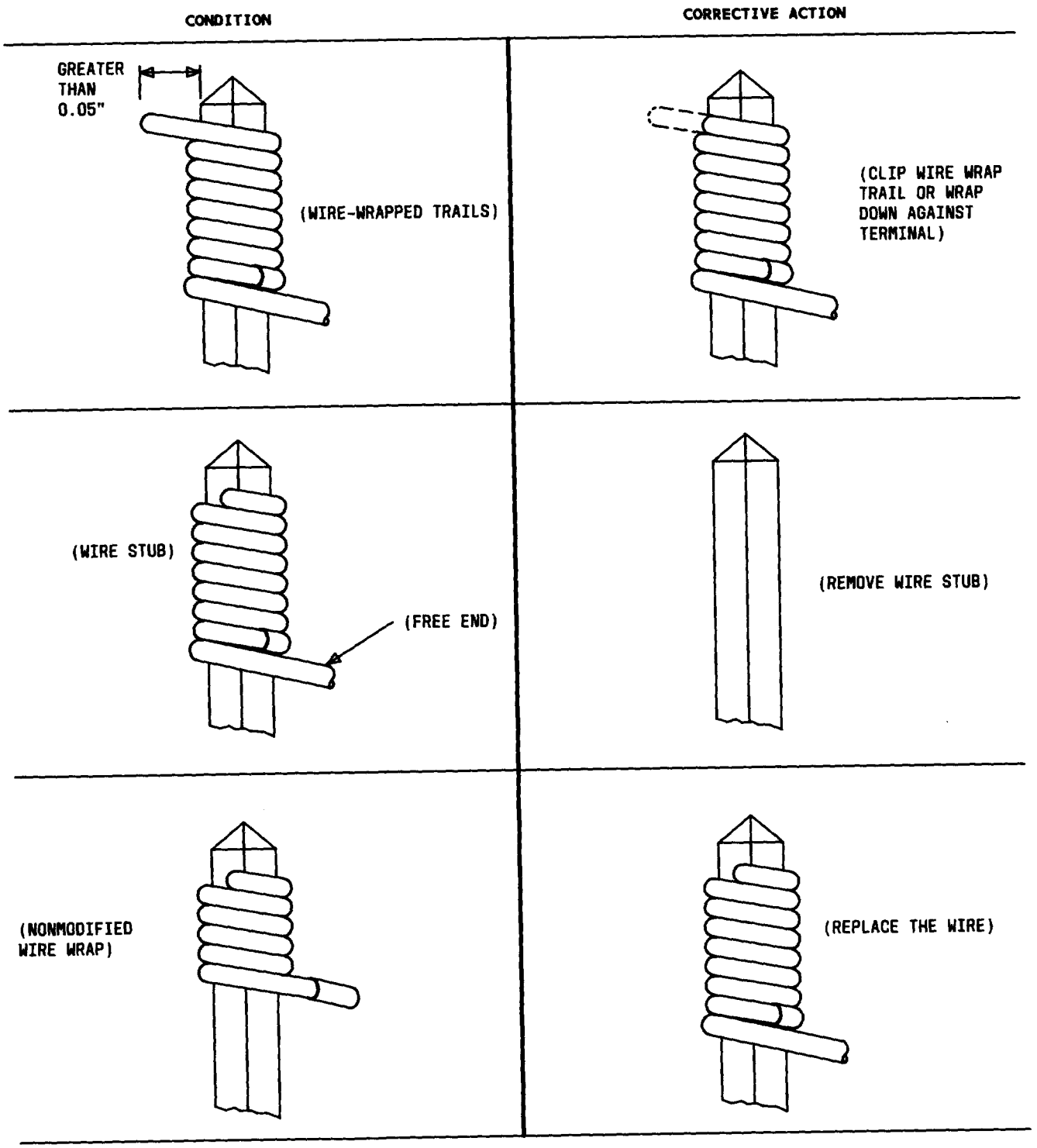
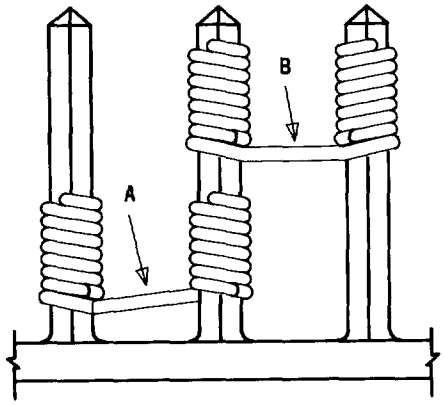


Fig. 3—Wire Wrap Repair Procedures (Sheet 7 of 9)

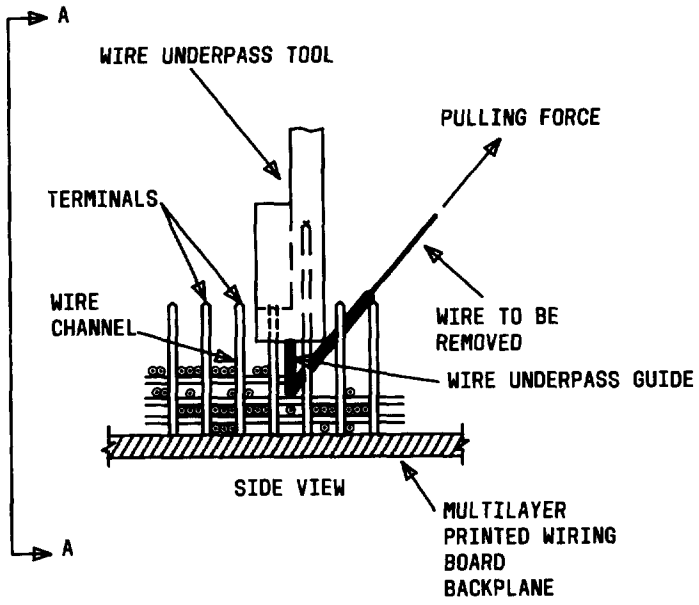
Guidelines for Replacing Wire

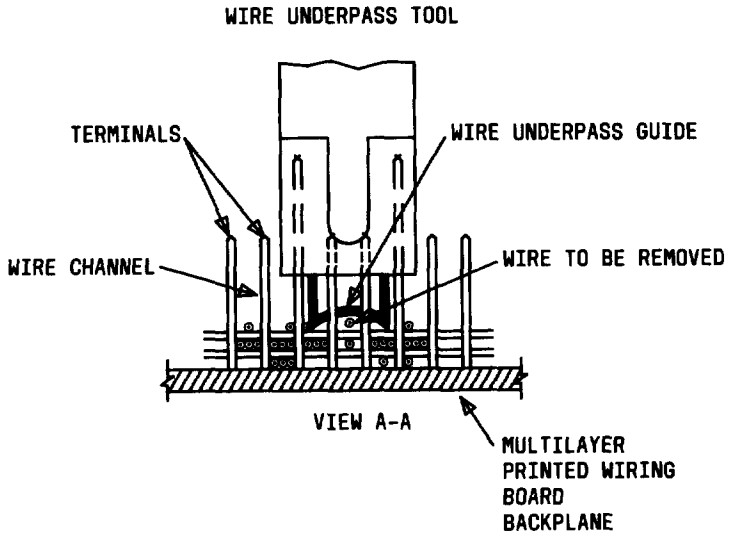
- The new wire should be positioned at the same level as occupied by the old wire. This may require the removal and replacement of wire(s) terminated above the desired wire.



IF WIRE A IS TO BE REMOVED, REPLACE WIRES A AND B.

- Sleeve any via terminal that has fewer than two wire-wrapped connections.
- Do not dress the new wire beneath wires already connected to the backplane.
- Determine the new wire length by adding the length required for each modified wire-wrap connection to the terminal-to-terminal length.
- Refer to the wiring requirements.
- Use the R-4559 probe to dress the wire.





POSITIONING OF R-4559 WIRE UNDERPASS TOOL

Fig. 3—Wire Wrap Repair Procedures (Sheet 8 of 9)

Remove Wire

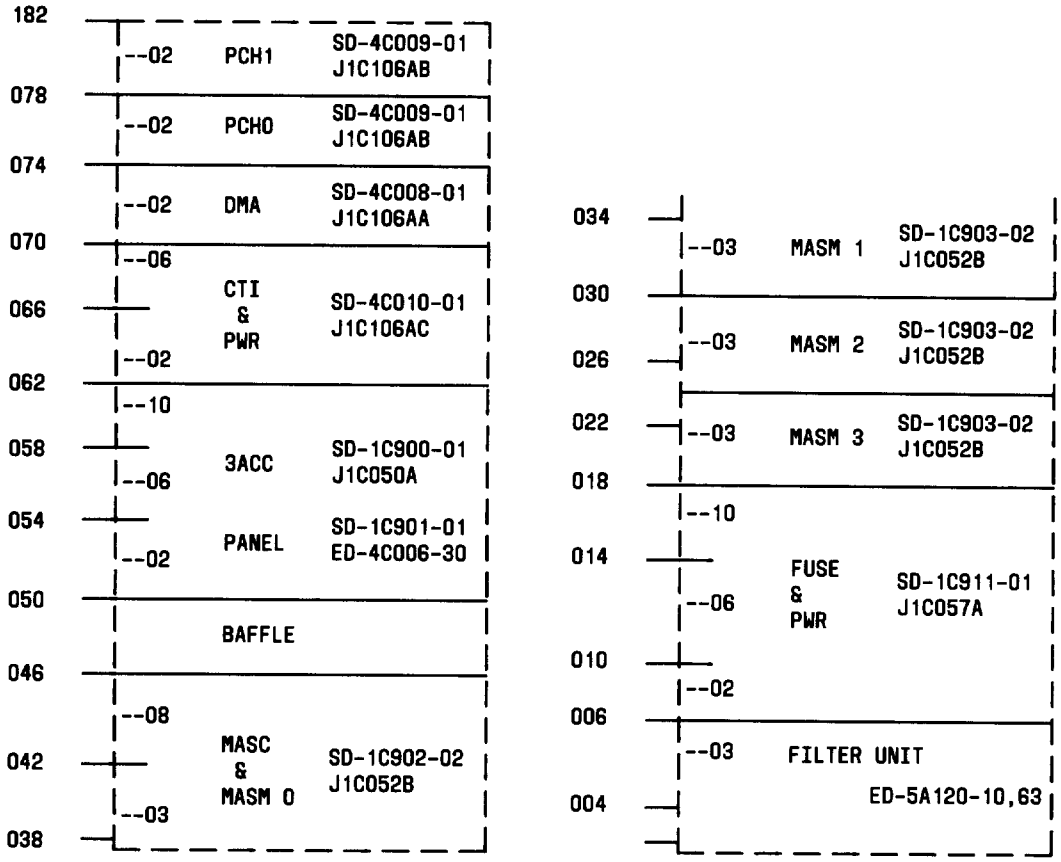
STEP	PROCEDURE
1	Locate both ends of the wire to be removed and any associated via terminals. Use the R-4475 terminal markers to flag the terminals.
2	Using the ITE-4525A tone buzzer or equivalent, verify that the correct terminals have been identified.
3	Sleeve any via terminal with a 3/4-inch length of RM-628437 teflon sleeving.
4	Place a piece of RM-583101 fiber sheeting beneath the wire to be removed.
5	Using the R-4621 wire unwrapper, unwrap the shortest wire leg first.
6	Using the hood of the wire unwrapper or the R-4107 needle-nose pliers, lift the unwrapped portion without disturbing surrounding wires to gain access to the shiner.
7	While holding the shiner with the needle-nose pliers, cut off the shiner using the 900289703 filament scissors.
8	Using the needle-nose pliers, straighten out the insulated portion of the cut-off wire end.
9	Using the wire unwrapper, unwrap the other end.
10	Position the R-4668 wire underpass tool so that the wire underpass guide is centered in the wiring channel containing the longest leg of the wire to be removed.
11	Using the tone buzzer, verify that the correct wire ends have been disconnected.
12	While holding the wire underpass tool, grasp the end of the longest wire leg with the needle-nose pliers and pull the wire out.
13	Using the recommended microscope (order No. R-4633) verify that the insulation of the surrounding wires has not been damaged.

Sleeve Via Terminal

STEP	PROCEDURE
1	Cut a 6-inch length of R-4563 polyimide sleeving.
2	Insert the sleeving over the via terminal and push it down until it rests on the multilayer printed wiring board surface.
3	Using the 900289703 filament scissors or equivalent, cut off the excess sleeving.

Fig. 3—Wire Wrap Repair Procedures (Sheet 9 of 9)

3A PROCESSOR AND MOUNTING PLATE NUMBERING



3A PROCESSOR FRAME 0

J-1C106B-1

SD-4C007-02

Fig. 4—3A Processor Frame and Mounting Plate Numbering

MAINTENANCE FRAME AND MOUNTING PLATE NUMBERING

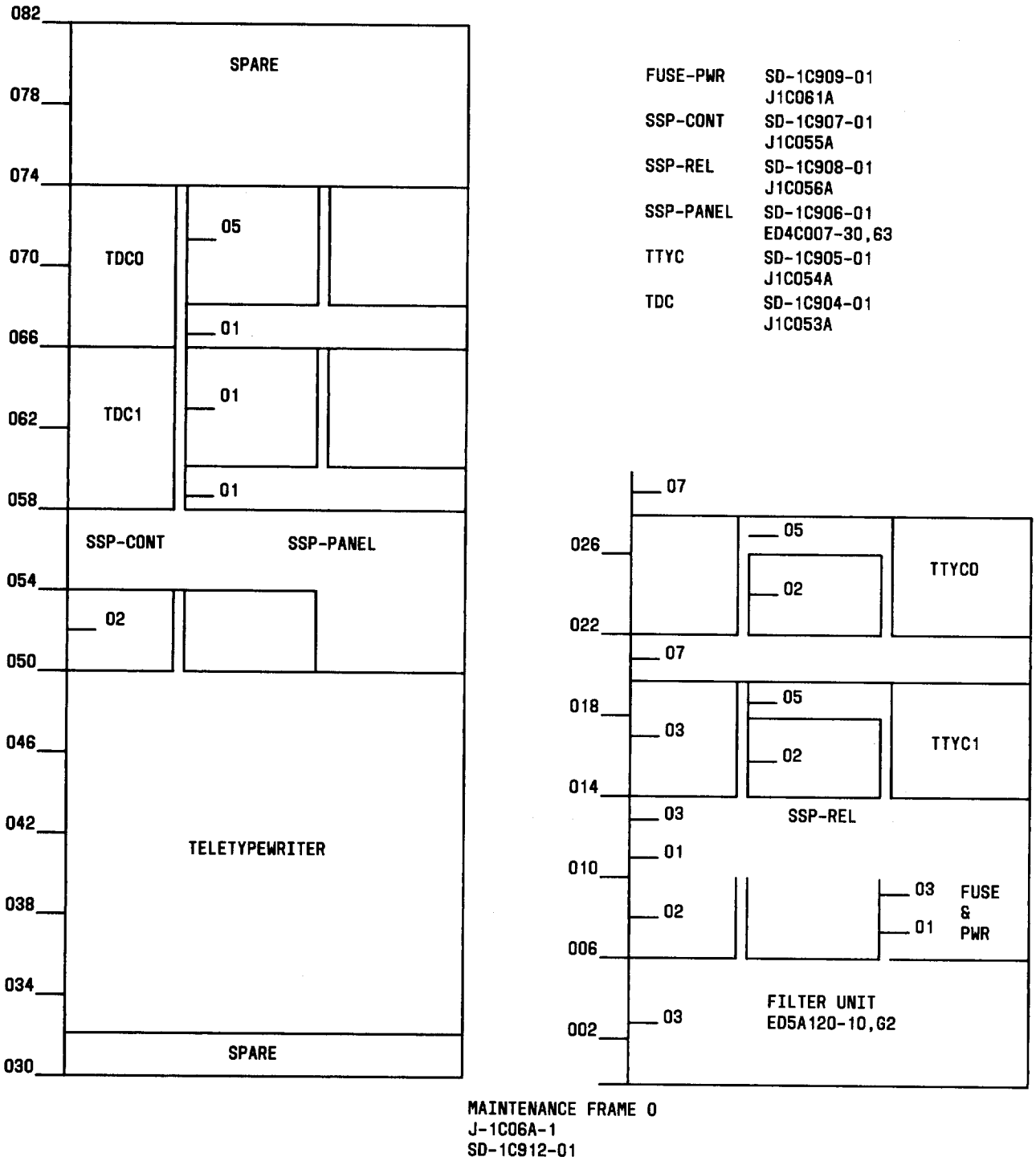
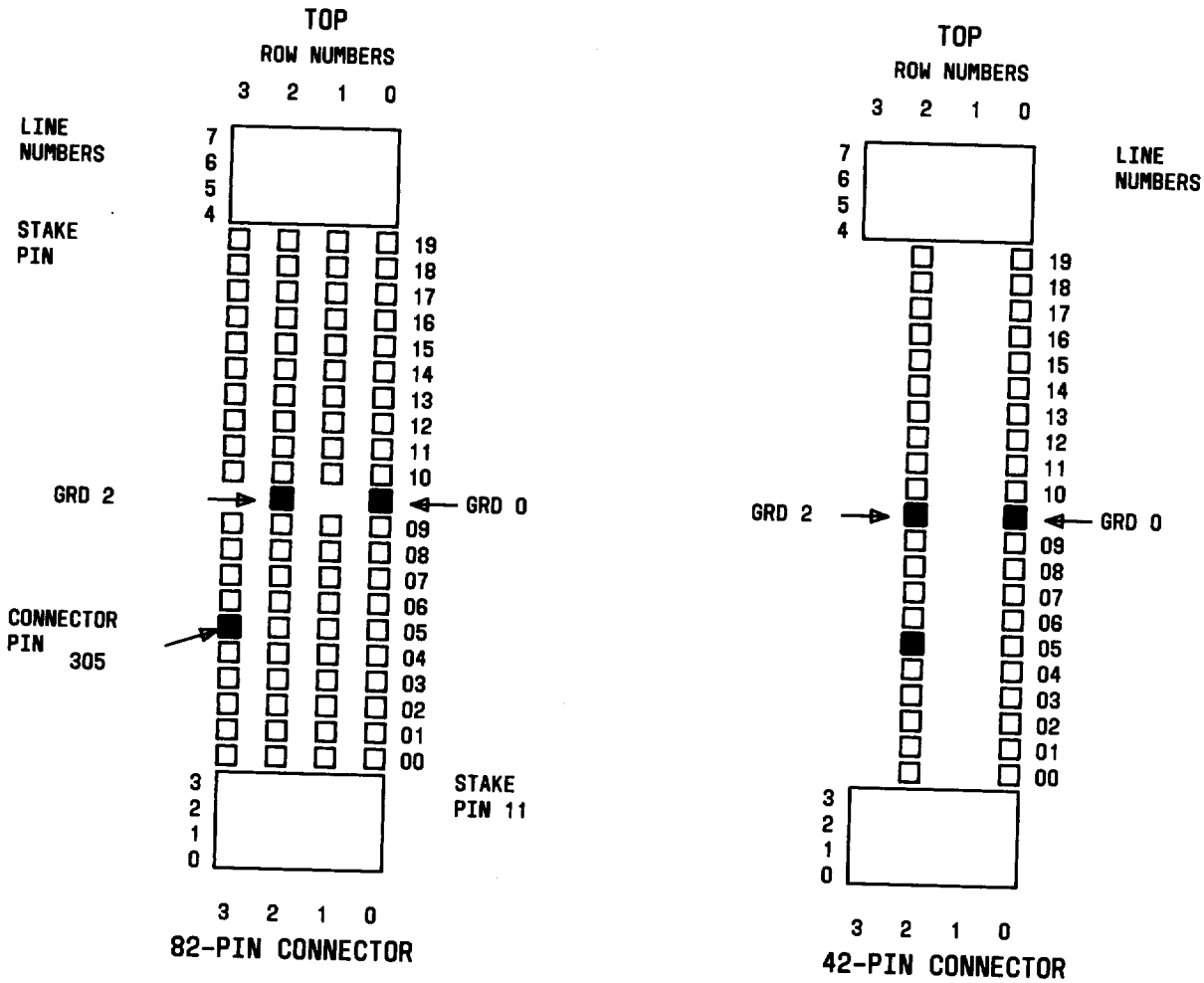


Fig. 5—Maintenance Frame Equipment and Mounting Plate Numbering



IN GENERAL, PIN REFERENCES CONSIST OF A ROW NUMBER FOLLOWED BY A LINE NUMBER

STAKE PINS
THE STAKE PINS ARE ASSIGNED LINE NUMBERS 0 THROUGH 3 (AT THE BOTTOM OF THE BOARD) AND 4 THROUGH 7 (AT THE TOP OF THE BOARD), AND ROW NUMBERS 0 THROUGH 3 (ALONG THE LONG EDGE OF THE BOARD).

CONNECTOR PINS
NOTE THAT THE TWO PINS IN THE CONNECTOR FIELD ARE CALLED GROUND (GND) PINS. ONE IS IN ROW 0 AND THE OTHER IS IN ROW 2. ALL THE OTHER PINS ARE IN ROWS 0 THROUGH 3 (82 PIN CONNECTOR) OR ROWS 0 AND 2 (42 PIN CONNECTOR), AND LINES 00 THROUGH 19.

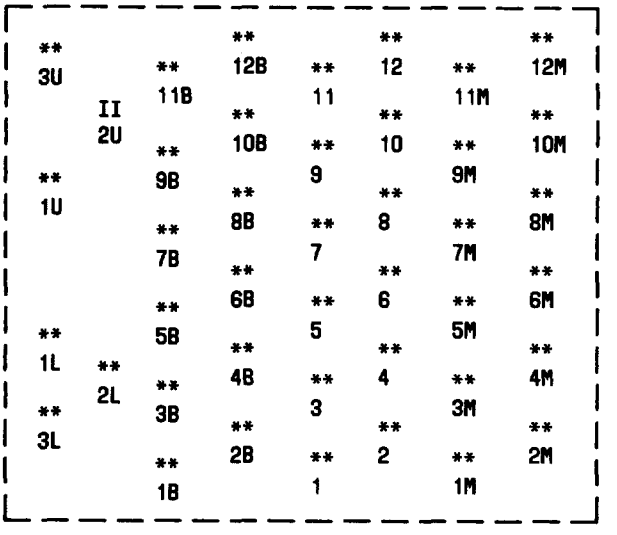
FIND A PIN
GO ACROSS TO THE APPROPRIATE ROW NUMBER AND THEN DOWN TO THE APPROPRIATE LINE NUMBER

EXAMPLES
STAKE PIN 34: PIN AT ROW 3, LINE 4 (TOP). 82 PIN CONNECTOR
CONNECTOR PIN 306: PIN AT ROW 3, LINE 05

CONNECTOR PIN 206: PIN AT ROW 2, LINE 06 42 PIN CONNECTOR

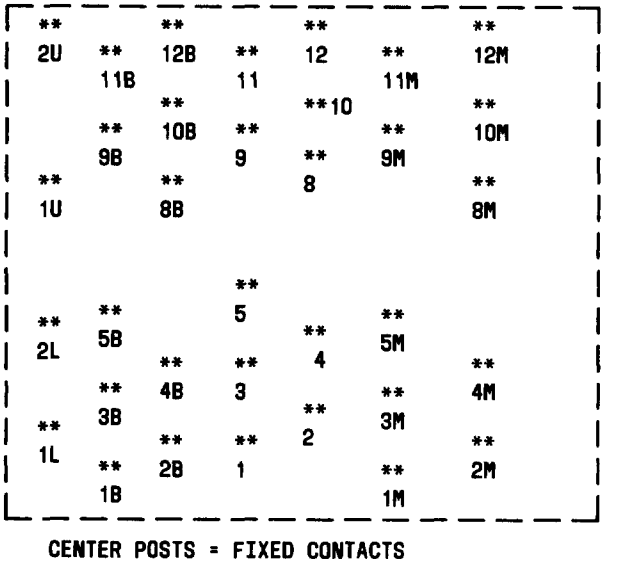
Fig. 6—947-Type Connector Pin Numbering

AF, AG, AJ, AL TYPE RELAYS (12 POSITION)
WIRING AND SPRING TERMINAL ARRANGEMENT



CENTER POSTS = FIXED CONTACTS
M = MAKE CONTACTS
B = BREAK CONTACTS
L = LOWER WINDING TERMINAL
U = UPPER WINDING TERMINAL

AK AND AM TYPE RELAYS
WIRING AND SPRING TERMINAL ARRANGEMENT



CENTER POSTS = FIXED CONTACTS
M = MAKE CONTACTS
B = BREAK CONTACTS
L = LOWER WINDING TERMINAL
U = UPPER WINDING TERMINAL

Fig. 7—Relay Contact Numbering

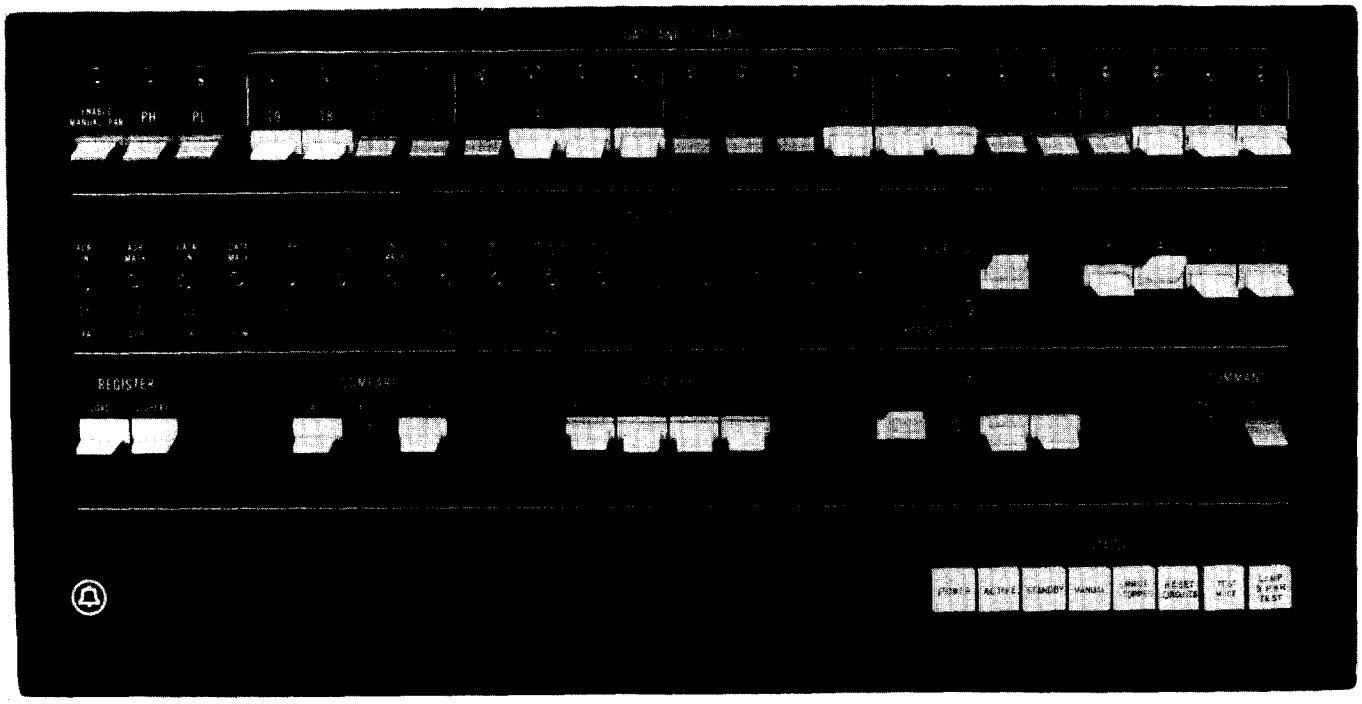


Fig. 8—3A CC Control Panel

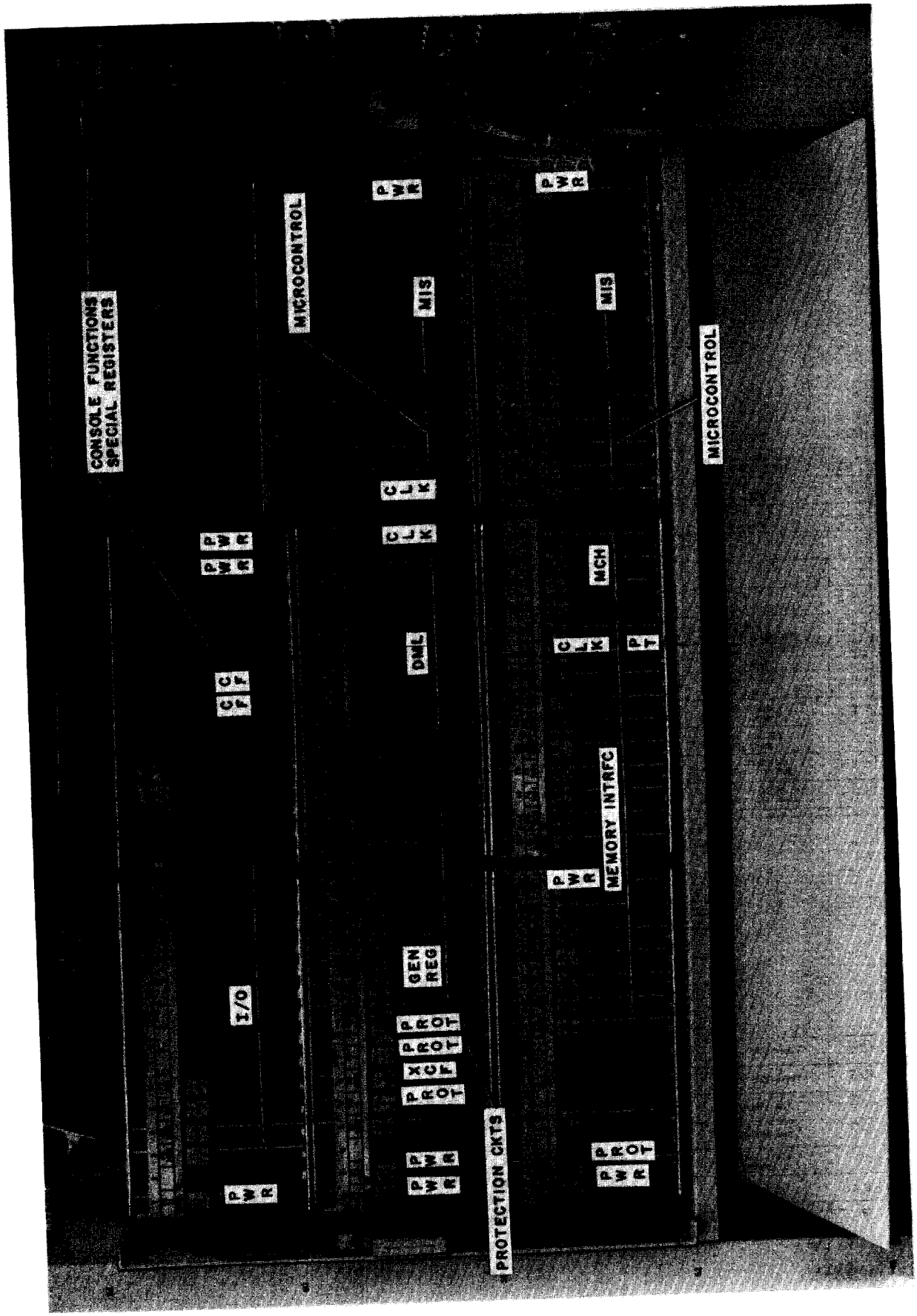


Fig. 9—3A CC Interior

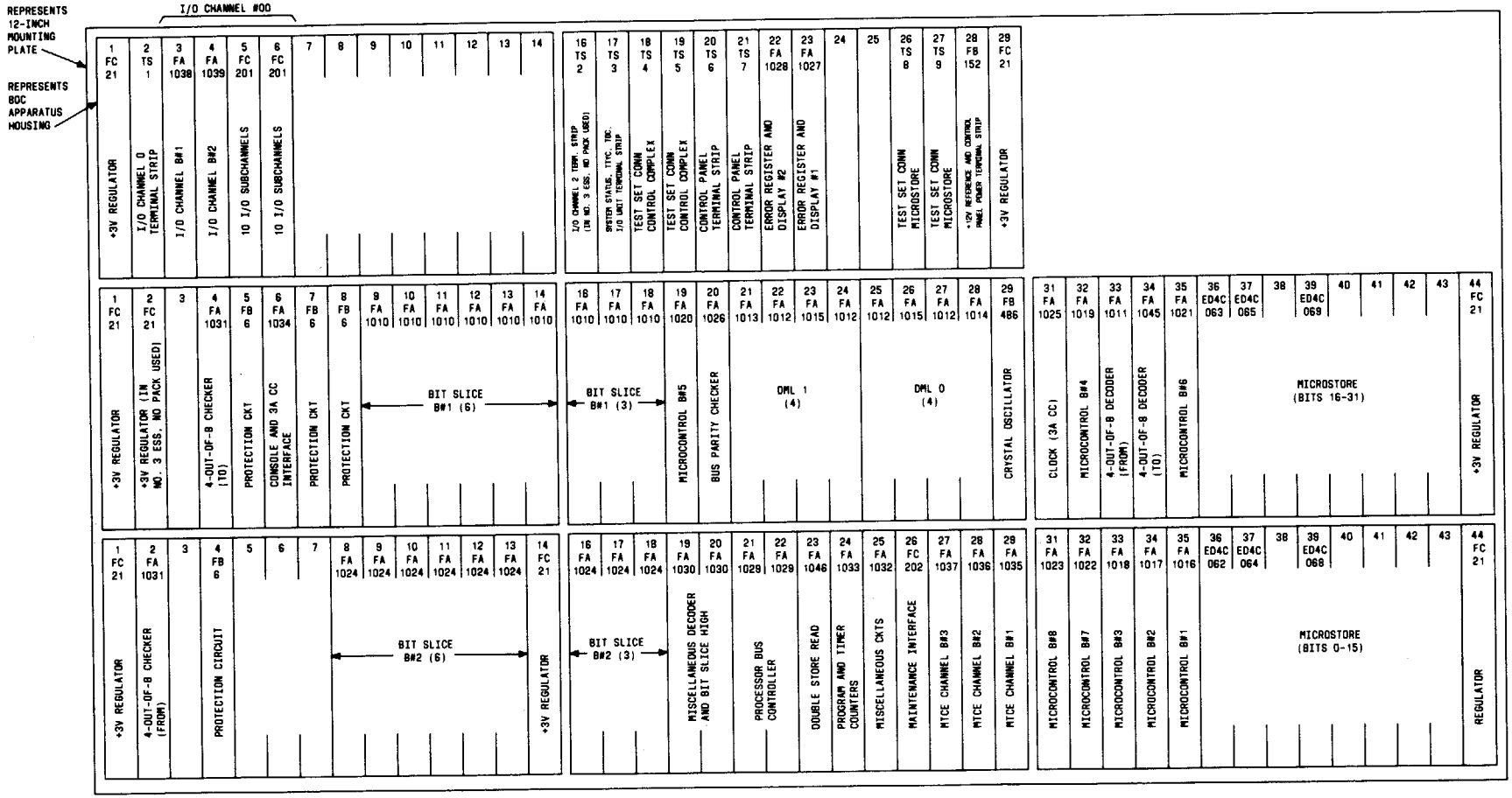
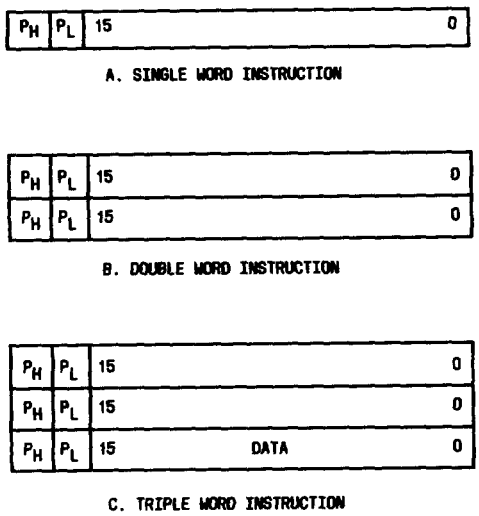


Fig. 10—3A CC Circuit Pack Locations



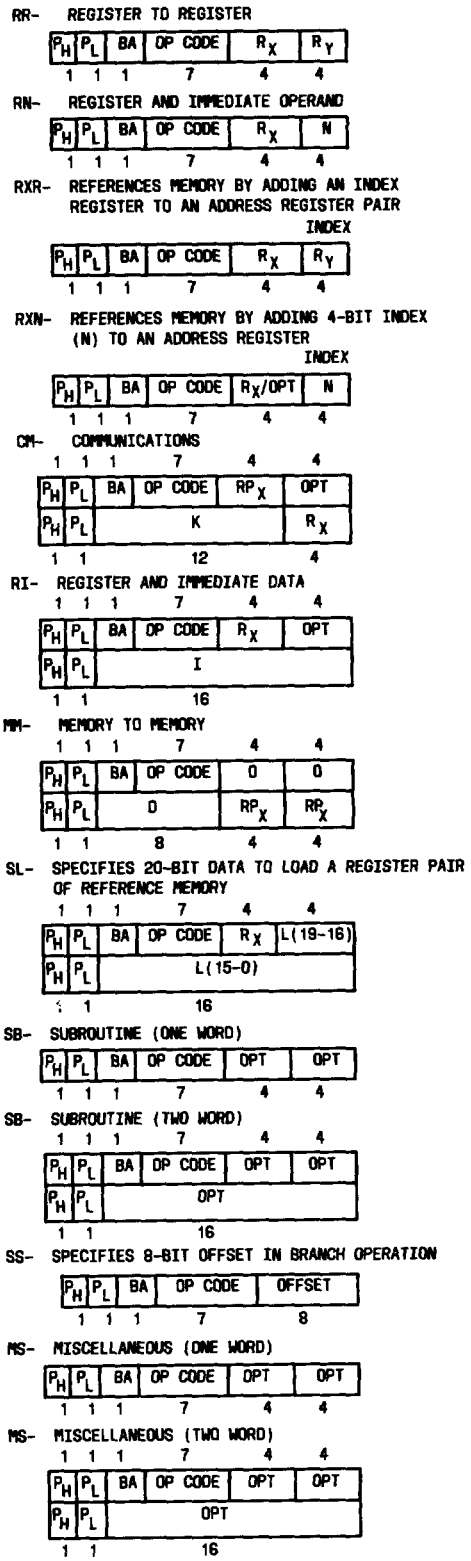


Fig. 11—3A CC Instruction Set Layouts

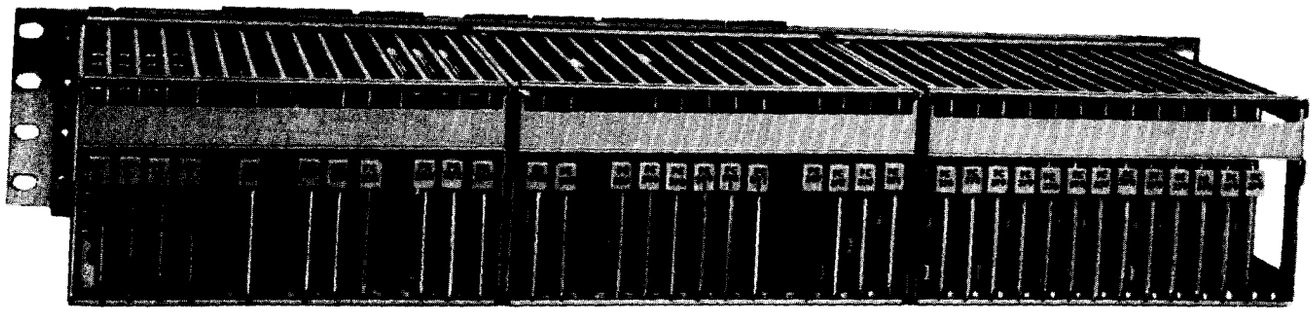


Fig. 12—DMA Unit

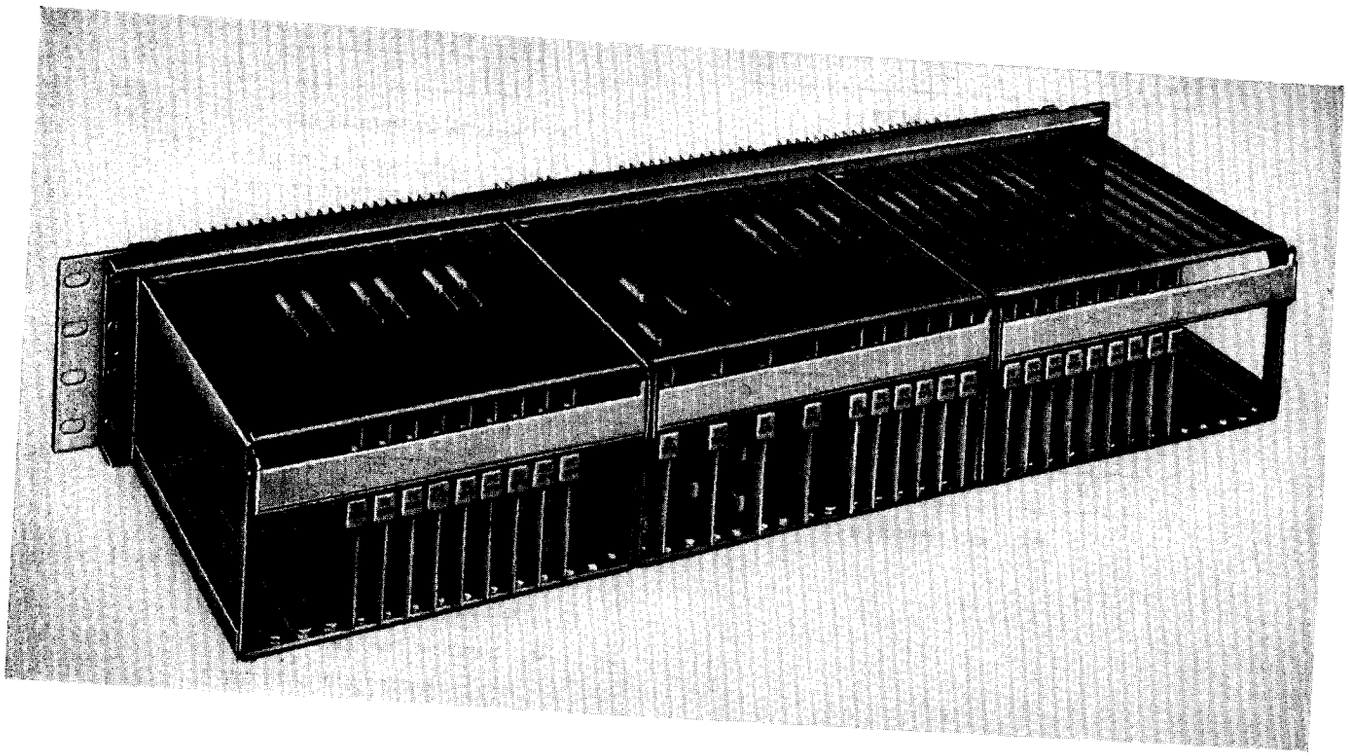


Fig. 13—PCH Unit

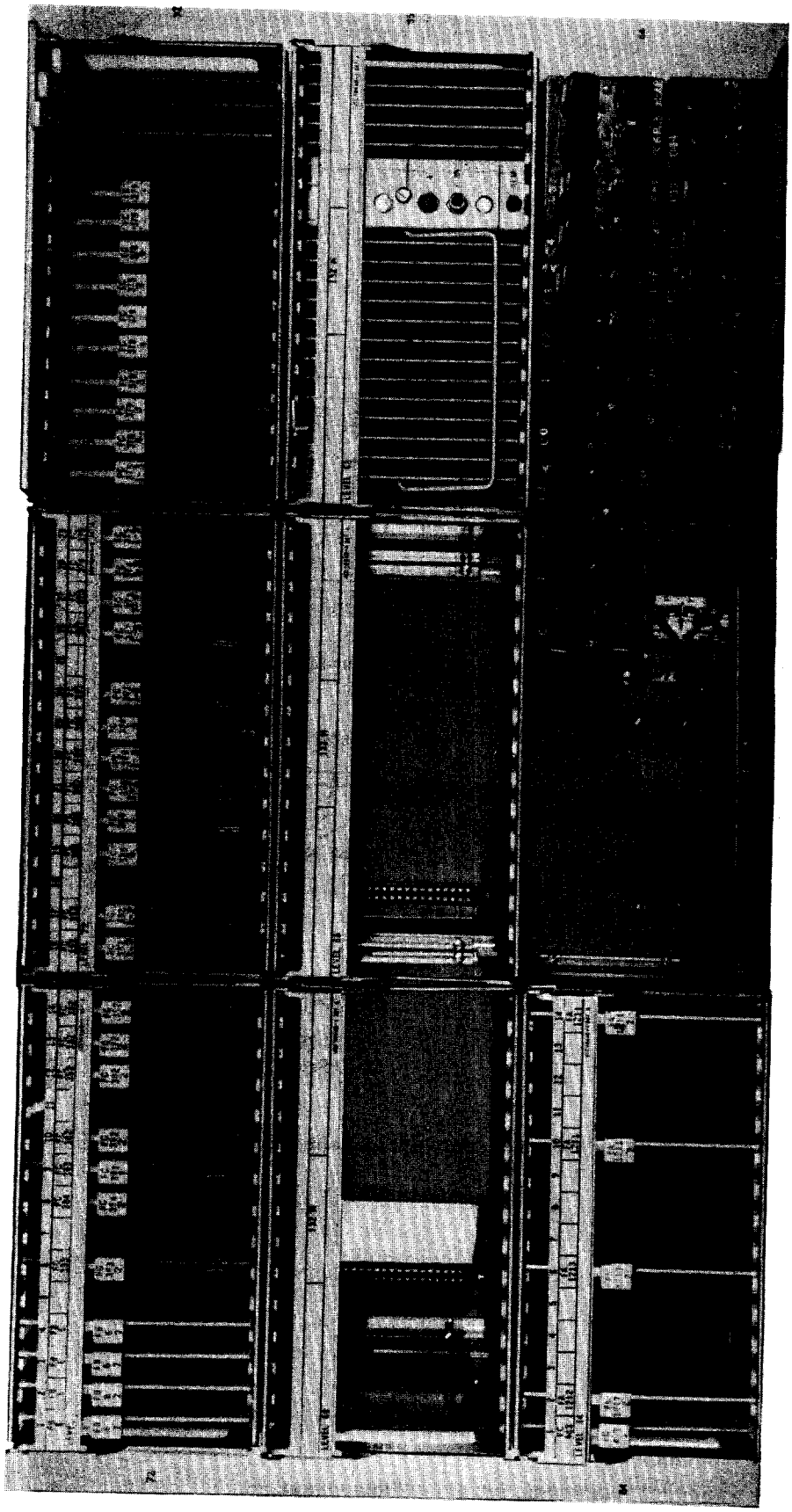


Fig. 14—CTI/Power Unit

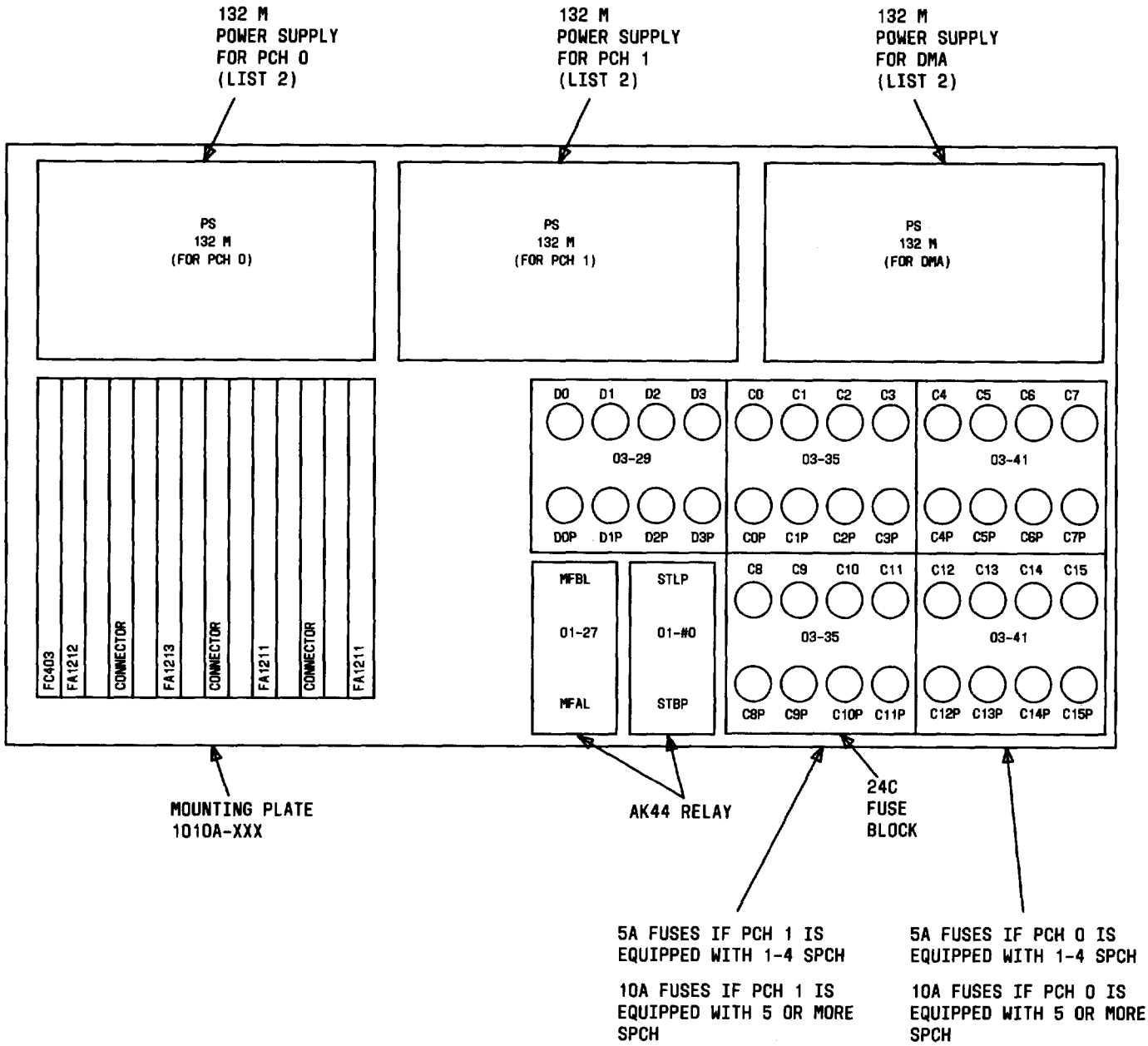
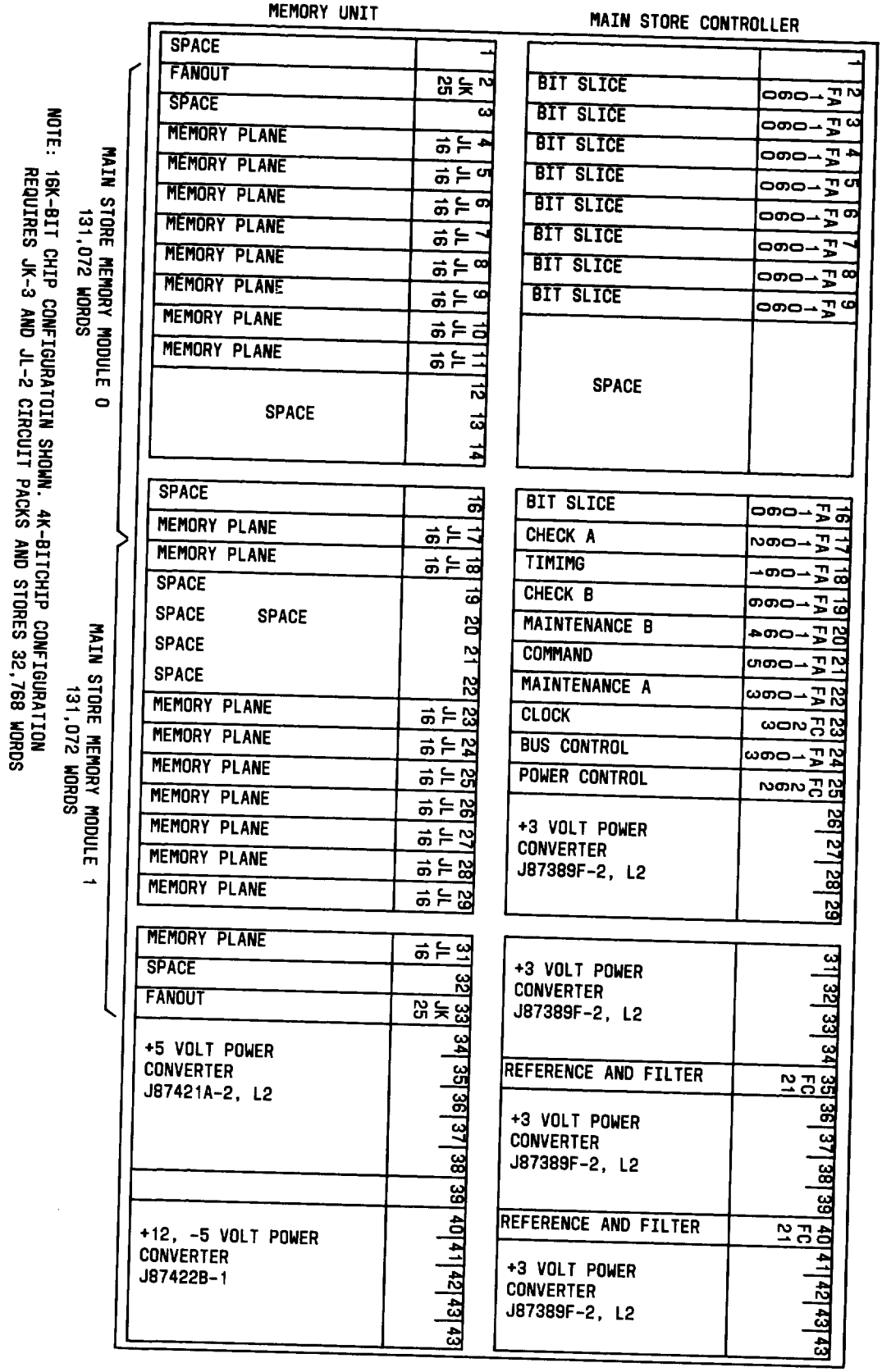


Fig. 15—CTI/Power Unit Component Locations



NOTE: 16K-BIT CHIP CONFIGURATOIN SHOWN. 4K-BITCHIP CONFIGURATION REQUIRES JK-3 AND JL-2 CIRCUIT PACKS AND STORES 32,768 WORDS

Fig. 16—MASC and Memory Unit Circuit Pack Locations

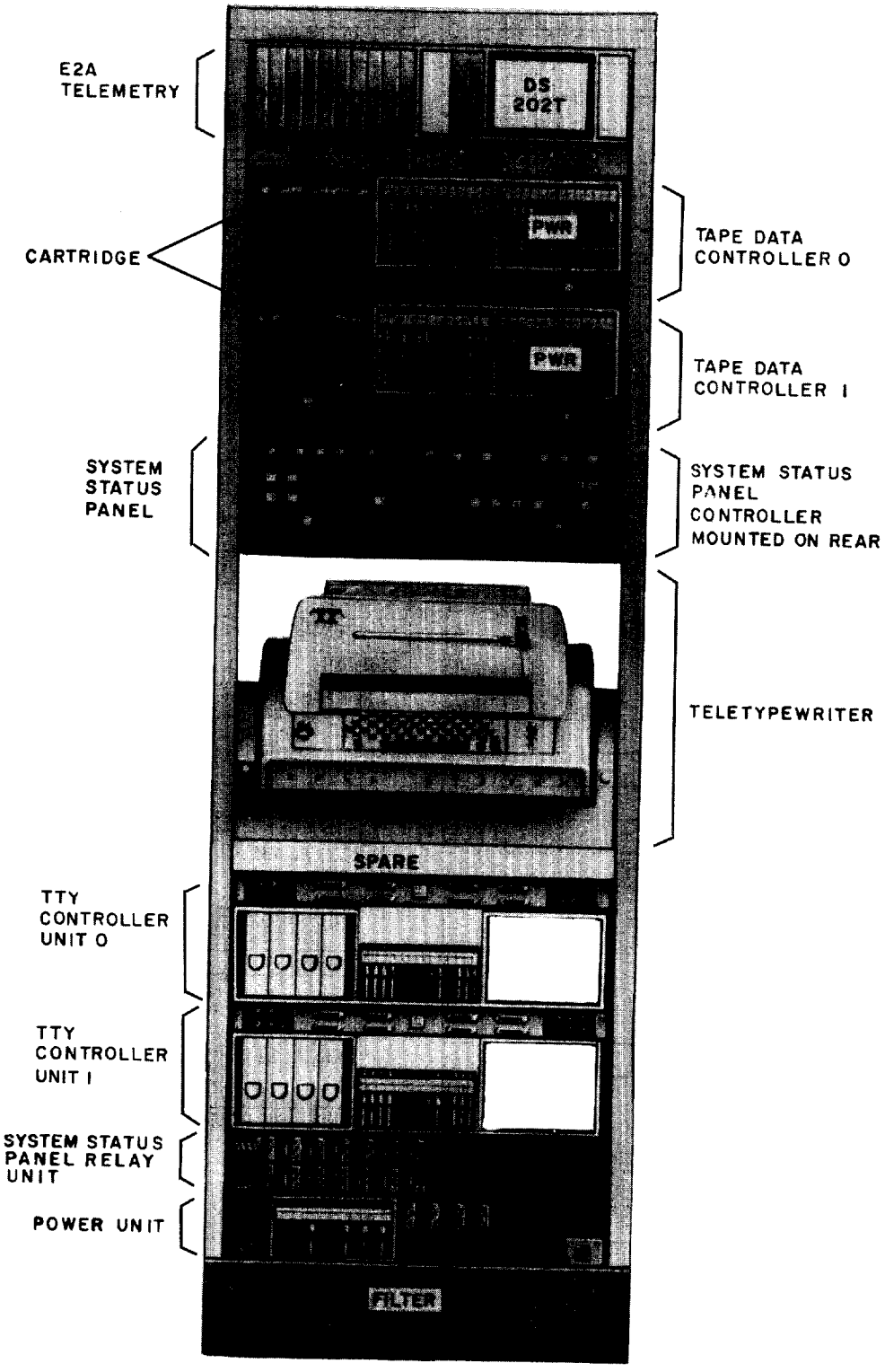


Fig. 17—Maintenance Frame

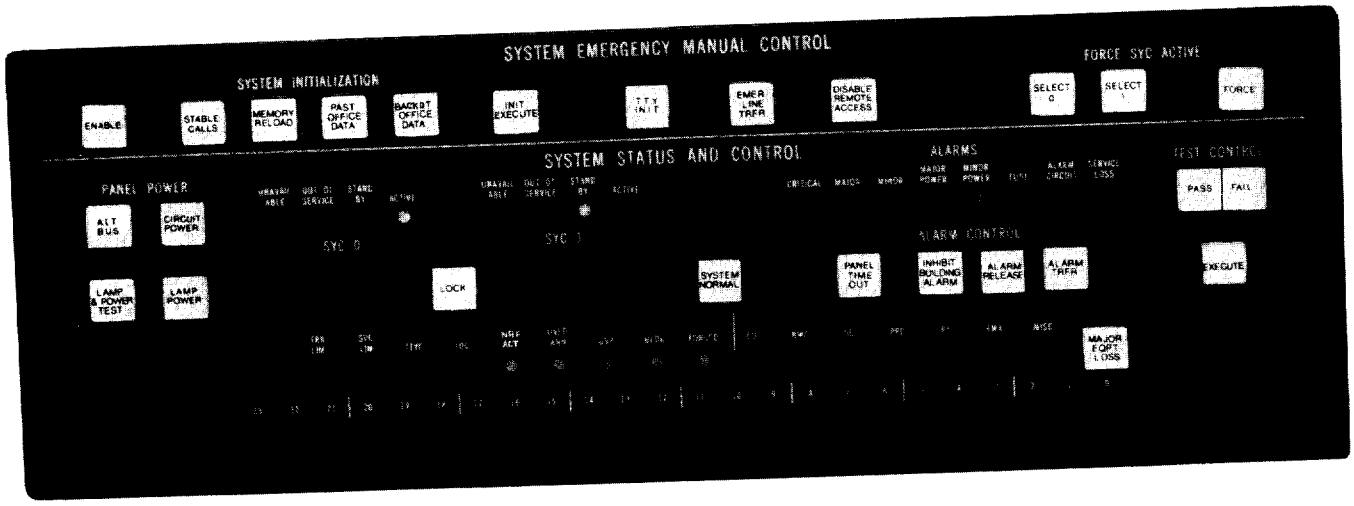


Fig. 18—System Status Panel (No. 3 ESS)

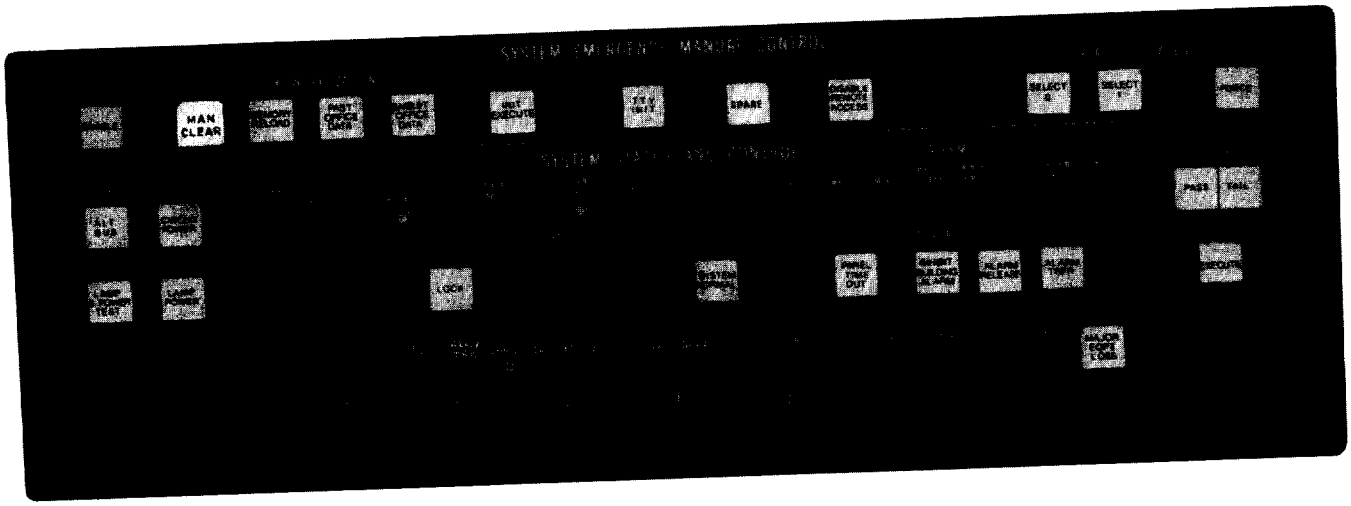


Fig. 19—System Status Panel (TNS)

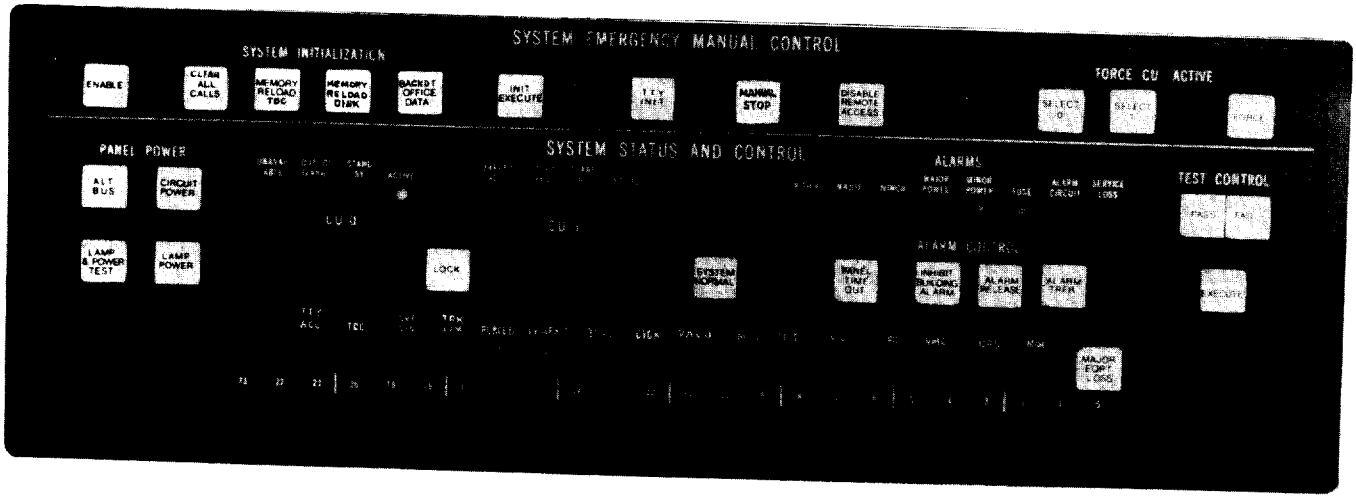


Fig. 20—System Status Panel (No. 5 ETS)

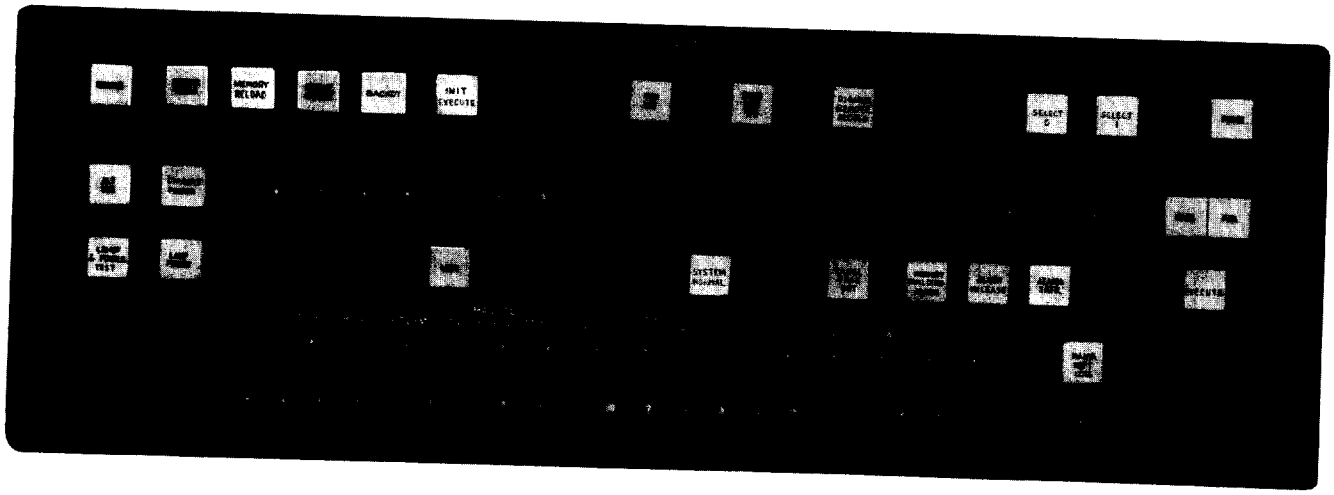
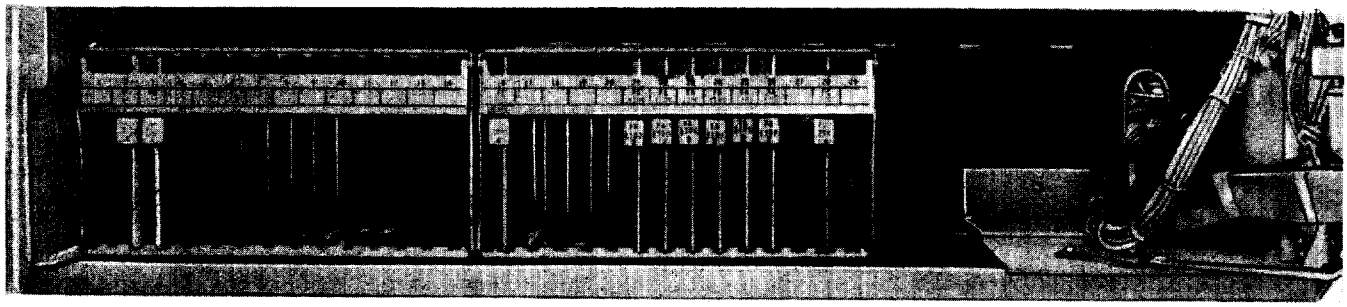
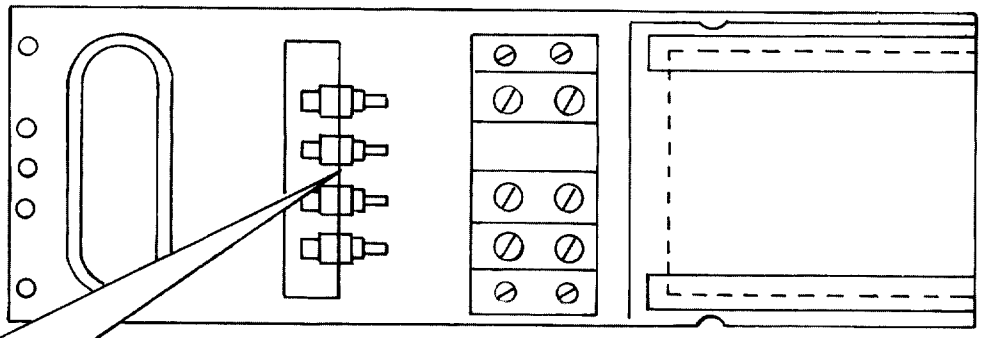


Fig. 21—System Status Panel (No. 2B ESS)



FRONT VIEW



REAR VIEW

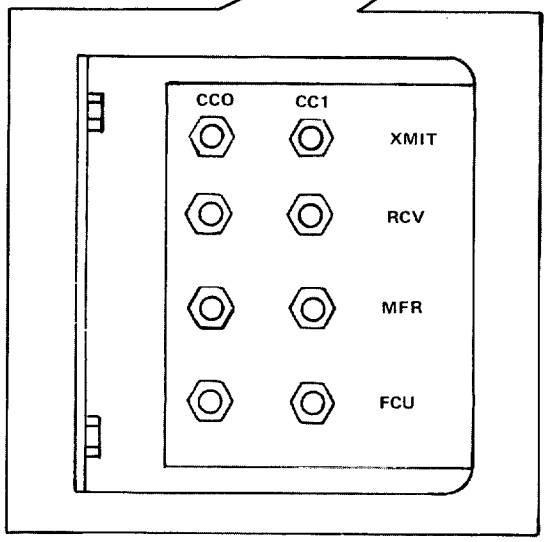


Fig. 22—System Status Panel Controller

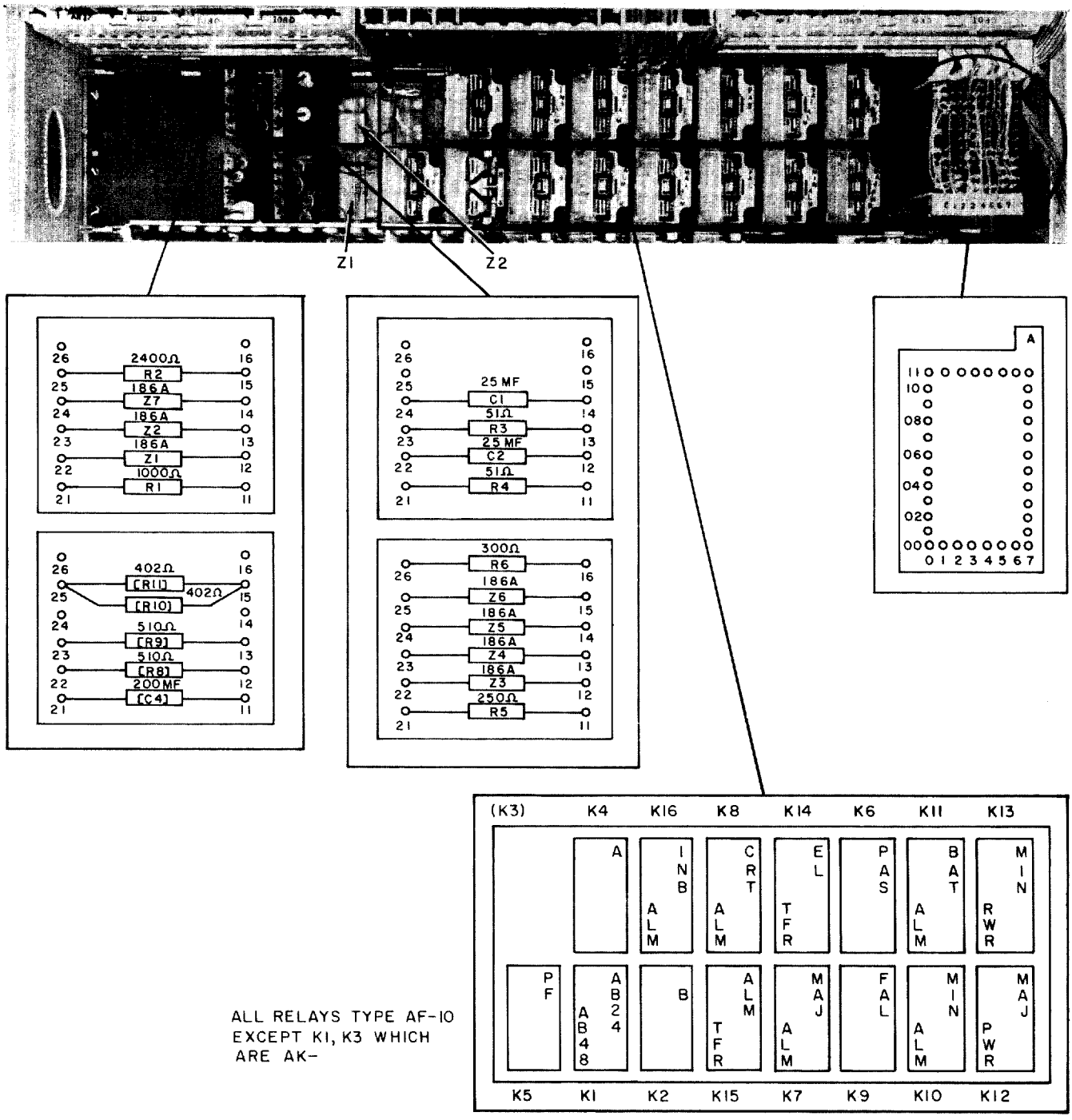


Fig. 23—System Status Panel and Relay Unit

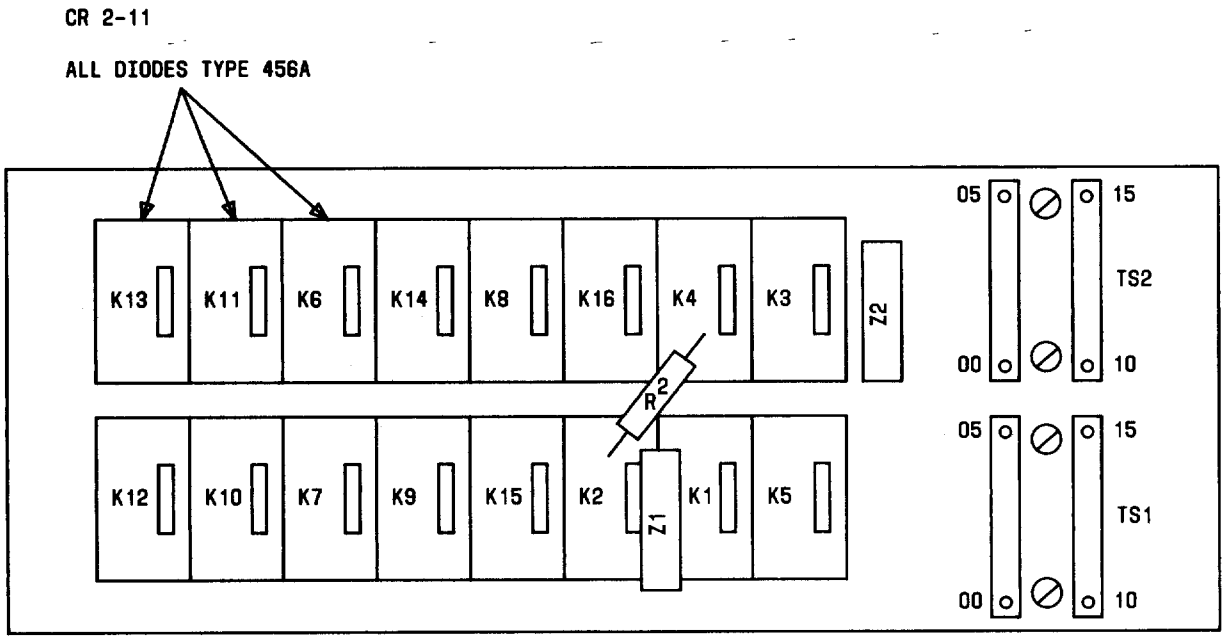
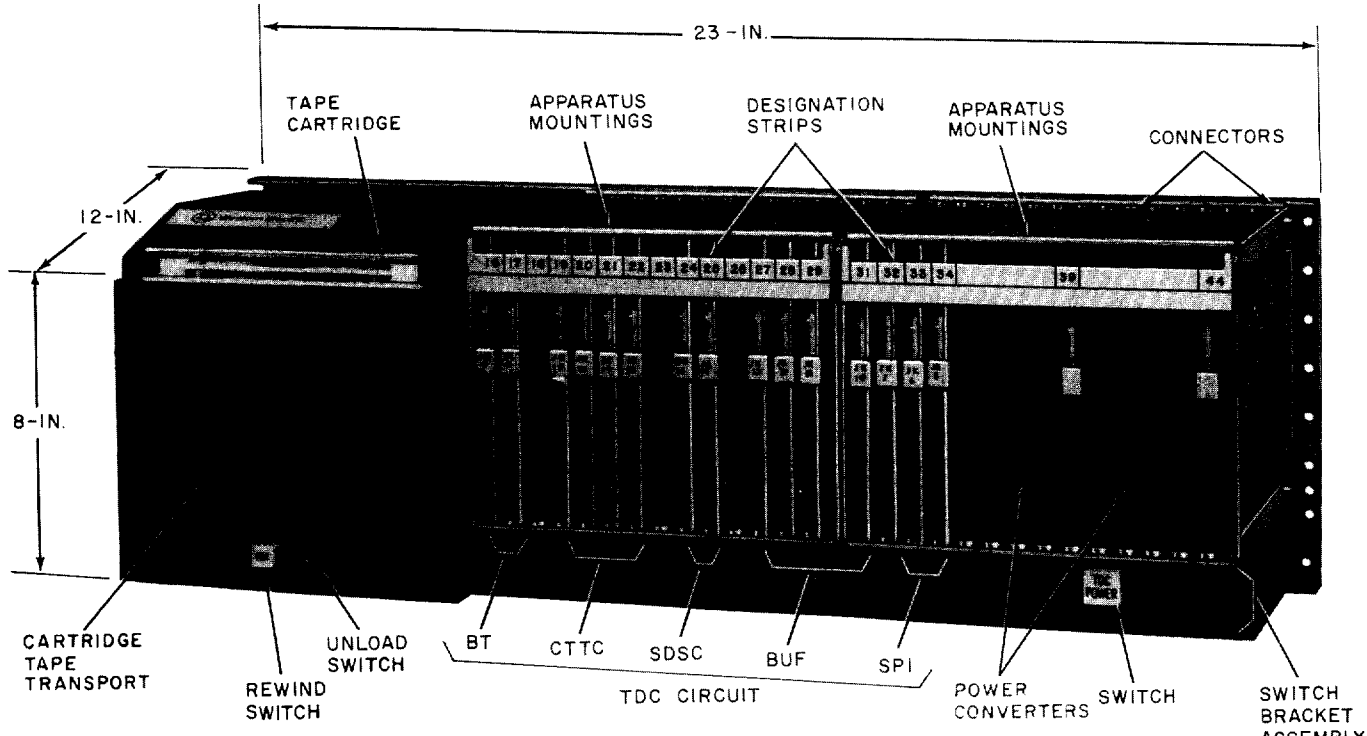


Fig. 24—System Status Panel and Relay Unit, Rear View



ABBREVIATIONS

BUF-BUFFER
BT-BUS TERMINATOR
CTTC-CARTRIDGE TAPE TRANSPORT CONTROLLER
SDSC-SYNCHRONOUS DATA SET CONTROLLER
SPI-SERIAL PERIPHERAL INTERFACE

Fig. 25—Tape Data Controller 0 or 1, Front View

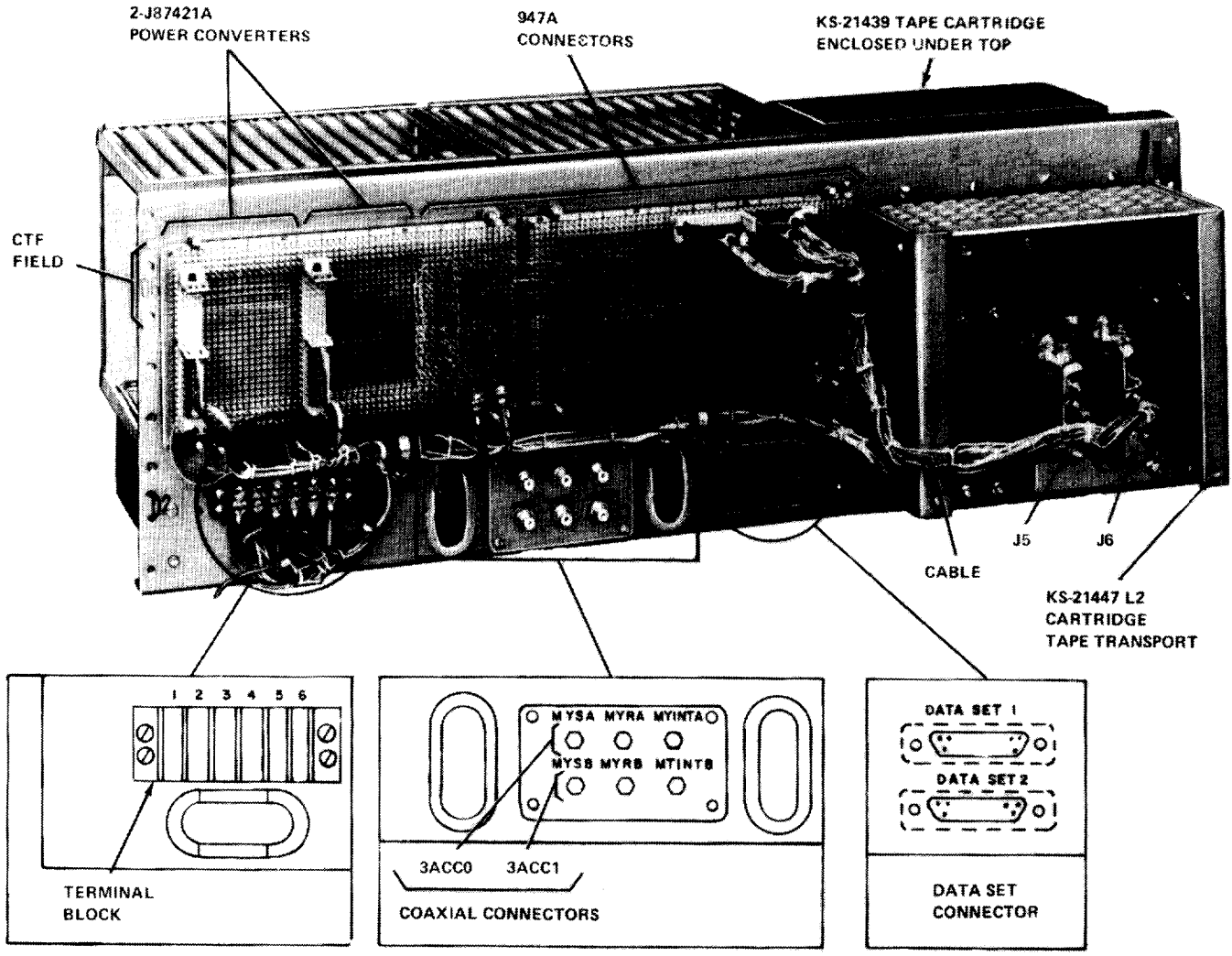


Fig. 26—Tape Data Controller 0 or 1, Rear View

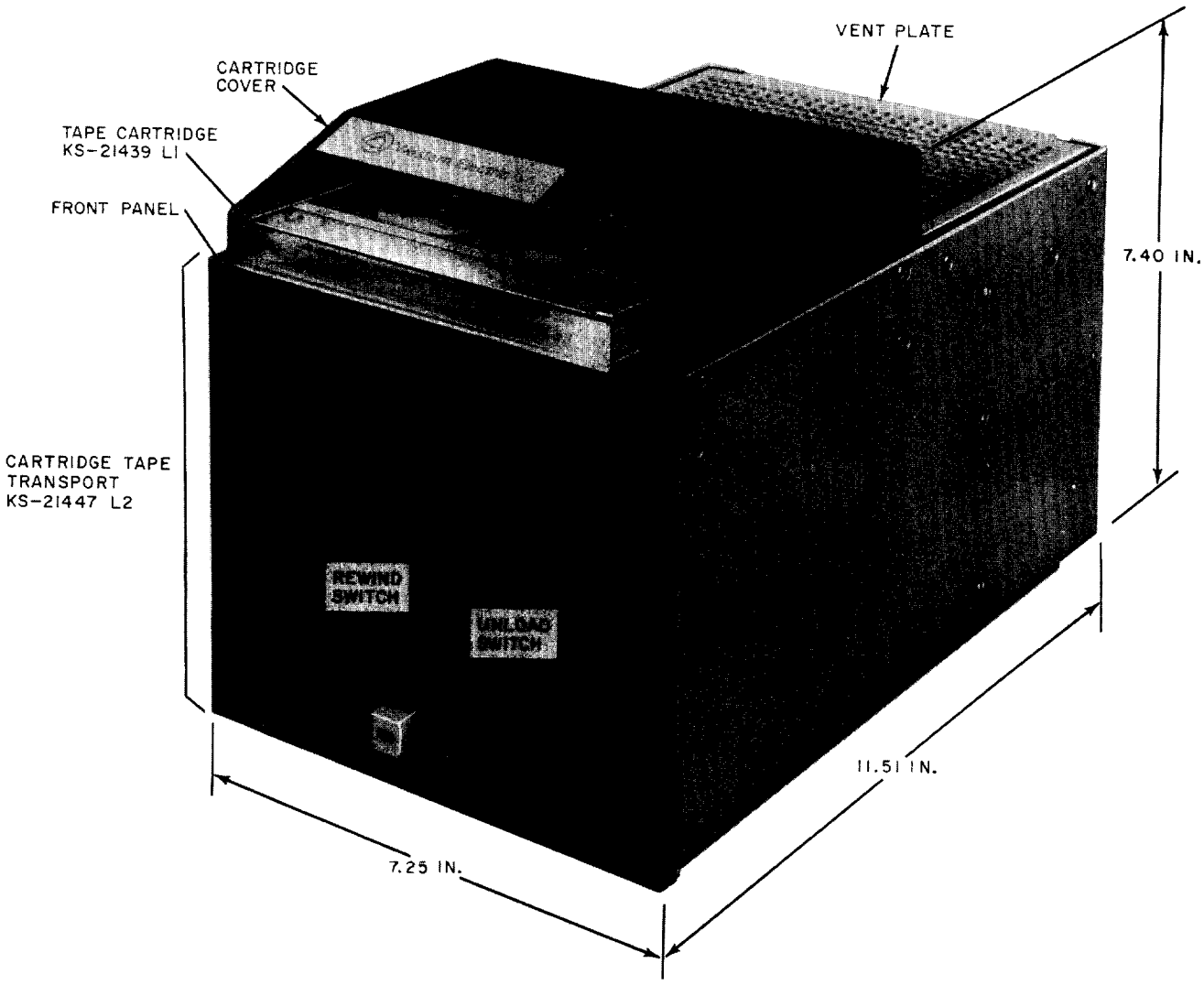


Fig. 27—Cartridge Tape Transport KS-21447, L2

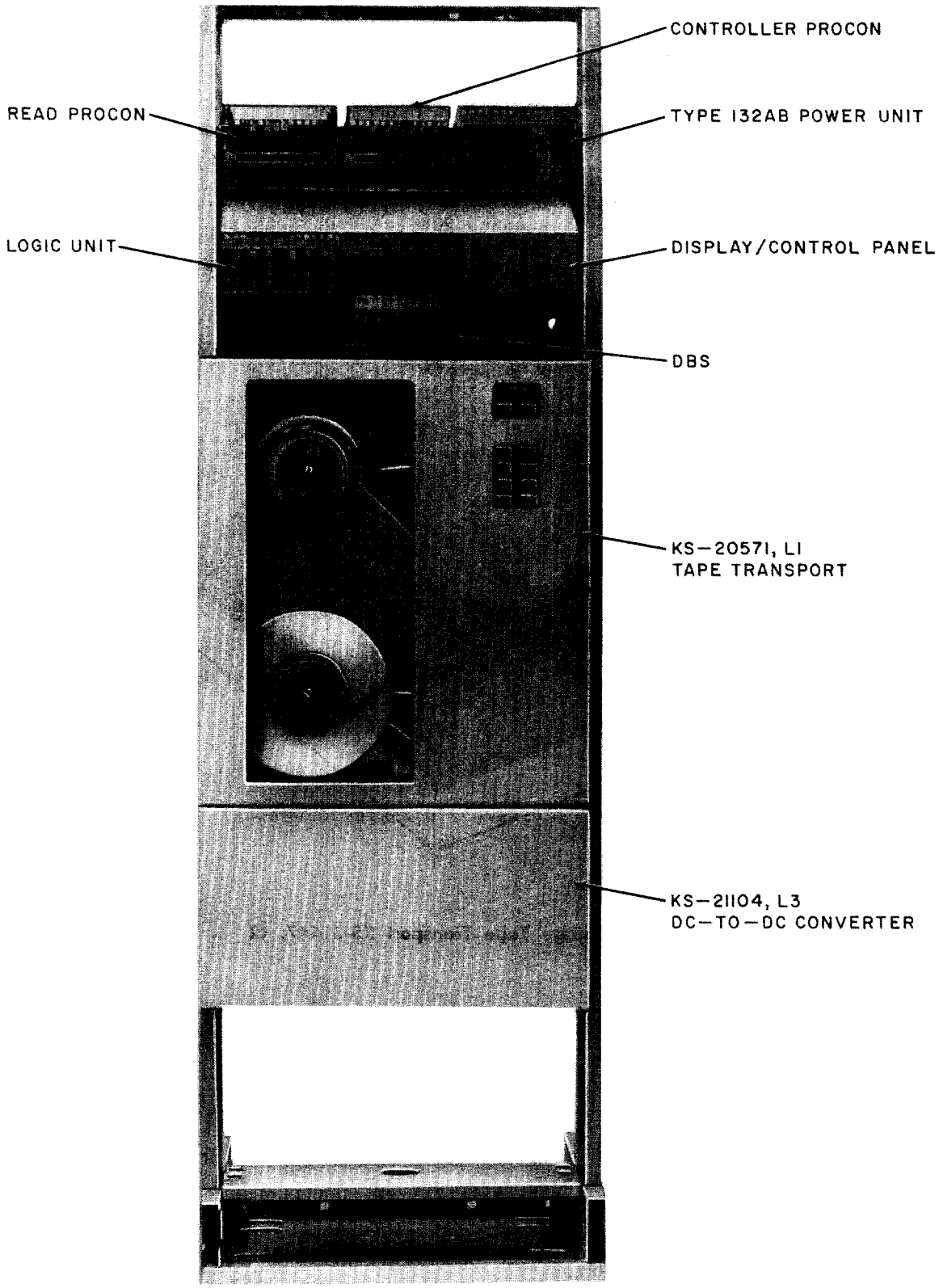


Fig. 28—PROMATS Frame

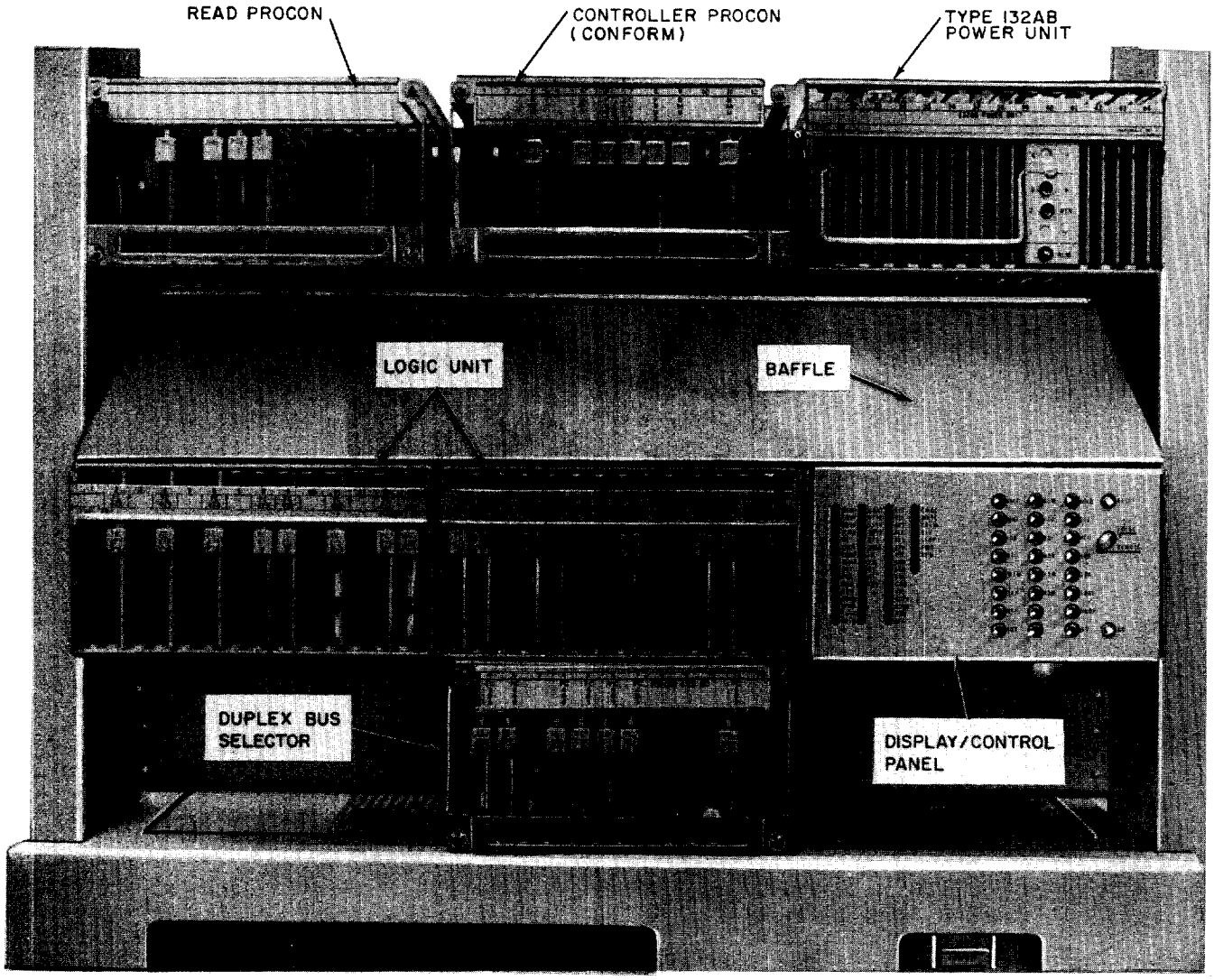


Fig. 29—PROMPTS Frame, Upper Section

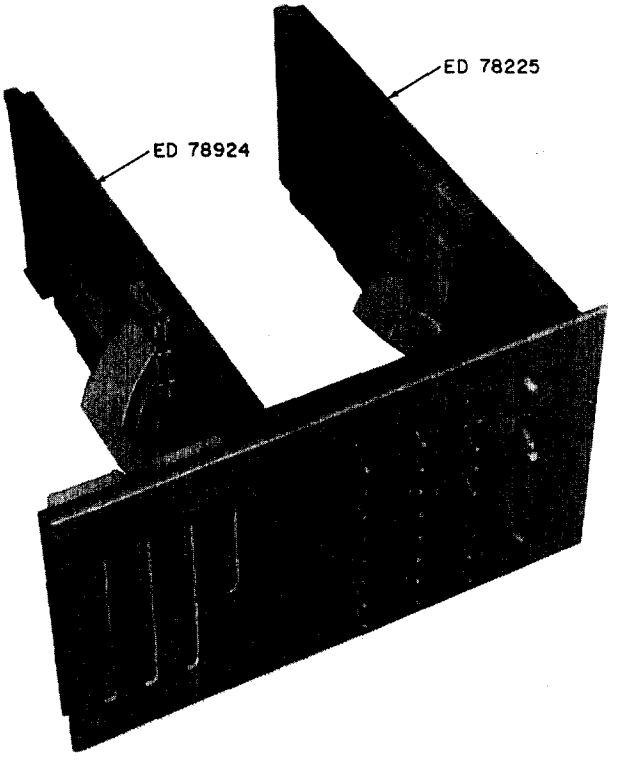


Fig. 30—Display Control Panel Front View

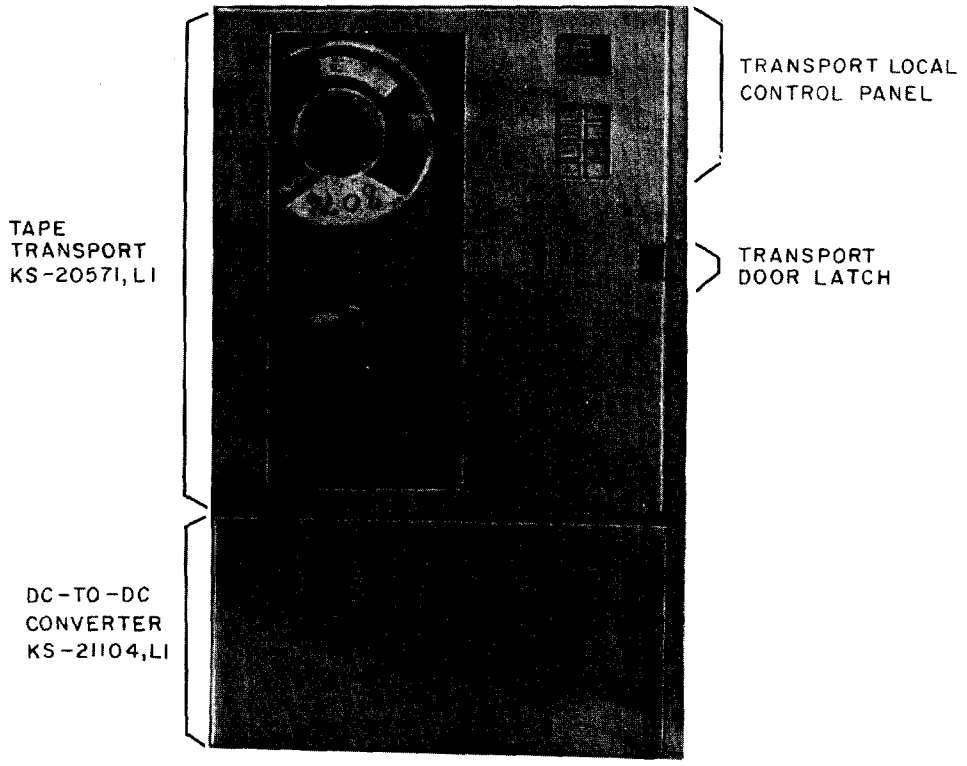


Fig. 31—Tape Transport and Power Supply

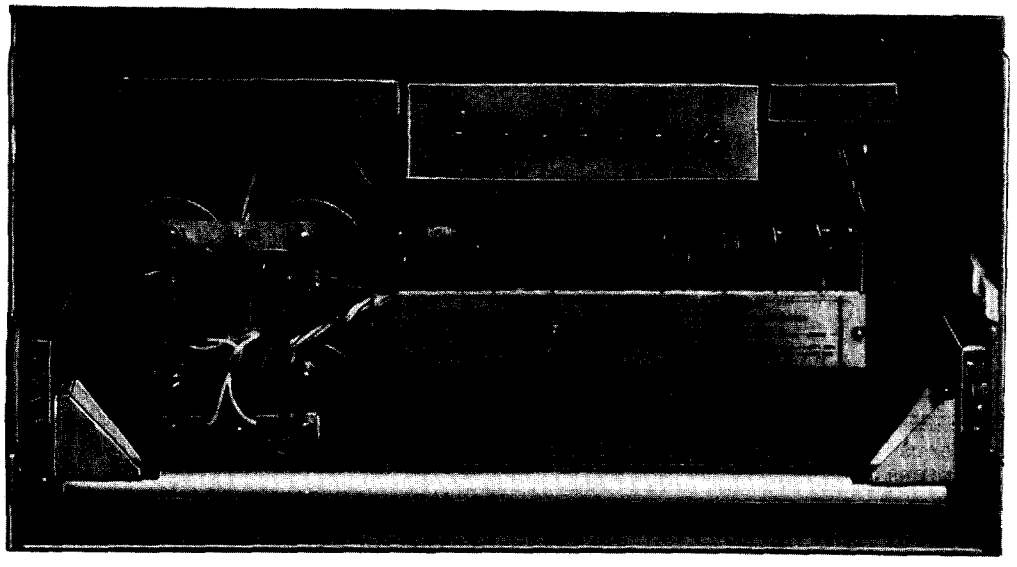


Fig. 32—Power Supply KS-21104, L3 Interior View

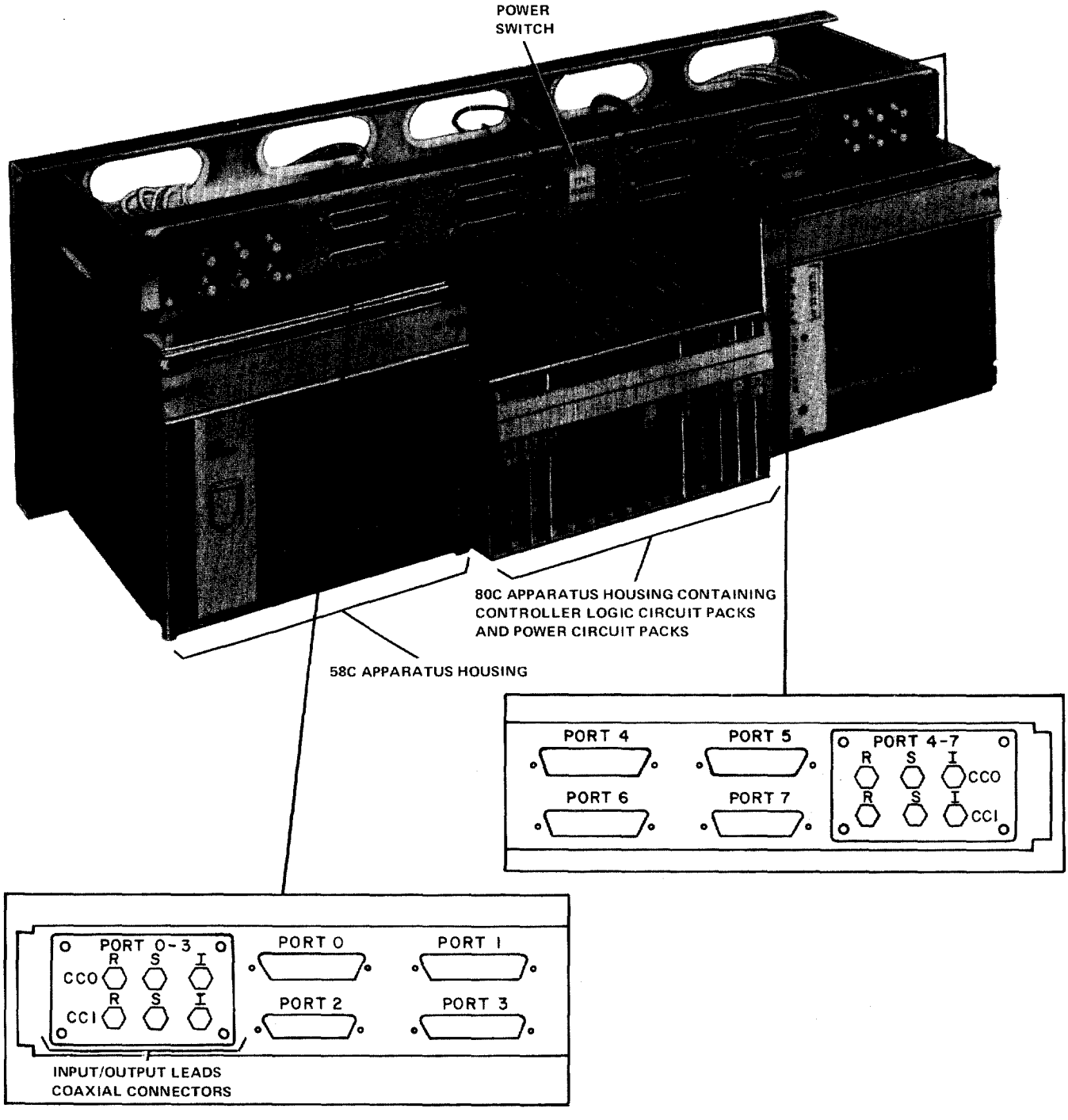
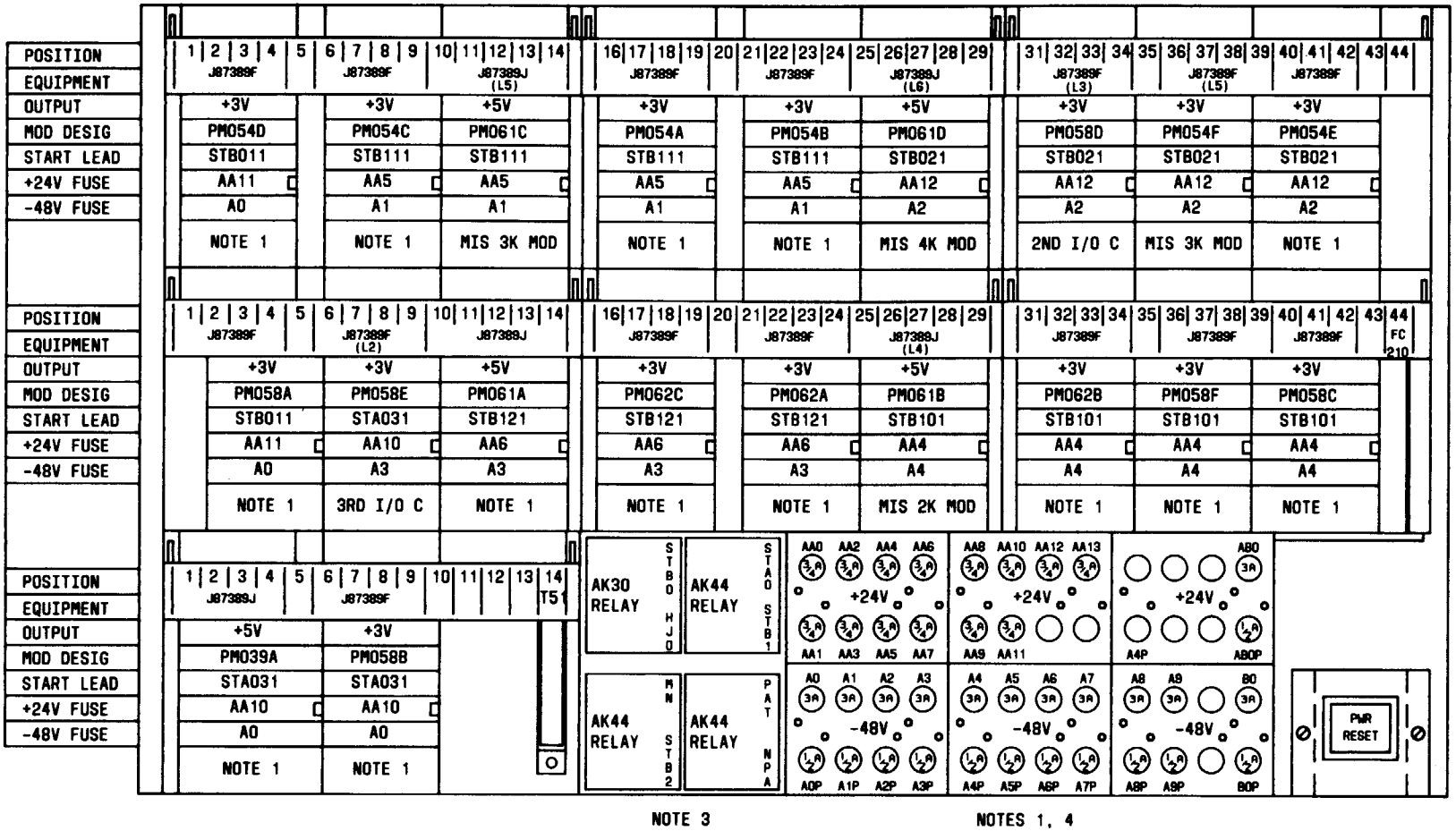


Fig. 33—Teletypewriter Controller J1C054A



NOTES:

1. FOR DISTRIBUTION OF THE PROCESSOR FRAME POWER UNIT, REFER TO TABLE CX, PROCESSOR FRAME FUSE ASSIGNMENT.
2. EQUIPMENT LOCATIONS 02, 06, AND 10 DESIGNATE VERTICAL LOCATIONS ON THE PROCESSOR FRAME POWER UNIT. CORRESPONDING FRAME EQLs ARE 08, 14, AND 16.
3. THE START LEADS ARE ASSOCIATED WITH RELAYS STA0, STB0, STB1, AND STB2.
4. FUSE AMPERE RATINGS AND TYPE RESPECTIVELY ARE AS FOLLOWS: 1/2 AMP, TYPE 70G; 3/4 AMP, TYPE 70H; 3 AMP, FAST BLOW. THE 1/2 AMP FUSES ARE PILOT FUSES.

Fig. 34—Processor Frame Power Unit

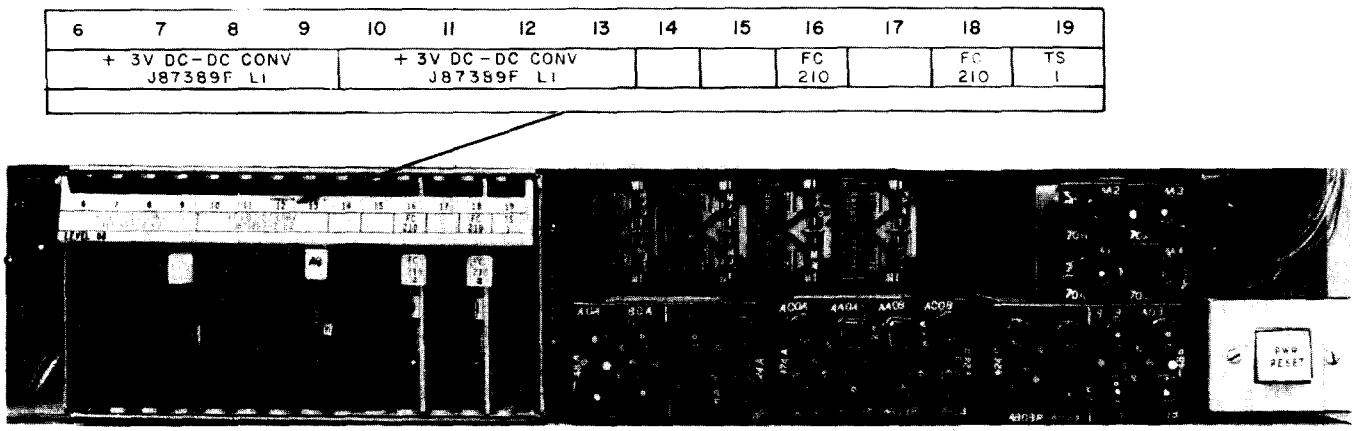


Fig. 35—Maintenance Frame Power Unit J1C061A

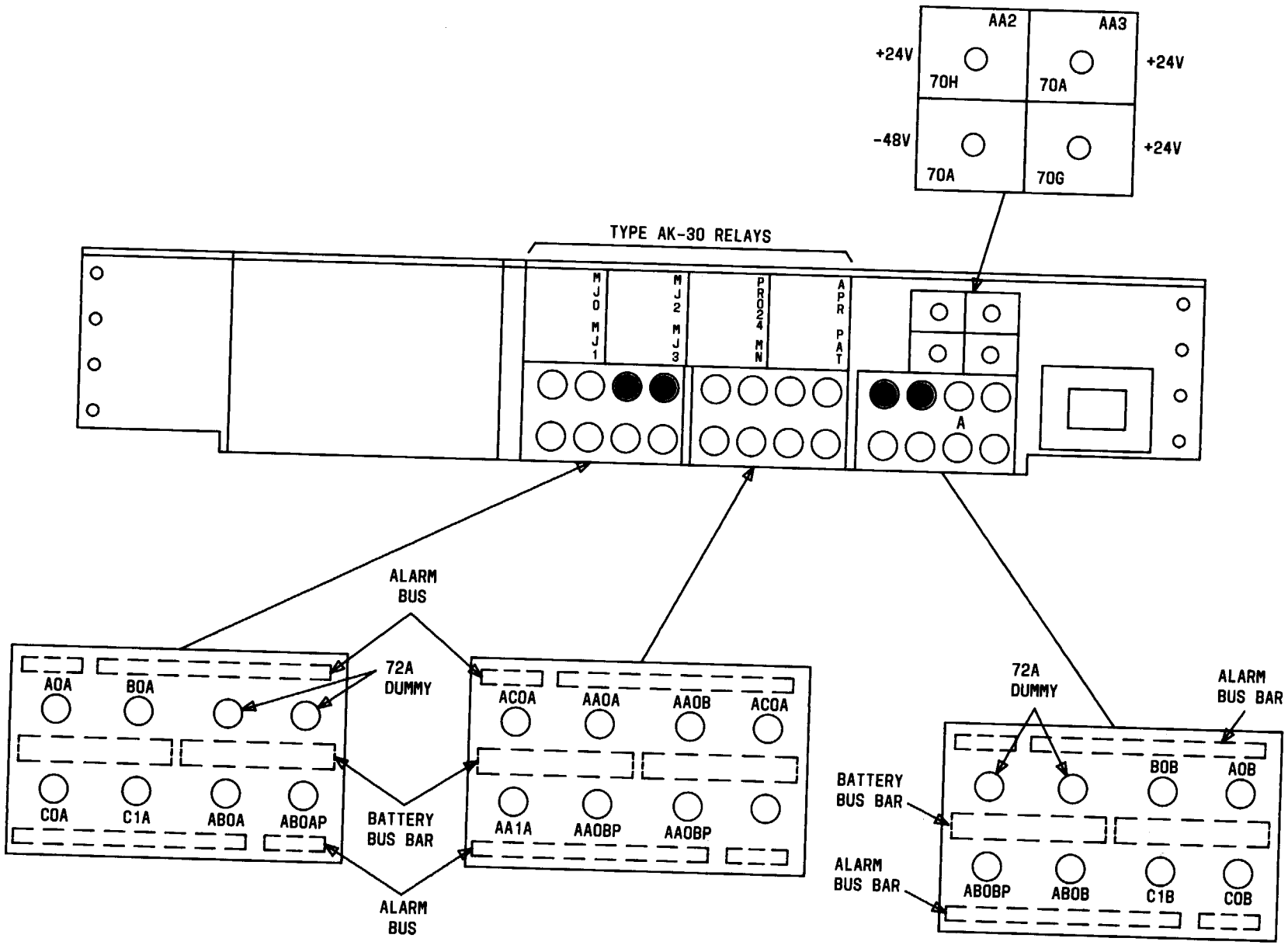


Fig. 36—Maintenance Frame Power Unit Component Locations

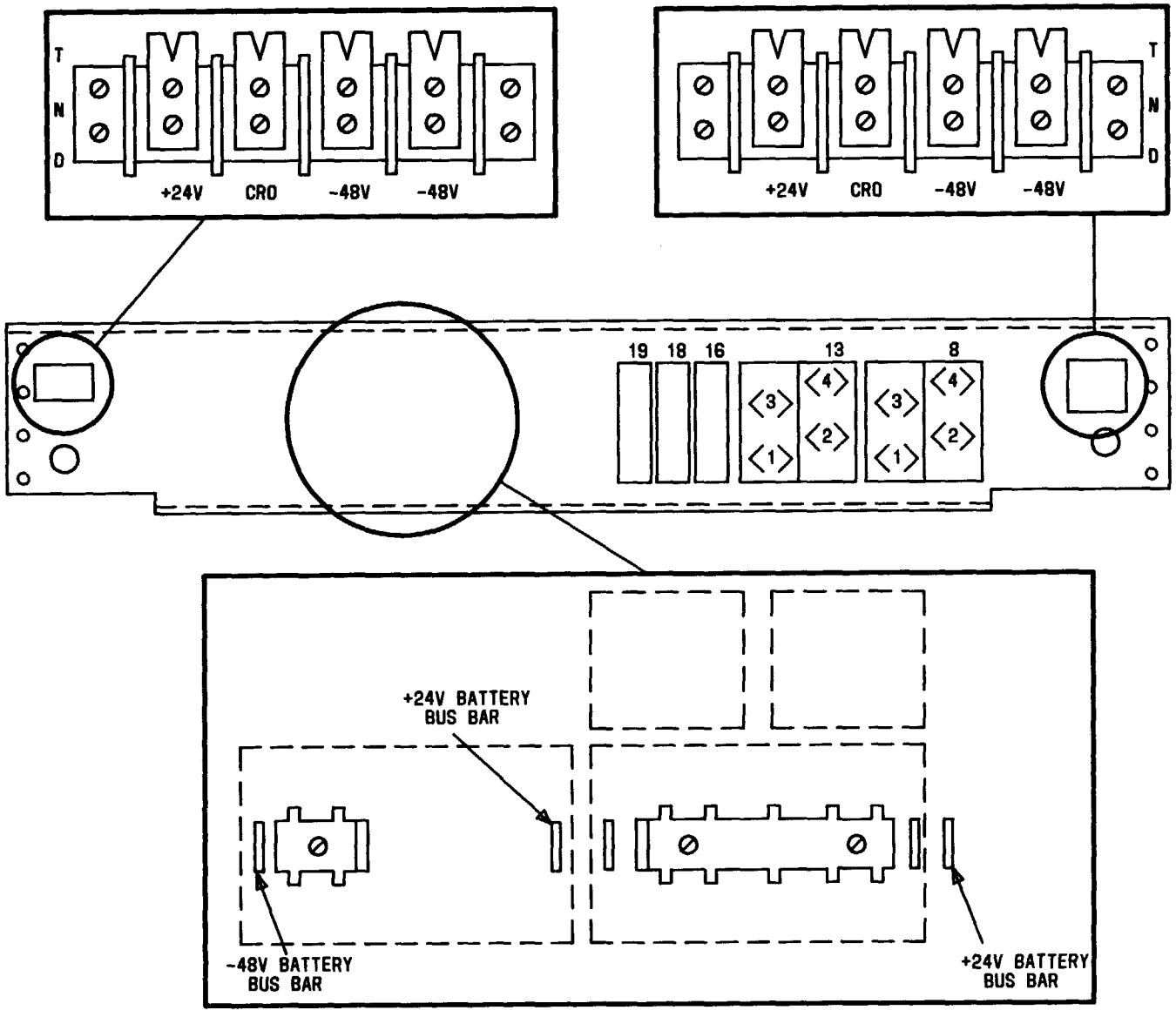


Fig. 37—Maintenance Frame Power Unit Component Locations, Rear

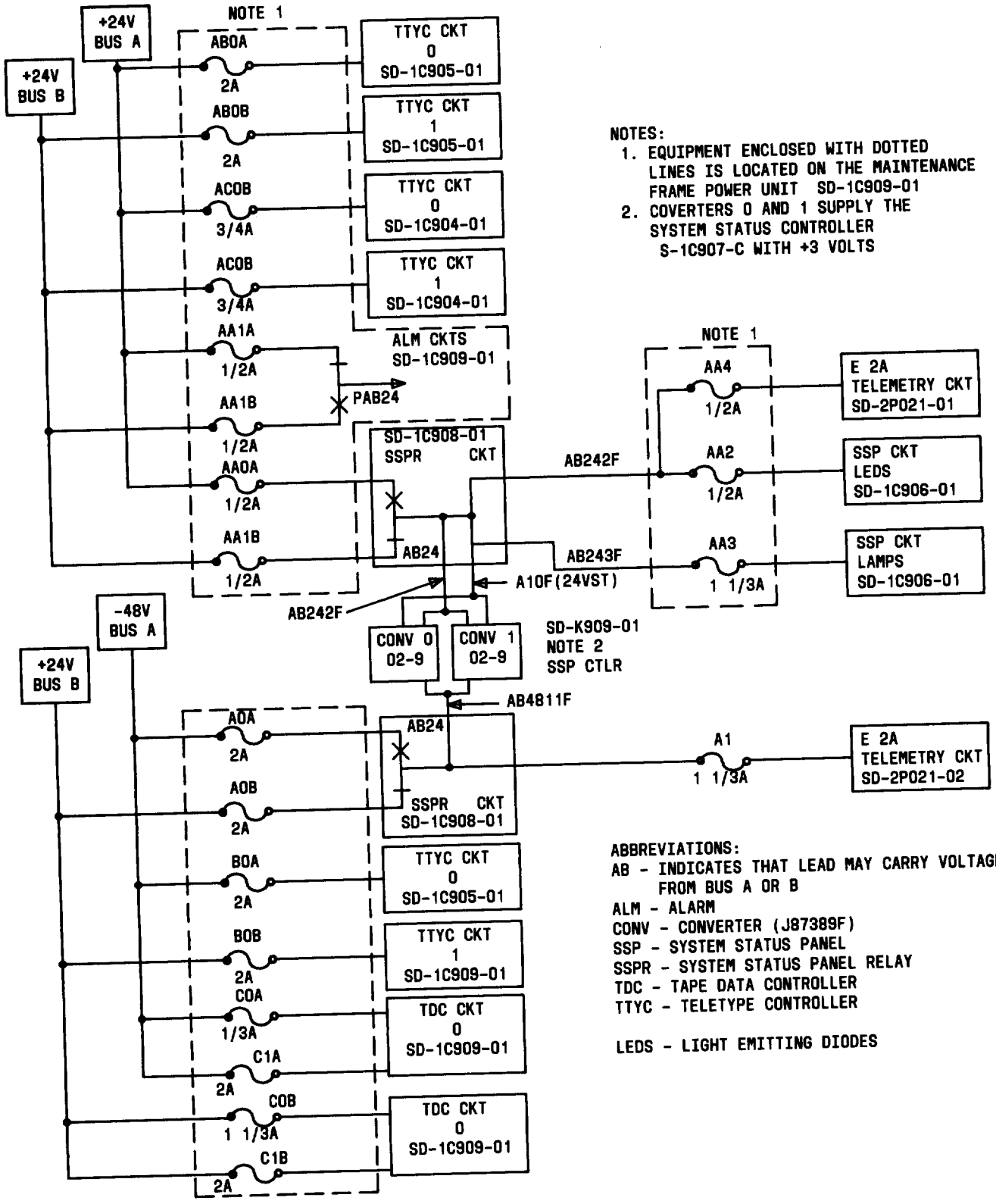
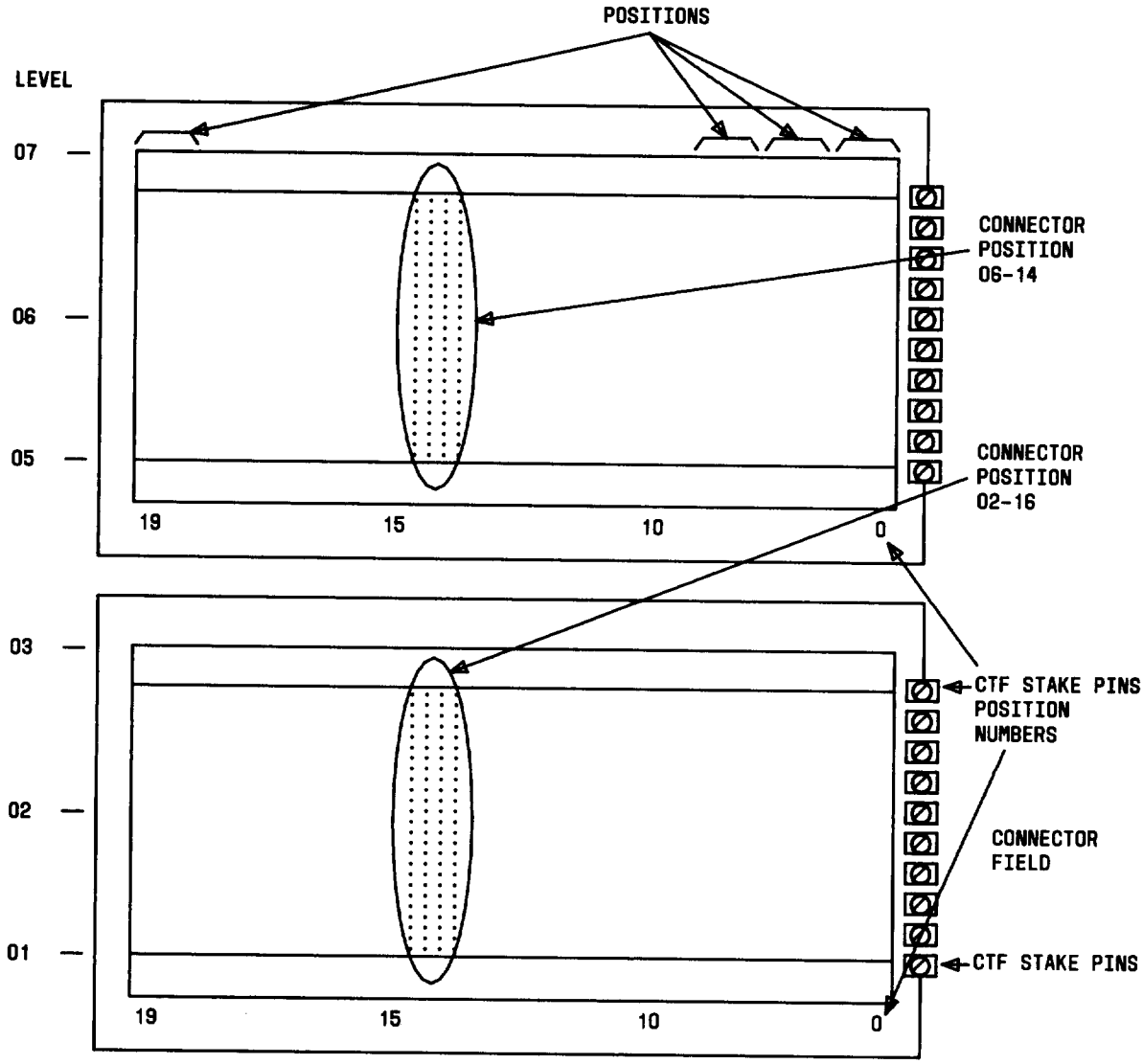


Fig. 38—Maintenance Frame Power Distribution



CONNECTOR AND COAXIAL TERMINAL FIELD (CTF) REFERENCES CONSIST OF A LEVEL NUMBER FOLLOWED BY A POSITION NUMBER. NOTE THAT CONNECTOR PINS ARE LOCATED AT LEVELS 02 AND 06.CTF PINS (STAKE PINS) ARE LOCATED AT LEVELS 01, 03, 05, AND 07.

Fig. 39—Connector & CTF Locations