AT&T 3B20D Model 1 Computer General Description

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1. Overview

1.01 This practice describes, in general terms, the physical and functional characteristics of the AT&T 3B20D Model 1 computer.

1.02 This practice is being reissued to include information about the Small Computer System Interface (SCSI). Since this is a general revision, revision arrows used to denote significant changes have been omitted. The Equipment Test lists are not affected.

1.03 This practice contains no admonishments.

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Purpose

1.07 The 3B20D Model 1 computer provides a high speed, general purpose, cost-effective computer which can be used in many applications. The 3B20D Model 1 computer is designed to be totally compatible with existing systems in terms of reliability and flexibility.

Configuration

1.08 Configuration of a 3B20D Model 1 computer varies depending on the application. The computer will generally consist of the following frames and associated functional units:

(a) Control unit (CU) frame

(b) Peripheral control (PC) frame

(c) Moving head disk (MHD) frame

(d) Magnetic tape (MT) frame

(e) Power distribution frame (PDF).

A. Control Unit Frame

1.09 The CU frame (Figure 1) contains the CU that provides the control function in the 3B20D Model 1 computer. Each CU consists of the following units:

- Direct memory access input/output (DMA I/O) unit.
- Central control (CC) unit.
- Main Store Module (MASM)—May consist of one MASM (0) or two MASMs (0 and 1). The MASMs are referred to as the main store (MAS).
- Power Units

— 244B DC-to-DC converters (maximum of 4)

— J1C129AE (one 203A DC-to-DC converter and one 132 AG DC-to-DC converter).

- Cooling unit ED-4C191.
- Fuse panels.

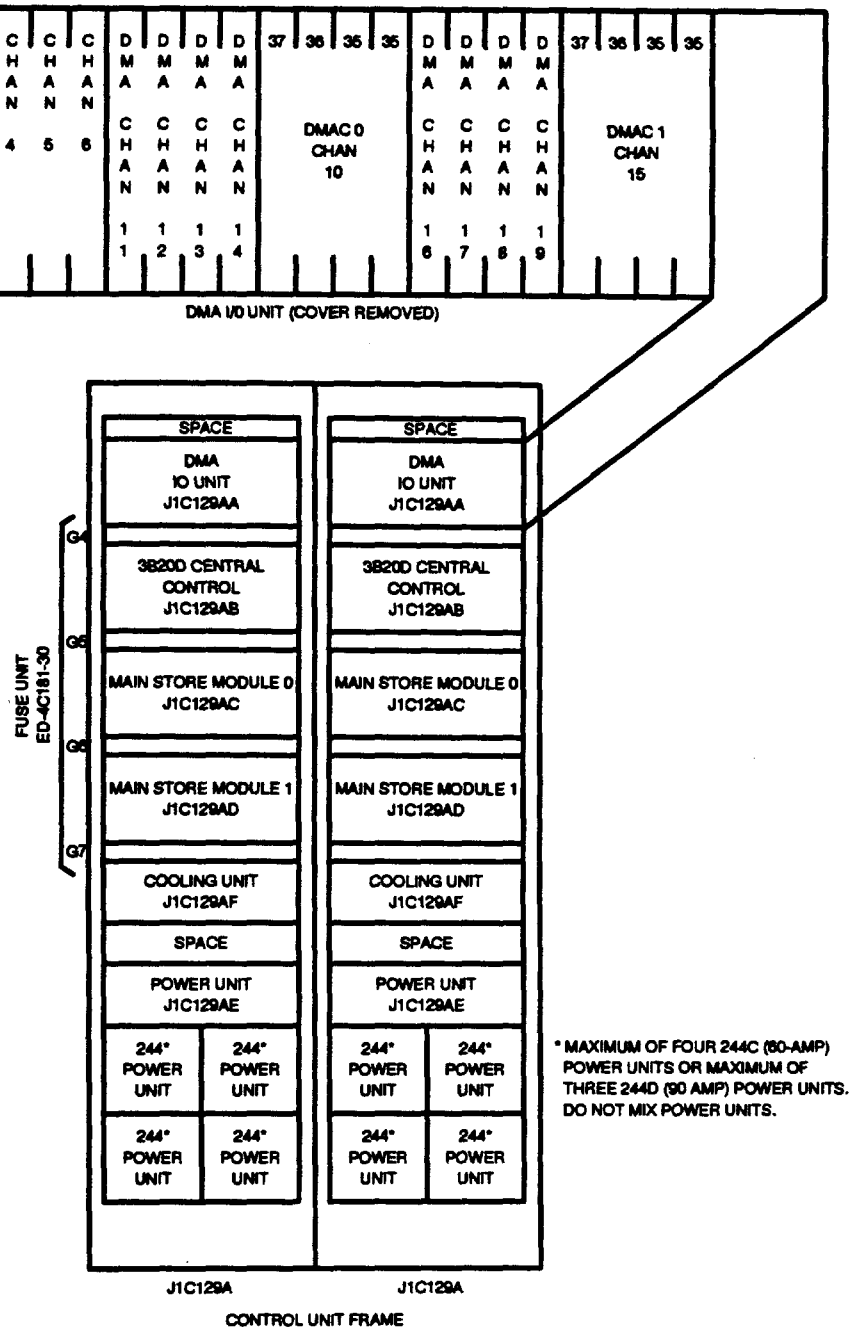

Figure 1. Control Unit Frame

B. Peripheral Control Frame

1.10 The PC frame (Figures 2 and 3) contains one each of the following units:

- Input/output processor (IOP)—The IOP may consist of an IOP basic unit or an IOP basic unit and IOP growth unit.
- Cooling unit ED-4C191—The cooling unit is always located beneath the IOP.
- Storage module drive - disk file controller (SMD-DFC).

1.11 When additional IOP units are required by the application, an IOP growth frame is required. A cooling unit ED-4C191 is required for each additional IOP. When additional SMD-DFCs are required, a DFC growth frame is required.

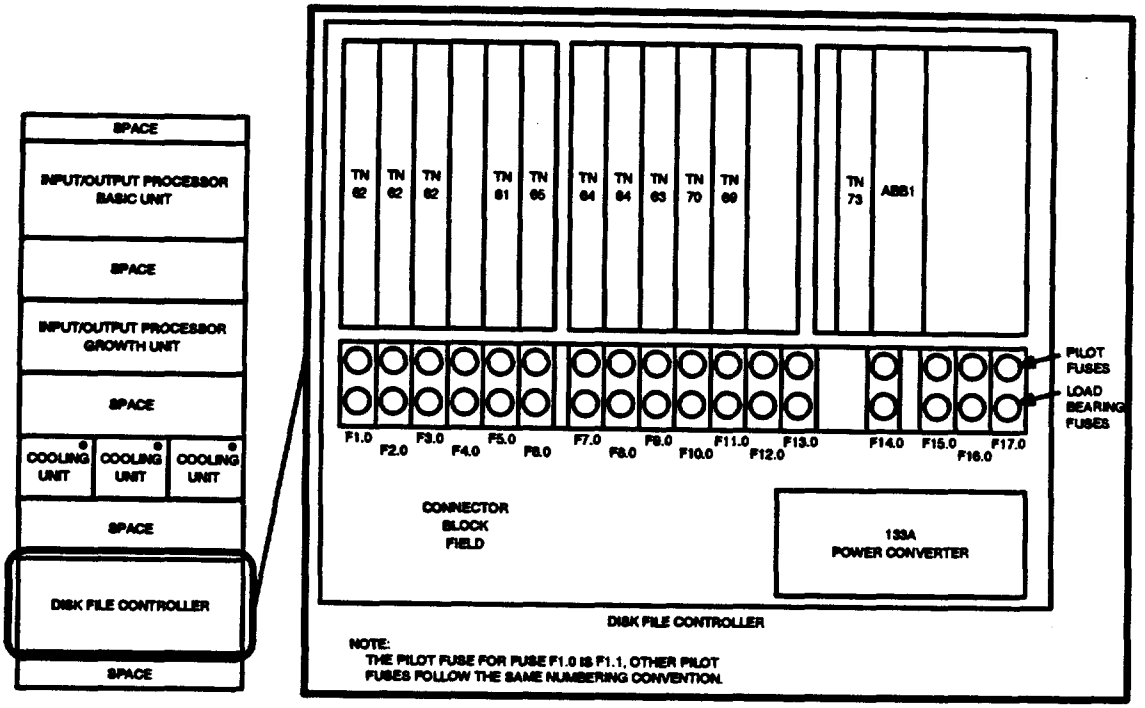

Figure 2. Peripheral Control Frame—SMD—Disk File Controller

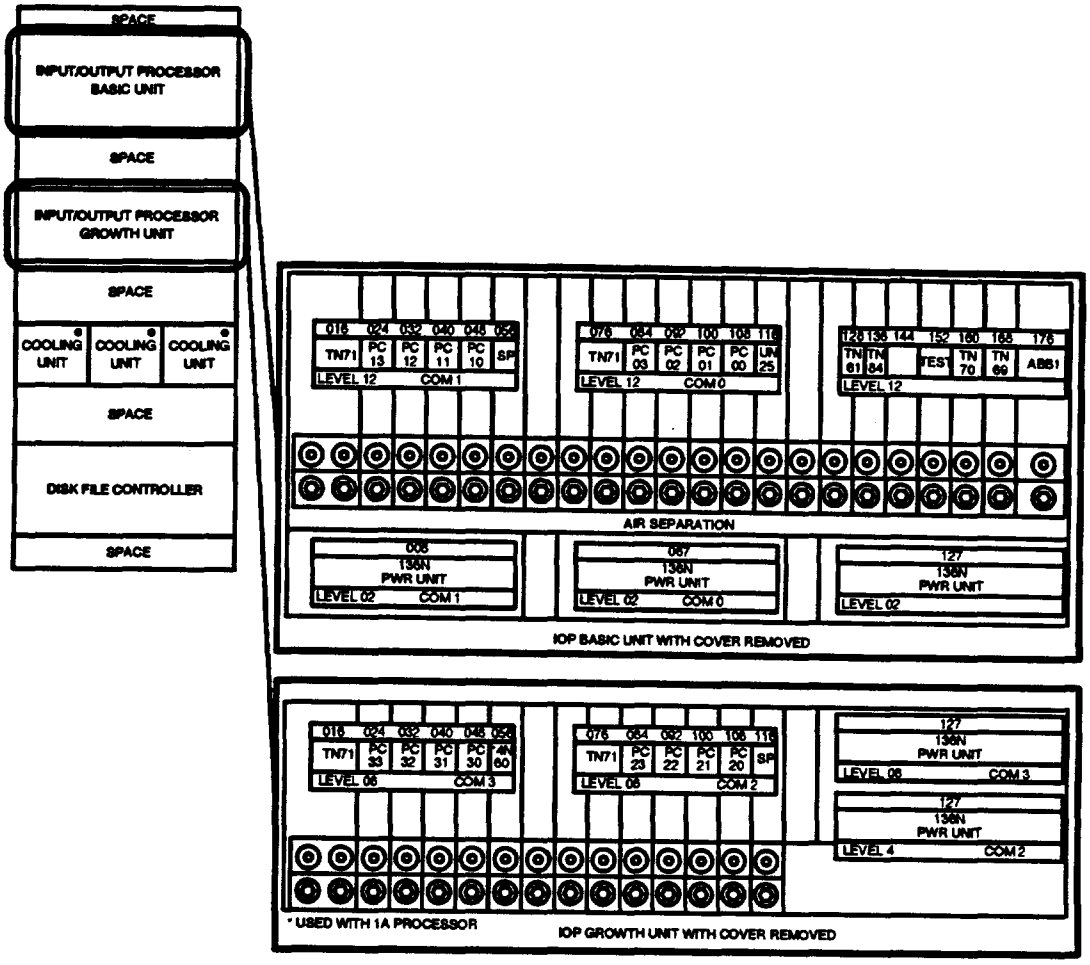

Figure 3. Peripheral Control Frame—Input/Output Basic Unit and Growth Unit

C. Moving Head Disk Frame

1.12 The MHD frame (Figure 4) contains one each of the following units:

- Disk file inverter
- Power control unit (PCU)
- Moving head disk drive (SMD interface), as follows:

— KS-21996, L2 or L3 (80 Megabyte)

— KS-22072, L1 or L2 (300 Megabyte)

— KS-22707, L1 or L2 (300 Megabyte)

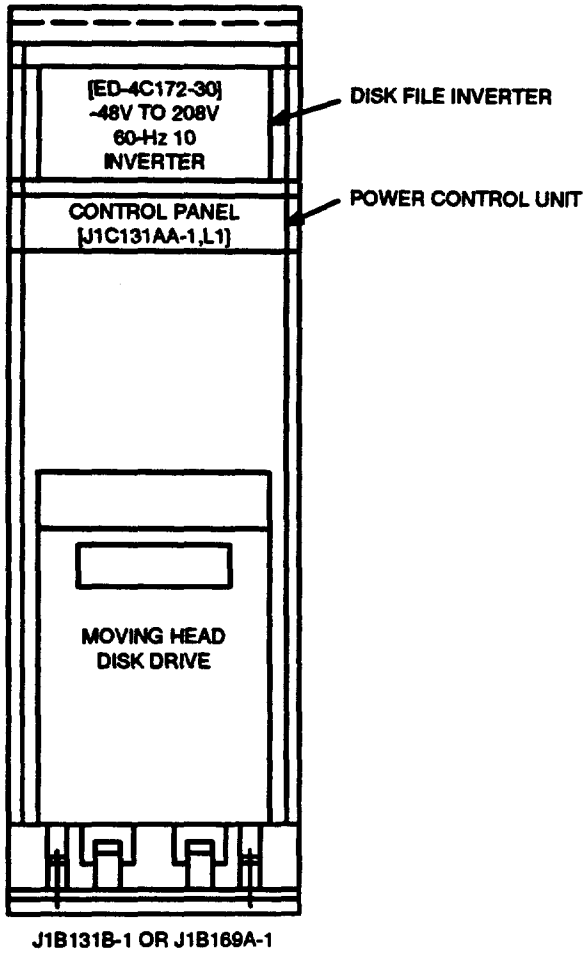

Figure 4. Moving Head Disk Frame (80/300 Mbyte)

D. Magnetic Tape Frame

1.13 The magnetic tape (MT) frame (Figure 5) contains one or two tape transports. Two models of tape transports are available:

- KS-22091, L2 (equipped with formatter)
- KS-22091, L1 (without formatter).

1.14 Each KS-22091, L2 tape transport (with formatter) can support a maximum of three KS-22091, L1 tape transports, which must be connected to a formatter. If more than two tape transports are required by the application, additional MT frames must be used. For fast backup, the streaming tape drive (KS-23113) may be used.

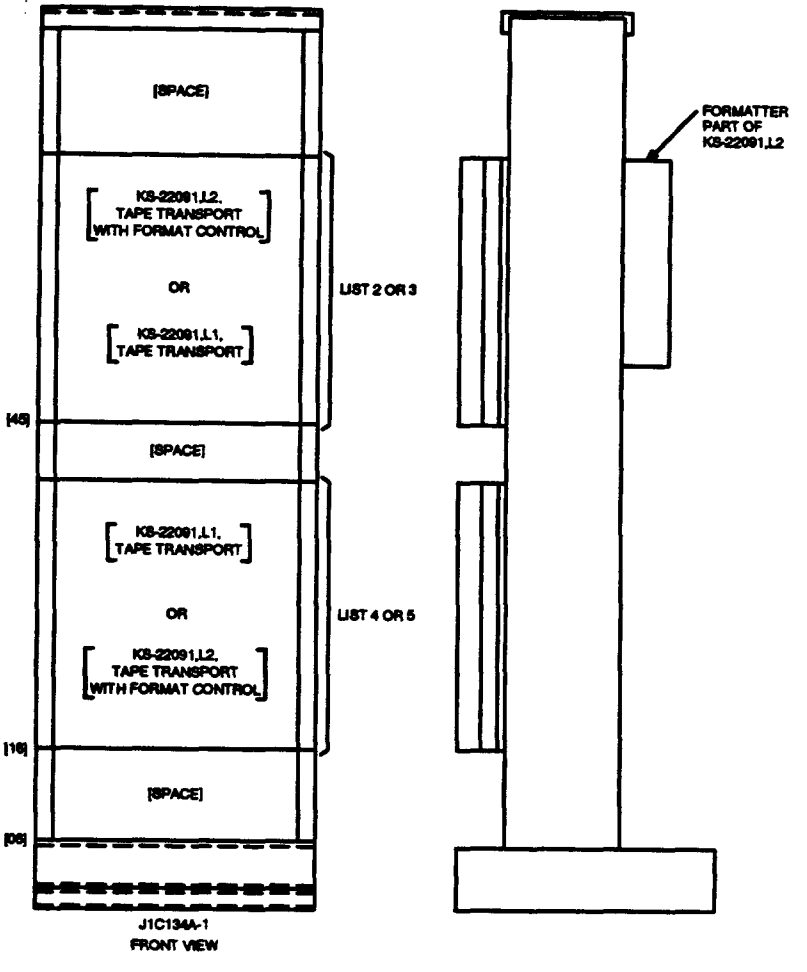

Figure 5. Magnetic Tape Frame

E. Power Distribution Frame

1.15 The power distribution frame (PDF) (Figure 6) provides the –48 V DC power distribution for the 3B20D Model 1 computer frames. Only one PDF is required per 3B20D Model 1 computer. The PDF contains the following units:

- Alarm Panel (one required)
- Filter-Fuse Panel (the number is dependent on application)
- Control Panel (one required)
- Circuit Breaker Panel (the number is dependent on application).

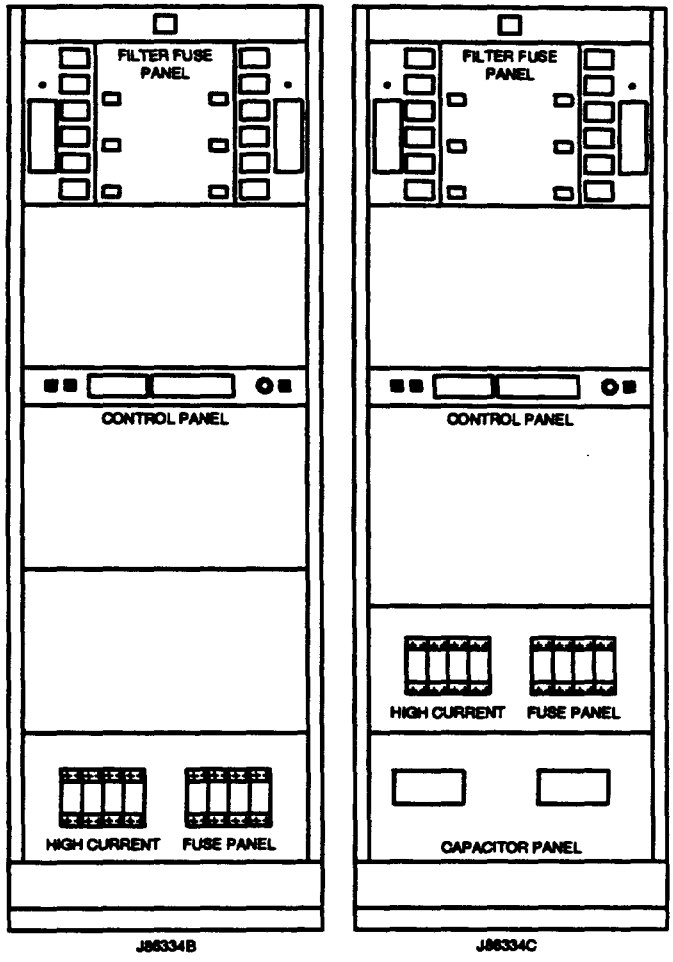

Figure 6. Power Distribution Frame

F. Circuit Packs

1.16 The basic circuit pack used in the 3B20D Model 1 computer measures 8 inches by 13 inches and is equipped with either a 200-pin connector (TN code series) or a 300-pin connector (UN code series).

1.17 The circuit packages are standard transistor-transistor logic (TTL) circuits and TTL-compatible large-scale integration (LSI) circuits. Low-power integrated circuit packs (ICPs) are used whenever possible to minimize power consumption and heat dissipation. High speed ICPs are used when higher speed is required.

1.18 Figure 7 illustrates a typical duplex 3B20D Model 1 computer floor plan.

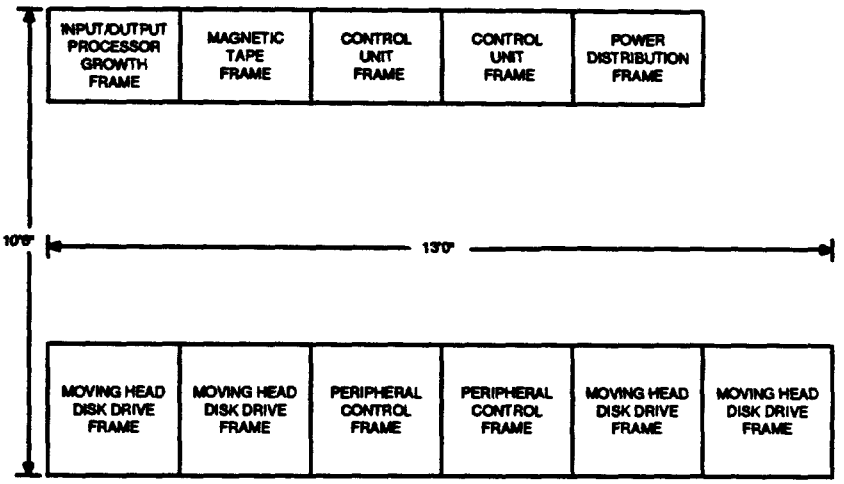

Figure 7. Typical 3B20D Model 1 Computer Floor Plan

G. Types of Configurations

1.19 The 3B20D Model 1 computer may have two types of configuration:

- Simplex (one CU frame)
- Duplex (two CU frames).

1.20 ***Simplex:*** A simplex configuration consists of only one CU and is used in applications where the computer is not performing service-affecting functions. Only one unit is required to perform all operating functions.

1.21 ***Duplex:*** The duplex (duplicated) configuration uses two CUs (one active and one standby). If a failure occurs in the on-line (active) CU, the on-line CU is switched off-line, and the standby CU is switched on-line, preventing service interruption. The duplex configuration is used for high reliability and continuity of service.

2. Physical Description

2.01 Table A is a summary of the physical dimensions of the units comprising the 3B20D Model 1 computer.

Table A. Physical Dimension

Frame	Unit	Width	Height	Figure
CU	DMA I/O	22 inches	8 inches	1
	3B Computer	22 inches	8 inches	
	MASM	22 inches	8inches	
	Cooling Unit	22 inches	6 inches	
PC	IOP Basic	22 inches	16 inches	2
	IOP Growth	22 inches	16 inches	
	Cooling Unit	22 inches	6 inches	
	DFC	22 inches	16 inches	
MHD	Disk File Inverter	22 inches	12 inches	3
	PCU	22 inches	5 inches	
	MHDD	22 inches	40 inches	
MT	Tape Transport	22 inches	24 inches	4
PDF	Alarm Panel	25 inches	3 inches	5
	Control Panel	25 inches	3 inches	
	Filter Fuse Panel	25 inches	13 inches	
	Circuit Breaker Panel	25 inches	10 inches	

A. Control Unit Frame

2.02 The CU frame (Figure 1) is comprised of a CU which consists of:

- Direct Memory Access I/O unit
- Central Control
- Main Store Module(s)
- Cooling Unit ED-4C191
- Power Unit
- Power Converter.

Direct Memory Access I/O Unit

2.03 The Direct Memory Access (DMA) I/O unit consists of the following subunits:

- ***DMA controller (DMAC)***—A maximum of two DMACs may be installed. Each DMAC requires four circuit packs.

- ***DMAC channels***—Each DMAC may be equipped with a maximum of four dual serial channels (DSCHs). One circuit pack is required for each DSCH.
- ***Input/Output (I/O) channels***—Five I/O channels (2 through 6) may be provided in the DMA I/O unit with each I/O channel consisting of one circuit pack. These may be any combination of the following I/O channels:
- ***Serial Channel (SCH)*** for low- and medium-speed peripheral devices (PDs). The SCH can support a maximum of 20 PDs.
- ***Application Channel (ACHI)*** used for application-designed circuits
- ***Dual Serial Channel (DSCH)*** for medium- and high-speed PDs. The DSCH can support a maximum of 16 PDs.

2.04 Figure 8 illustrates the I/O structure and interfaces.

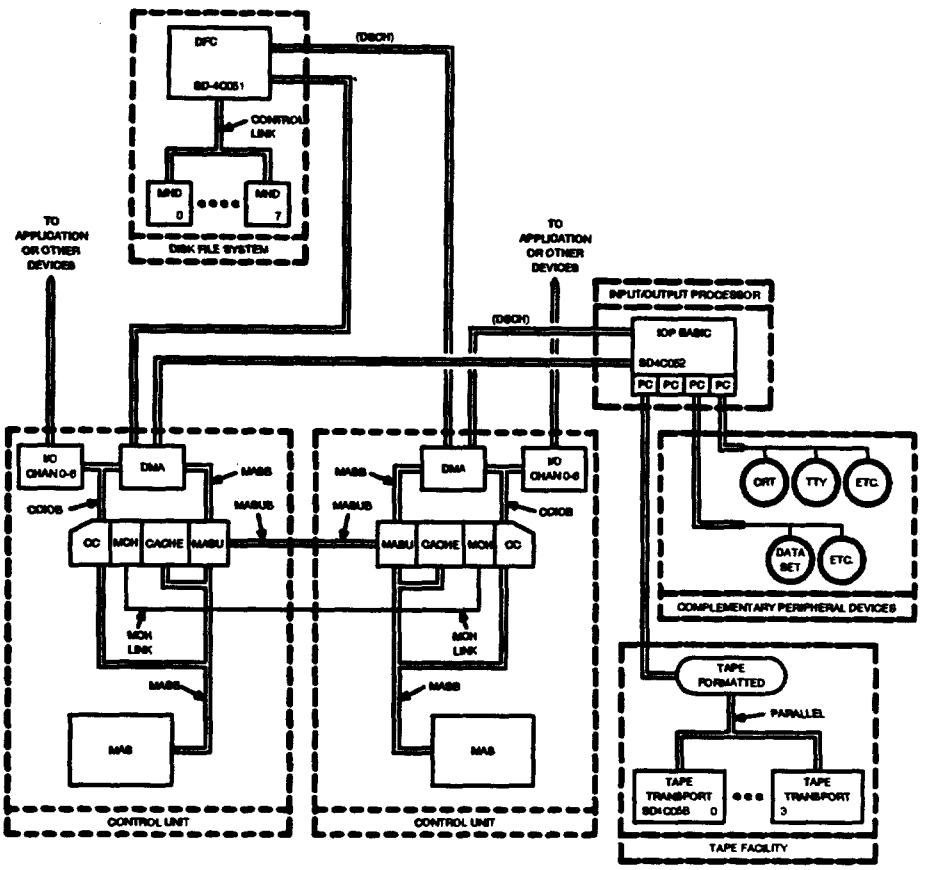

Figure 8. 3B20D Model 1 Computer Functional Overview

Central Control

2.05 The central control (CC) contains the following units:

- ***Microstore***—Two to four circuit packs; one contains 4K (K=1024) words (32 bits) of writable microstore. The remaining circuit packs contain 4K (4096) words of read-only memory. The number of circuit packs used is dependent on the application.
- ***Central Processing Unit***—Eight circuit packs which contain the microcontrol, store address translator, data manipulation unit, store data control, special registers, and store address controller.
- ***Main Store Update Unit***—One circuit pack is required, which is used with the DMA and/or duplex configuration.
- ***Maintenance Channel***—One circuit pack is required for the duplex configuration or simplex (application-dependent).
- ***Cache Store Unit***—When this option is used, three circuit packs are required.
- ***Microaccess***—If the 3B20D Model 1 computer is equipped with a microlevel test set, one circuit pack for microaccess is required.
- ***Softwareaccess***—This circuit pack position is available for use by either the utility circuit or software test set option.
- ***I/O Channels***—Two circuit pack positions are available for I/O channels (0, 1). Each I/O channel requires one circuit pack and may be any combination of SCH, DSCH, and ACHI.

Main Store Module

2.06 The CU may be equipped with one or two main store modules (MASMs) (0, or 0 and 1). The MASM 0 contains two additional circuits more than the MASM 1. These are the ABB1 power switch and the emergency action interface (EAI) circuit pack. Basically, a MASM consists of a MAS controller (MASC) and up to 16 MAS arrays (MASAs). The MASC requires one or two circuit packs (application-dependent) and the MASA requires one. The minimum-equipped MASM contains a MASC and one MASA.

2.07 The capacity of the MASA circuit pack is 0.5 megabyte when equipped with the TN14. Effective with duplex multienvironment real time (DMERT) generic 2, a TN28 MASA circuit pack with a 1-megabyte capacity may be retrofitted. The TN56 MASA circuit pack with a capacity of 2 megabytes may replace the TN28 effective with *UNIX** RTR Operating System Release 1. With either the TN28 or TN56, the MASC must be changed to a UN59 or UN59B circuit pack, respectively. The main store can

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have a maximum capacity of 16 megabytes; thus, main store module 1 cannot be used with TN56 main store array circuit packs.

2.08 Application of the extended main memory feature increases the amount of memory for a 3B20D Model 1 computer, in increments of two megabytes, from 16 to a maximum of 32 megabytes.

Cooling Unit ED-4C191

2.09 The cooling unit is located directly below the MASMs. It is divided into three cooling sections, each containing a fan, control circuitry, filter, and an alarm condition light emitting diode (LED).

Power

2.10 Two to four (maximum) 244B, DC-to-DC converters (–48 V to +5 V) may be used, depending on the application. The +5 V outputs are paralleled to increase current capability.

2.11 The J1C129AE power unit is comprised of the following:

- 203A DC-to-DC converter (–48 V to +5 V and ±12 V)
- 132AG DC-to-DC converter (–48 V to –5 V and +12 V).

2.12 The power units are located at the bottom of the CU frame.

B. Peripheral Control Frame

2.13 The PC frame (Figures 2 and 3) is comprised of:

- IOP made up of an IOP basic unit or an IOP basic unit and an IOP growth unit
- Cooling Unit ED-4C191 located beneath the IOP
- SMD-DFC located at the bottom of the PC frame.

2.14 The IOP basic unit contains the peripheral interface controller, peripheral communities 0 and 1, power units, an ABB1 power switch, and fuses. Each peripheral community consists of a maximum of four peripheral controllers and power circuitry.

2.15 The IOP growth unit consists of two peripheral communities (2 and 3). Each community can contain a maximum of four peripheral controllers and associated power circuitry.

2.16 The cooling unit ED-4C191 is divided into three cooling sections. Each section contains a fan, control circuitry, filter, and alarm condition LED.

2.17 The SMD-DFC contains disk file controller circuitry, ABB1 power switch, and associated power circuitry. The DFC can support up to a maximum of eight MHDs.

C. Moving Head Disk Frame

2.18 The moving head disk (MHD) frame (Figure 4) contains the following units:

- ***Disk File Inverter*** located at the top of the frame, converts a high-current –48 V DC to 208 V for disk drive operation.
- ***PCU*** located directly below the disk file inverter which provides the power switch for the disk drive.
- The moving head disk drive located at the bottom of the frame and slightly raised from the floor by a metal plate. This is a self-contained commercially manufactured disk drive.

D. Magnetic Tape Frame

2.19 The magnetic tape (MT) frame (Figure 5) may contain one or two tape transports. The tape transport is a 9-track, dual density recorder which can record and reproduce data in an 800 bit-per-inch nonreturn-to-zero format, or a 1600 bit-per-inch phase-encoded format.

E. Power Distribution Frame

2.20 The power distribution frame (PDF) (Figure 6) contains the following:

- Alarm Panel, one per PDF, which consists of four lamps
- Filter Fuse Panel (ED-82884-30) (a maximum of five) which consists of capacitors, fuse blocks, fuse holders, and LEDs
- Control Panel (ED-82884-30) (one per PDF) which consists of fuse blocks, switches, two circuit packs, a charge circuit, and a charge probe.
- Circuit Breaker Panel (ED-82884-30) (a maximum of two) which consists of a maximum of 12 circuit breakers. The circuit breaker panel is used for power distribution to the MHD frames.

3. Interfaces

3.01 The 3B20D Model 1 computer can essentially be divided into three sections:

(a) CU

(b) Periphery (which is controlled by the CU)

(c) Power.

A. Control Unit

3.02 Figures 8 and 9 illustrate the 3B20D Model 1 computer interfaces. The CC is connected to the MASM(s) via the MAS bus (MASB), which is a 74-lead bus used to transmit address, data, and control information. The CUs communicate with each other via the maintenance channel (MCH) using the MCH link bus.

3.03 In the duplex configuration, interconnection between the duplicated CUs (CU 0 and CU 1) is via the MAS update bus (MASUB). Also, the DMAC(s) access the duplicated MASMs via the MASB and MASUB. The MAS update circuit pack (MASU) selects which of the three users of the MASM (CC, DMAC, and MASU from the duplicated CU) will have use of the MASB at any particular time. The on-line CU will normally keep the off-line MASM (in off-line CU) updated in case of a necessary switching of CUs.

3.04 The I/O channels (DMAC, SCH, ACHI, and DSCH) are accessed by the CC via the CCIO bus (CCIOB). The CCIOB is used to transmit address, data, and control information between the I/O channels and the CC. Peripheral devices (PDs) connected to the SCH, ACHI, or DSCH require CC control for each word received or transmitted. The PDs connected to the DMAC operate independently from the CC once the data transfer parameters are established and the transfer is initiated.

3.05 The MASM is connected to the CC via the MASB and the MASUB in the duplicated configuration. The MASM is connected to the DMAC via the MASB, and the duplicated MASM via the MASU by the MASUB.

3.06 The SCH can interface with a maximum of 20 PDs, each of which can be up to a 100 feet distant from the CU. Serial data is transmitted between the SCH and PDs via a single cable.

3.07 The DSCH (part of DMAC or as a program-controlled I/O channel) can interface a maximum of 16 PDs. Two serial messages are transmitted to the selected PD via two separate cables while two simultaneous messages are received over another pair of cables. The PDs connected to a DSCH may be located up to 250 feet from the CU when the 5-MHz clock is used, and 100 feet when the 10-MHz clock is used.

3.08 The ACHI is a general purpose parallel interface for the 3B20D Model 1 computer. It may be located in the CC unit or the DMA I/O unit. The ACHI is interfaced to the CC via the CCIO bus and to the peripheral device via DC differential lines. The maximum distance between the ACHI and peripheral device is 50 feet. One ACHI can interface only one peripheral device.

B. Periphery

3.09 The major peripheral units in the 3B20D Model 1 computer are the IOP and DFC units. Application peripheral units are interfaced to the CU via the I/O channels or the IOP. The DFC provides interface for the file system (MHDD) to the CU.

3.10 The IOP and DFC are interfaced to the DMAC via the DIO which is similar to the CCIO. Interface units are used to connect the units to the DIO bus. These are:

- Duplex dual serial bus selector (DDSBS) in the IOP and DFC and
- DSCH in the DMAC (DMAC channel).

3.11 In the duplex configuration, the DDSBS provides access to the IOP and DFC by either CU. The PDs connected to the I/O channels (SCH, ACHI, DSCH, but not the DMAC channels) can only be accessed by the CU containing those I/O channels unless a DDSBS or similar interface unit is used. (Either CU can then access the PD.)

3.12 The PDs connected to the SCHs, ACHIs, and DSCHs are connected by cables. The DMAC channels (DSCHs) require connection to the DIO bus.

3.13 Peripheral devices connected to the IOP require an interfacing peripheral controller in a peripheral line community. The IOP can support the following types of peripheral controllers:

- Tape controller (tape transport)
- Scanner/signal distributor
- Data link controller
- TTY controller (printer, TTY, video terminal)
- Application-designed controllers.

3.14 These peripheral controllers are circuit packs that are installed in an IOP peripheral line community. Connection between the peripheral controllers and PDs are provided by cable.

3.15 Connections between the SMD-DFC and MHD frames is provided by the control link bus. Each DFC can support a maximum of 8 MHD frames.

3.16 The MT frame is connected to the IOP via a cable to the peripheral controller. One tape transport with formatter can support a maximum of four tape transports without a formatter.

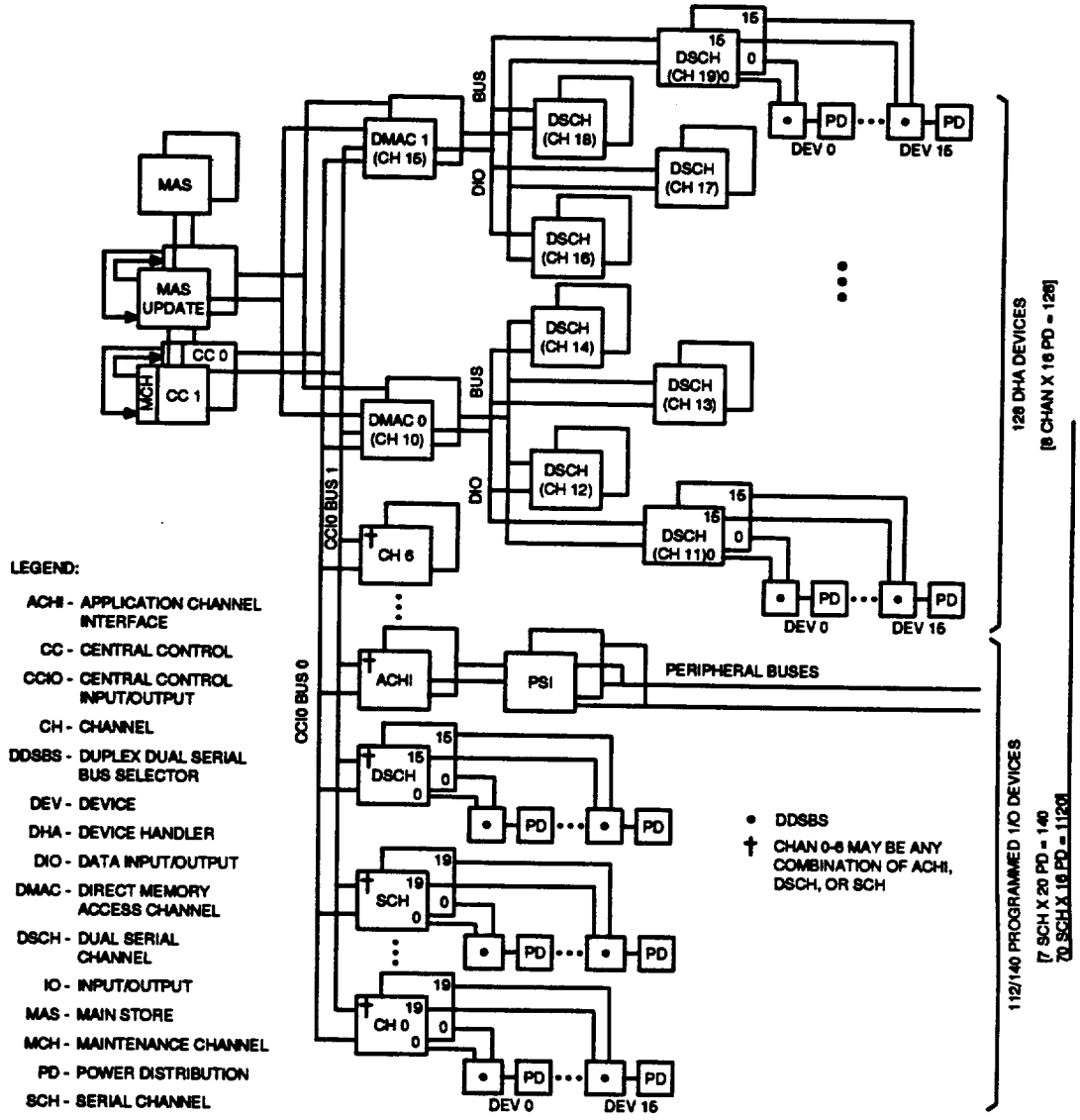

Figure 9. I/O Interfaces

C. Power

3.17 A summary of the power requirements is provided in Table B.

Table B. Power Requirements

Source	Destination	Voltage
Filter-Fuse Panel (PDF)	CU Frame	-48 V DC
	PC Frame	-48 V DC
	IOP Growth Frame	-48 V DC
	DFC Growth Frame	-48 V DC
	MT Frame(s)	-48 V DC
Circuit Breaker Panel (PDF)	MHD Frame(s)	-48 V DC
AC Distribution Panels	MHD Frame(s)	208 V 60 Hz
	Peripheral Units (ie, Terminals, etc.)	115 V 60 Hz

3.18 The –48 V DC source voltage is connected to the PDF frame and distributed to the 3B20D Model 1 computer frames via buses (See Figure 10). Filter-fuse panels provide fusing for the –48 V DC to the frames. Circuit breakers are required for the MHD frames because of the current requirements. The MHD frames require 208 V for MHDD operation. Additional power (115 V AC 60 Hz) is required for peripheral equipment (e.g., terminal, etc.). This is provided by the application.

3.19 The CU contains a power unit to convert the –48 V DC from the PDF to the required voltages for the CU units. The outputs of the power unit are connected to the units via backplane wiring. The IOP and DFC contain DC-to-DC converters that convert the –48 V from the PDF to the required voltages for operation. These outputs are connected to the circuits via backplane wiring.

3.20 The –48 V from the PDF is connected to the tape transports in the MT frame. The tape transports are provided with internal converters.

3.21 The MHD frame requires –48 V from the PDF for the disk file inverter as a back-up source in case commercial 208 V is interrupted.

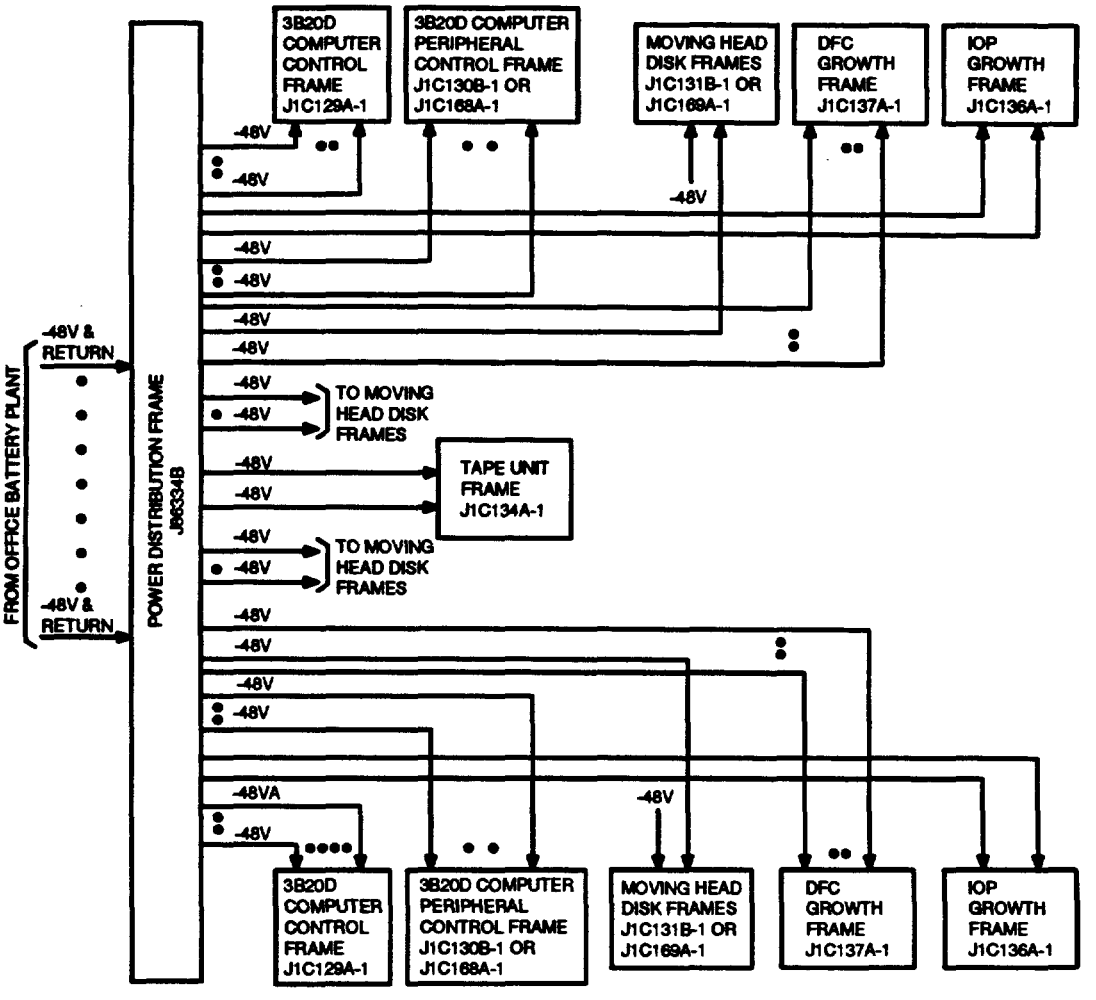

Figure 10. Typical Power Distribution

4. Functional Description

A. Control Unit

4.01 The CU is comprised of the following:

- A CC
- MASM(s)
- A DMA I/O unit
- Power.

Central Control

4.02 The CC is a microprogrammed processor using a read-only memory to contain a series of microinstructions which direct activity of the processor. Each MAS instruction is put into effect by executing a series of microinstructions that are read out of microstore, one microinstruction at a time. Figure 11 depicts the CC internal architecture.

4.03 The microstore is addressed using the 16-bit microaddress bus and is normally controlled by the microcontrol section of the CC. Output of the microstore is a microinstruction (56-bit plus 8-bit parity) word which is decoded by microcontrol to provide control signals for the CC.

4.04 Fields within the microinstruction are used to define the type of microinstruction, define minimum microinstruction execution time (150, 200, 250, or 300 nanoseconds), define source and destination registers, define operations to be performed, provide part of the address of the next microinstruction, and provide check bits to verify proper operation of the microstore.

4.05 Sixteen 32-bit general registers are available and are usable by the software as a scratch pad as well as by the CC as sources and destinations for data. Several special registers are available that perform unique functions. These registers are generally not accessible by the programmer, but are used by the CC to store results of internal operations. These registers include the program address, program data, instruction buffer, and interrupt set registers, for example. Table C contains a list of all special registers and their functions. All special registers are 32 bits long except PA and SAR, which are 24 bits long.

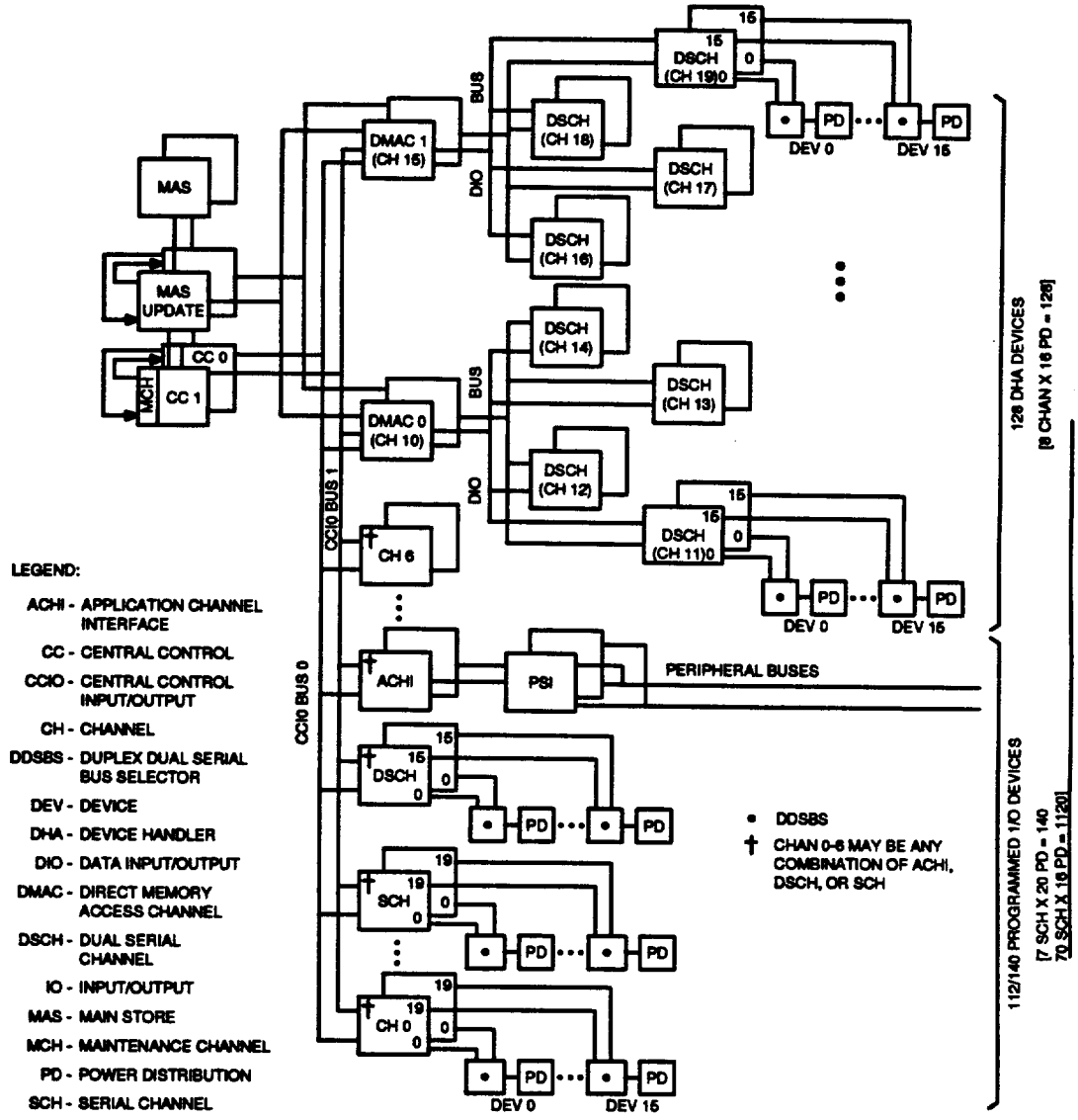

Figure 11. Control Unit Internal Architecture

Table C. Special Registers

Register	Function
Program Address	A 24-bit register which contains the address of the current instruction being executed.
Store Address (SAR)	A 24-bit register which contains address of operand being referenced in MAS.
Store Data (SDR)	Contains copy of operand being referenced in MAS.
Instruction Buffer (IB)	Contains copy of instruction being referenced in MAS.
Store Control (SCR)	Holds data word used to control MAS operation.
Interrupt Source (IS)	Records interrupts as they occur.
Interrupt Mask (IM)	Used to control recognition of interrupt. Contents of IM are logically ANDed with IS to signal presence of allowed interrupts
Program Status Word (PSW)	Contains status information pertinent to currently executing programs.

4.06 Other registers include: the system status register, which stores information concerning system status; an error register, which stores signals which indicate that certain errors have occurred; a sanity timer and elapsed time counter to provide time-out capability and a real-time clock.

4.07 The arithmetic logic unit (ALU) performs arithmetic and logical operations on data supplied to it. These operations are binary 2s complement addition and subtraction, OR, AND, EXCLUSIVE OR (XOR), EXCLUSIVE NOR (XNOR), and complement. The rotate mask unit (RMU) provides right rotates and shifts of zero to 31 bits in one operation. The AND/OR operations can also be performed on bits, nibbles (4-bit groups), bytes (8 bits), and half words (16 bits).

4.08 An optional cache store unit (CSU) provides a means of decreasing access and cycle times of store operations. The CSU consists of three high speed memory arrays, each containing 512 words, and has an access time of 200 nanoseconds. The CSU may also provide a 2K word buffer for use as an interrupt stack. Each word read from MAS is also stored in the cache memory. In addition, each time a main store read is requested, part of the address is decoded to read the corresponding address in the cache memory. If the requested data word is in cache, it is returned from there and the main store read is inhibited. Thus, frequently used data words will usually be found in cache memory. Since a fetch from cache is much faster than a fetch from MAS, this technique significantly improves CC throughput.

Direct Memory Access I/O Unit

4.09 The 3B20D Model 1 computer may be equipped with as many as seven programmable I/O channels (two of these are in the CC unit) and as many as eight DMA channels (Figure 9). Programmable channels are controlled directly by the 3B CC over the CCIO bus (Figure 12). The DMAC provides the capability for direct data transfers between main store and peripheral devices. Three types of channel interfaces are available, each of which is described in the following text.

Serial Channel

4.10 The serial channel (SCH) can communicate with as many as 20 devices via individual transformer-coupled cables, one cable for input and one cable for output for each device. A serial message is transmitted to the selected device, and a response is returned. Each message contains a 3-bit start code and a 36-bit data message. The SCHs may also connect to 16-bit devices, in which case software commands cause a 21-bit serial message to be transmitted (16 data bits, 2 parity bits, and the 3-bit start code.)

4.11 All signals on the SCH are transformer-coupled to provide DC fault isolation and are bipolar to prevent a DC voltage level from appearing on the cable.

Dual Serial Channel

4.12 A dual serial channel (DSCH) communicates with as many as 16 devices over separate pairs of input and output cables to each device. For write operations, two serial messages are simultaneously transmitted to the selected device and two responses are received. For read operations, two messages are sent to the device and two messages are received. The message format is identical to the SCH. The DSCH is used as an I/O channel or a DMAC channel.

4.13 The DSCH to device interface is made by a duplex dual serial bus selector (DDSBS), which allows the peripheral device to be connected to either of the duplicated CCs.

Direct Memory Access Controller

4.14 Each DMA unit operates under the control of the direct memory access controller (DMAC) located in the CU. The DMAC provides interfaces with main store, as many as four DSCHs over the DIO bus, the CC over the CCIO bus, and logic needed to control data transfers. Each DMA unit may contain up to two DMACs.

4.15 The main store interface, under control of the DMAC, carries address, data, and control information, receives read data from main store, and notifies the DMAC when the data transfer is complete.

4.16 The DMAC can transfer data at a rate sufficient to read or write two disk drives operating at full speed.

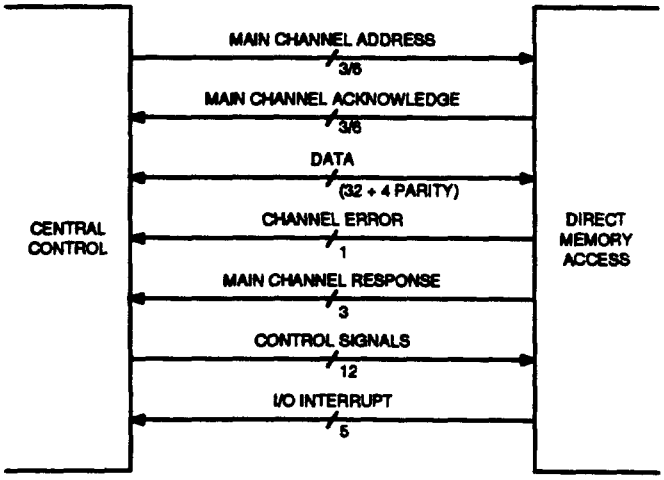

Figure 12. Processor CCIO Bus

Application Channel Interface

4.17 The application channel interface (ACHI) is provided so that the system designer may have a great deal of flexibility in the types of peripheral devices that may be controlled by a 3B20D Model 1 computer. The ACHI consists of a 36-bit input register, a similar output register, flag flip-flops, and interface logic to the CCIO bus. Signals between the ACHI and the peripheral device are carried on differential DC-coupled lines.

Main Store Module

4.18 The MASM is comprised of the MASC and MASAs. The MASC provides the interface between the MASAs and other CU units. It also determines which MASM should store data and, during data retrieval, which MASM contains the data. The MASA is the device used to store program instructions and data.

4.19 Operations the MASM is capable of executing are:

- Read (fullword)
- Read and clear (fullword)
- Read and clear (halfword)
- Read and clear (byte)
- Write (fullword)
- Write (halfword)
- Write (byte).

4.20 Control of the MASC is provided by the CC or DMAC. These control signals are necessary to initiate the operation to be performed by the MASC.

B. Peripheral Control Frame

Storage Module Drive - Disk File Controller (SMD-DFC)

4.21 The 3B20D Model 1 computer uses microprocessor-based intelligent disk file controllers (DFCs). Various versions of SMD-DFCs have been used in the 3B20D computer. Each newer version provides increased capabilities and functions over their predecessor DFC.

4.22 The SMD-DFC provides microprocessor control which interprets and executes commands from the CC to cause information transfers to and from the disk drives. Each controller can support up to eight disk drive units.

4.23 The controller is microprogrammed to accept jobs from the disk driver software in the CC. The controller assigns each job to a disk drive work queue. When a drive is selected and its heads are positioned correctly for a given job, the controller begins the requested data transfer between the disk drive and the main store, through the DMA-I/O unit. When the transfer is completed, the controller notifies the CC by means of an interrupt signal.

4.24 The SMD-DFC will support only those disk drives with a SMD interface. Various drive capacities have been offered with the 3B20D as new start options and as retrofit features.

Input/Output Processor

4.25 The input/output processor (IOP) (see Figure 13) interfaces the duplex 3B20D Model 1 computer with as many as four groups of four peripheral devices so that transfers of data between the devices and main store may be made without requiring CC control. This relieves the CC of much of the load of routine control of data transfers and allows it to be better used as a system controller.

4.26 A 16-bit microprocessor called the peripheral interface controller (PIC) connects to the DSCH of the CC through a DDSBS and connects to as many as four PCs. One to four devices may be connected to each PC.

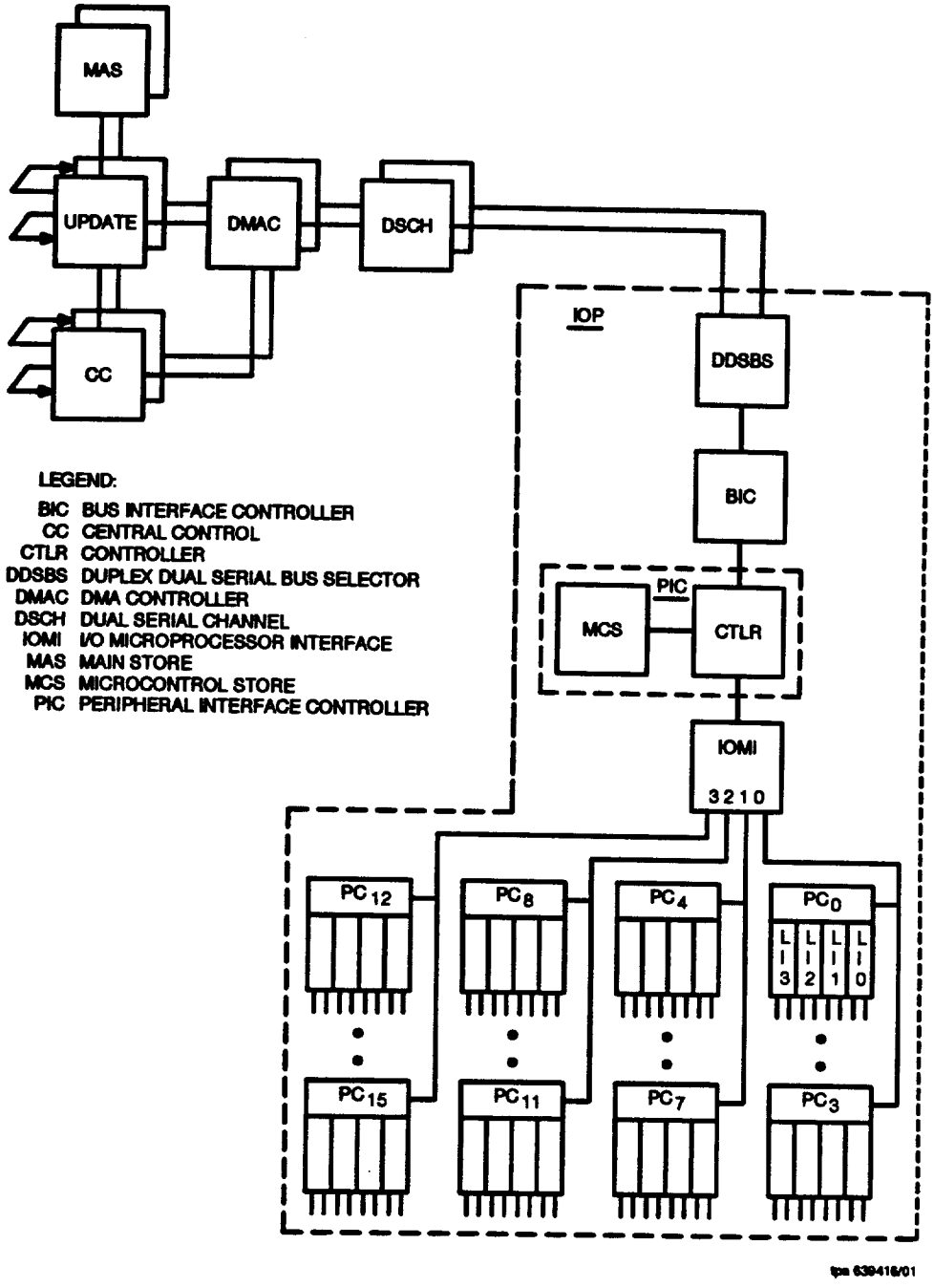

Figure 13. Input/Output Processor Block Diagram

C. Moving Head Disk Frame

4.27 The MHD frame contains the disk file inverter, power control, and the MHD drive. The disk file inverter provides a constant 208 V source (208 V commercial or inverting –48 V DC to 208 V AC) to the MHD drive. The PCU provides for the power control switch to control power to the MHD drive. The MHD is used to store maintenance, application software, DMERT Operating System software, and initialization data.

4.28 The disk file system consists of as many as eight commercially built disk drives and associated controllers. The moving head disk drives are available in 80-megabyte or 300-megabyte storage capacities. Each version uses one recording-reproducing head for each disk surface. A disk pack for an 80-megabyte drive consists of 3 disks with 6 usable surfaces. Five surfaces are used for data storage, while the sixth surface is used for head positioning information. A disk pack for the 300-megabyte disk drive has 20 surfaces on 10 disks. Nineteen surfaces are used for data storage and one surface is used for head positioning information.

4.29 Each data surface has 815 tracks, arranged concentrically. Each track has a storage capacity of 20,160 bytes. The group of tracks occupying the same physical position on all the disks is called a "cylinder". The surfaces are divided into pie-shaped sectors, one of which is the smallest block of information that is read or written.

4.30 The disks on both versions of the disk drive rotate at 3600 rpm.

D. Magnetic Tape Frame

4.31 The magnetic tape (MT) frame contains the tape transport unit(s) that make up the magnetic tape system. It is a peripheral device connected to the IOP. The tape transport records and stores billing, application software, recent change, utility, system update, and audit data.

4.32 The magnetic tape system consists of a tape controller, a tape formatter, and a tape unit. The tape controller is a microprocessor-controlled circuit which interfaces the CC and the tape formatter-tape unit. The function of the tape controller is to transfer blocks of data between the Model 1 computer main store and the tape units. A maximum data transfer rate of 40,000 bytes per second can be attained. The tape controller is connected to its associated tape formatter and tape units by means of a cable with a maximum length of 250 feet.

4.33 The tape formatter can address and control up to four tape units. The formatter accepts commands to automatically write an identification at the beginning-of-tape mark, write an end-of-file mark, format blocks of data to be written on tape, and to interpret data read from tape.

4.34 The tape unit accepts a single reel of half-inch wide tape on a reel up to 10 1/2 inches in diameter. Data is read or written at a speed of 25 inches per second, while a fast forward or reverse speed of 100 inches per second is available. During all write operations, the mode for detecting any recording errors is read-after-write. The

tape unit accepts commands for rewind, forward/reverse, read/write, erase, write end-of-file mark, and off-line. Status indications for beginning of tape, end of tape, on-line, write-enable ring, rewinding, and ready are returned to the system.

4.35 The tape unit reads or writes nine tracks on standard magnetic tape. Data can be recorded at 1600 bits per inch in a phase-encoded format, or 800 bits per inch in a non-return-to-zero format. Each record is written with both vertical and longitudinal parity and the tape controller is capable of correcting single-track errors on reads.

E. Power Distribution Frame

4.36 The power distribution frame (PDF) is used as a distribution frame for the –48 V DC used in the 3B20D Model 1 computer. The PDF provides additional fusing for the –48 V DC and also provides a charging facility. The charging facility is used to precharge capacitive loads internal and external to the PDF, at the PDF. Internal capacitors on the PDF are used to control power transients.

5. Maintenance

5.01 The maintenance objective of the 3B20D Model 1 computer is to provide a system with a cumulative processor downtime of not more than an average of two hours per system over a 40-year period.

5.02 Extensive use of self-checking, plus duplication of equipment to provide an operating spare in case of serious fault, is employed to meet the maintenance objectives. A duplex computer system is the primary method used to ensure continuous system operation. The on-line CU keeps the off-line memory updated on each memory write so that it always agrees with the on-line memory. The basic fault recovery technique is to switch the off-line CU on-line. Once the faulty CU is off-line, further fault diagnostic and location procedures, both hardware and software, may be used. The MCH is the circuit used to switch CUs when an error occurs; it is then used by the on-line CU to exercise and diagnose the off-line system.

5.03 The maintenance channel provides a serial channel link into the microcontrol structure of the CC. This provides maintenance and diagnostic access between the CCs of a duplex system. The MCH functions in the same manner as a DSCH, although it is not considered to be a part of the I/O system. Refer to Figure 14.

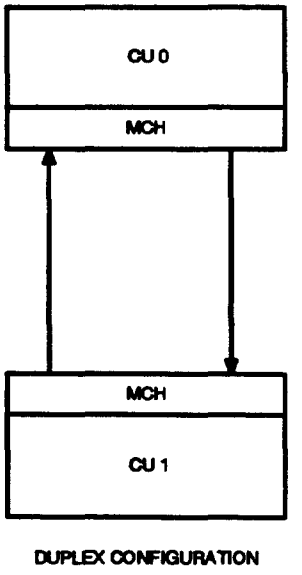

Figure 14. 3B20D Model 1 Computer Maintenance Channel Configuration

5.04 Maintenance procedures are divided into nondeferrable and deferrable categories. Nondeferrable functions center around fault recovery, which usually requires a processor switch with a resulting equipment reconfiguration. Deferrable maintenance normally involves the man-machine interface, since human intervention usually results in comparatively long downtimes.

5.05 An emergency action interface (EAI) is a part of the CC and provides some manual control to be used primarily for troubleshooting. The EAI unit is located in the CC frame adjacent to the MAS module. It has no controls of its own, but instead accepts signals from the serial channel input and produces control signals to initiate certain operations. Indicators on the EAI unit provide status information to the craft person. (See Table D.)

Table D. Emergency Action Interface Unit Indicators and Functions

Indicator	Function
Run	Indicates CU is executing microinstructions.
Active	Indicates that CU is on line.
Emergency Action Enable	Indicates that this CU is in the emergency action mode, enabling control of other EAI functions.
Forced On-Line	Indicates this CU has been forced into the on-line mode.
Forced Off-Line	Indicates this CU has been forced into the off-line mode.
Diagnostic Display	A one-digit hexadecimal display which indicates the last successfully executed step of the sanity diagnostic sequence, providing a software-driven verification of system sanity in the event of a TTY or duplex IOP failure.

5.06 The KS-22497 video terminal and a Teletype Corporation model 40 printer are provided to permit communication with the 3B20D Model 1 computer. The operator types commands on the terminal keyboard; status indications and return messages are displayed on the video terminal. Results of diagnostic tests may be printed out on the model 40 printer. The video terminal can display reversed video and flashing characters, and has a split screen capability so that status messages and other long term information can be continuously displayed on a part of the screen while other messages and displays may be placed on the other parts of the screen.

5.07 The video terminal connects to the CC through the maintenance teletypewriter peripheral controller (MTTYPC) in the peripheral control frame, and the EAI unit located in the CC. Remote access to the CC through the EAI unit is made via a data link on a dedicated port in the MTTYPC. Figure 15 depicts maintenance access from the local and remote points.

5.08 A microlevel test set (MLTS) is available which provides access to the microstore address bus, microstore data bus, maintenance channel bus, and bidirectional gating bus. This access is through a UN16 circuit pack installed at location 040 in the CC. The MLTS provides a method of inputting microinstructions and monitoring operations of the CC.

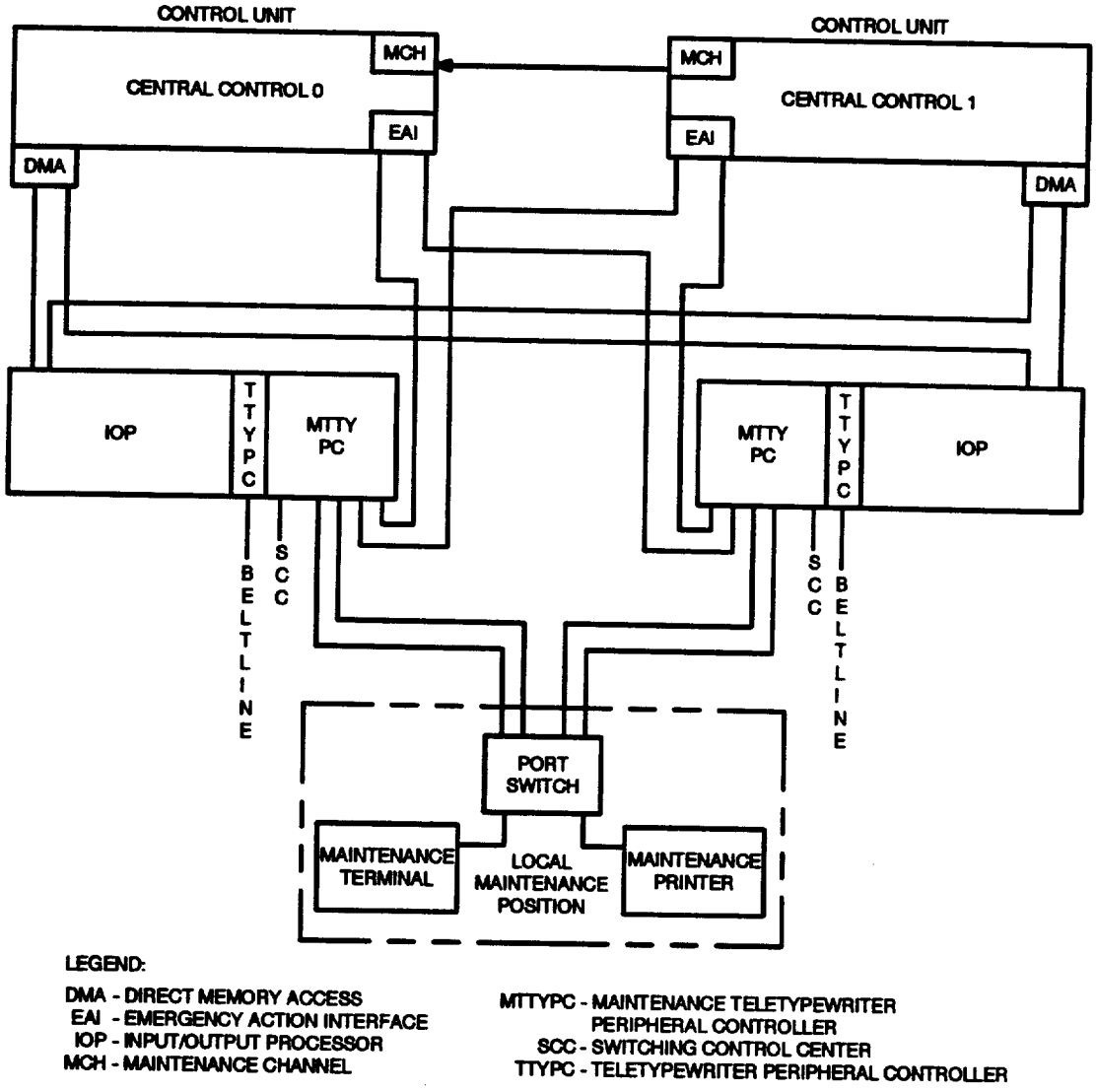

Figure 15. 3B20D Model 1 Computer Maintenance Interfaces

6. Growth

6.01 The following units are considered to be growth and/or optional units, use of which is dependent upon the application.

(a) CU Frame

- I/O Channels—There are a maximum of seven I/O channels available. These may be any combination of the SCH, ACHI, and/or DSCH.

  There may be a maximum of two DMACs in the DMA facility, each of which may be equipped with a maximum of four DSCHs.

- MASM—The CU may be equipped with a maximum of two MASMs. Each MASM may be equipped with a maximum of 8 MASAs (128K words per MASA).
- Power—The CU may contain two to four 244B DC-to-DC converters depending on the +5 V DC current requirements of the application.
- CC—The CC may be equipped with the following options:

  — CACHE

  — MCH

  — MASU

(b) Peripheral Control Frame

- IOP growth unit may be added to IOP basic unit
- IOP basic and IOP growth units may be installed with a maximum of eight PCs per each (four per community).

(c) IOP Growth Frame(s) can be added for additional IOPs. Each frame can contain up to two IOPs (IOP basic unit, or IOP basic unit and IOP growth unit).

(d) DFC Growth Frame(s) can be added for additional DFCs. Each frame can contain up to two DFCs.

(e) MHD Frame(s) may be added in any number depending on the application. However, a DFC can support only 8 MHD frames.

(f) MT Frame(s) may be added in any number depending on the application. Each frame may contain up to two tape transports. However, a tape transport with formatter can support up to four tape transports with formatters.

(g) PDF Frame(s) may be expanded by the addition of panels. These are:

- Filter-Fuse Panels (maximum of 5)
- Circuit-Breaker Panels (maximum of 2).

7. Features

7.01 The following features can be added to the 3B20D Model 1 computer through growth and retrofit. Software may be updated through retrofit or broadcast warning messages.

Expanded Main Memory

7.02 Main store module 0 can be expanded to the maximum capacity of 16-megabytes by replacing main store array circuit packs with the 2-megabyte circuit packs (TN56). The main store controller (UN39 and UN40) circuit packs must be changed to a single UN59B.

Extended Main Memory

7.03 The extended main memory feature provides the option of increasing the amount of memory for a 3B20D Model 1 computer, in increments of 2 megabytes, from 16 to a maximum of 32 megabytes. The system must be equipped with the extended main memory controller boards (2-UN10C, UN11C, UN43D, UN59C, and UN133B) and 16 megabytes of TN56 memory in each CU.

Microstore

7.04 A 4K writable microstore (UN48B) is available. This will free microstore slots for other uses. The UN28 programmable microstore is updated to a UN28B and the UN44 microstore controller is changed to a UN135.

Fast Backup

7.05 A new streaming tape drive (KS-23113) has the capability of writing tapes with a 6250 bits per inch density and of using 6K byte data blocks to speed system backup. This new tape drive requires the dual density magnetic tape controller circuit pack (UN145). Changes were also made in the tape writer program to accommodate this tape drive.

Fixed-Medium Disks

7.06 The 340-megabyte disk drives are available through retrofit. These larger capacity disk drives are smaller, more reliable, and require less power and maintenance. One disadvantage is that disk packs cannot be removed for system backup. The new streaming tape drive somewhat alleviates this disadvantage.

Critical Indicator Administrator

7.07 Effective with *UNIX* RTR Operating System Release 1, critical indicators on the maintenance terminal can be routed to a terminal in a remote maintenance center (other than the switching control center). This feature requires growing a TN75 signal data link controller and changing the unit control block in the equipment configuration database. Software for this feature is available in the basic load.

Remote Terminal Printer

7.08 The remote terminal printer is an add-on feature for *UNIX* RTR Operating System Release 1. This feature permits an application to duplicate the maintenance terminal and the receive-only printer at a remote location. The remote maintenance terminal must have an intelligent printer port. This feature requires a dedicated TN74 teletypewriter controller in the input/output processor, sending and receiving data sets (modems), and phone line. The remote receive-only printer plugs into the terminal. Software is updated through a broadcast warning message.

A. SCSI Disk Cabinet (Optional)

7.09 The SCSI disk cabinet is used with the units shown in Figure 16 when converting a 3B20D Model 1 computer having SMD-type disk file controllers to one having SCSI-type disk file controllers. This capability is optional only with the proper version of operating system software. The SCSI disk cabinet contains the following units:

- Power distribution unit
- SCSI DFC (2 units)
- Cooling unit
- SCSI disk unit package (up to 16).

Power Distribution Unit

7.10 This unit distributes power to and provides fusing for the units contained in the SCSI disk cabinet.

Disk File Controller

7.11 The SCSI DFC interfaces the SCSI disks to the 3B20D computer. In providing this interface, the DFC performs job control, timing, error handling, and SCSI bus protocol. The SCSI DFC supports up to 8 SCSI MHDs.

Cooling Unit

7.12 The high packaging density of the components on the SCSI DFC circuit boards require the use of forced air cooling. Each cooling unit is powered by -48 V DC and has failure alarms.

Disk Unit Package

7.13 Each SCSI disk unit package (DUP) contains a SCSI disk drive, power supply, power switch, fan, and identity selector switch. Connectors are provided at the rear of the unit to allow attachment to the SCSI bus, input power, and scan/alarm grids.

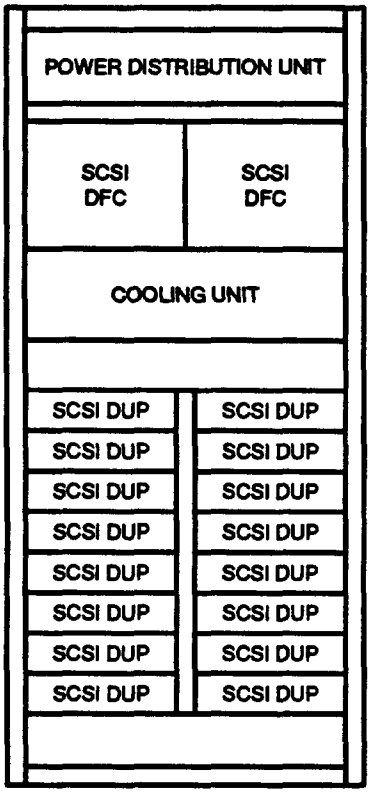

Figure 16. SCSI Disk Cabinet

7.14

8. References

8.01 The following AT&T Practices contain additional information pertaining to the 3B20D Model 1 computer.

Practice	Title
Description	
AT&T 254-001-031	*AT&T 3B20D Model 1 Computer, Equipment Test List*
AT&T 254-301-000	*AT&T 3B20D Model 1 Computer, System Documentation, Description and Organization*
AT&T 254-301-115	*AT&T 3B20D Model 1 Computer, Teletypewriter/Printer System, Description*

AT&T 254-301-810 *AT&T 3B20D Model 1 Computer, Test Equipment, Description*

Description and Theory of Operation

AT&T 254-301-010 *AT&T 3B20D Model 1 Computer, Central Control, Description and Theory of Operation*

AT&T 254-301-020 *AT&T 3B20D Model 1 Computer, Power Systems, Description and Theory of Operation*

AT&T 354-301-100 *AT&T 3B20D Model 1 Computer, Input/Output Interfaces, Description and Theory of Operation*

AT&T 254-301-105 *AT&T 3B20D Model 1 Computer, Input/Output Processor, Description and Theory of Operation*

AT&T 254-301-110 *AT&T 3B20D Model 1 Computer, Input/Output Processor Peripheral Controllers, Description and Theory of Operation*

AT&T 254-301-200 *AT&T 3B20D Model 1 Computer, Main Store, Description and Theory of Operation*

AT&T 254-301-210 *AT&T 3B20D Model 1 Computer, Moving Head Disk Drive, General Description*

AT&T 254-301-215 *AT&T 3B20D Model 1 Computer, Disk File Controller, Description and Theory of Operation*

AT&T 254-301-220 *AT&T 3B20D Model 1 Computer, Magnetic Tape System, General Description*

Procedural and Maintenance

AT&T 254-301-800 *AT&T 3B20D Model 1 Computer, Emergency Action Procedures, Description*

AT&T 254-301-809 *AT&T 3B20D Model 1 Computer, Acceptance Test Plan*

Task Oriented Practices (TOP)

AT&T 254-301-811 *AT&T 3B20D Model 1 Computer, Office Equipment*

AT&T 254-301-812 *AT&T 3B20D Model 1 Computer, Trouble Clearing*

Software Support Documentation

AT&T 254-341-000 *AT&T 3B20D Model 1 Computer, Duplex Multi-Environment Real-Time Operating System*

AT&T 254-341-020 *AT&T 3B20D Model 1 Computer, Glossary and System Calls, Duplex Multi-Environment Real-Time Operating System*

AT&T 254-341-100 *AT&T 3B20D Model 1 Computer. File System, Duplex Multi-Environment Real-Time Operating System*

AT&T 254-341-105	*AT&T 3B20D Model 1 Computer, Input/Output and Data Management, Duplex Multi-Environment Real-Time Operating System*
AT&T 254-341-110	*AT&T 3B20D Model 1 Computer,Software Management and Basic Kernel Functions, Duplex Multi-Environment Real-Time Operating System*
AT&T 254-341-115	*AT&T 3B20D Model 1 Computer, System Utilities, Duplex Multi-Environment Real-Time Operating System*
AT&T 254-341-120	*AT&T 3B20D Model 1 Computer, DMERT Interface and Integrity Facility, Duplex Multienvironment Real-Time Operating System*
AT&T 254-341-200	*AT&T 3B20D Model 1 Computer, Initialization and Recovery, Duplex Multienvironment Real-Time Operating System*
AT&T 254-341-210	*AT&T 3B20D Model 1 Computer, Configuration Management, Duplex Multienvironment Real-Time Operating System*
AT&T 254-341-220	*AT&T 3B20D Model 1 Computer, Maintenance Management and Diagnostics, Duplex Multienvironment Real-Time Operating System*
AT&T 254-302-213	*AT&T 3B20D Model 2 and Model 3 Computers, General Description, Small Computer System Interface, Disk Unit Package*
AT&T 254-302-216	*AT&T 3B20D Model 2 and Model 3 Computers, Description and Theory of Operation, Small Computer System Interface, Disk File Controller.*

Table E contains a brief description of the contents of those documents listed which contain detailed information relating to the 3B20D Model 1 computer.

Table E. Document Contents

Practice	Details
254-001-031	***Equipment Test List*** — This practice contains information for routine maintenance, class, and frequency of test.
254-301-005	***AT&T 3B20D Model 1 Computer General Description*** — This practice describes the 3B20D Model 1 Computer in general terms with the following details covered: configuration, interfaces, equipment physical description, equipment functional description, and maintenance.
254-301-010	***Central Control*** — This practice provides description and theory of operation of the Central Control. Items described are: physical description, interface, functional description, theory of operation, power requirements, and maintenance.
254-301-020	***Power Systems*** — This practice provides a description and the theory of operations of the power system used in the 3B20D Model 1 Computer system. Items described are: power distribution frame, frame power units, inverters, DC-to-DC converters, power control switch, power distribution, power interfaces, control, and maintenance.
254-301-100	***Input/Output Interfaces*** — This practice provides a description and theory of operation of the input/output channels which include: serial channel, dual serial channel, direct memory access channel, and the application channel interface. These units provide the interface between peripheral units and the 3B20D Model 1 Computer. Items described are: physical description, interfaces, functional description, theory of operation, power requirements, and maintenance.
254-301-105	***Input/Output Processor*** — This practice provides a description and theory of operation of the IOP used in the 3B20D Model 1 computer and its applications. The IOP is a flexible peripheral unit that provides an interface between the main store and peripheral controllers. Items described are: physical description, interfaces, configuration, functional description, theory of operations, power requirements, and maintenance.
254-301-110	***Input/Output Processor Peripheral Controllers*** — This practice provides a description and theory of operations that are connected to the IOP and considered part of the computer system. Peripheral controllers described are the teletypewriter controller, scanner distributor, maintenance teletypewriter controller, nine track type controller, etc. Items described are: physical description, interfaces, functional description, theory of operation, power requirements, and maintenance.

Table E. Document Contents (Contd)

Practice	Details
AT&T 254-301-115	***Teletypewriter/Printer*** — This practice describes the teletypewriter and printer used in the 3B20D Model 1 computer. Items documented are: physical description, interface, functional description, teletypewriter/printer configuration, power, and maintenance.
AT&T 254-301-200	***Main Store*** — This practice provides a description and theory of operation of the main store used in the 3B20D Model 1 computer system. Description of the overall operation of the main store is provided in detail by a physical description, interfaces, functional description, theory of operation, power, and maintenance.
AT&T 254-301-210	***Moving Head Disk Drive, General Description*** — This practice provides a description of the disk drives available for use in the 3B20D Model 1 computer. Disk drives available are KS-21996, L2; KS-21996, L3 (80 megabytes); KS-22072, L1; and KS-22072, L2 (300 megabytes). Information is provided on physical description, interfaces, functional description, power, and maintenance.
AT&T 254-301-215	***Disk File Controller*** — This practice provides a description and theory of operation of the file store controller including options. Detailed information is presented on physical description, configuration, functional description, interfaces, power, and maintenance.
AT&T 254-301-220	***Magnetic Tape System, General Description*** — This practice provides a description of the KS-22091 tape system used in the 3B20D Model 1 computer. Information is provided on physical description, interfaces, functional description, power, and maintenance.
AT&T 254-301-800	***Emergency Action Procedures*** — This practice provides a description of emergency action facilities available to the craft. This includes manual and automatic facilities. Also, described are responses to emergency situations.
AT&T 254-301-801	***Maintenance Data*** — This practice provides a description of maintenance data (in a handbook format) that would be useful to the craft as a quick reference source.
AT&T 254-301-809	***Acceptance Test Plan*** — This practice provides a description of the acceptance test plan to assist the operating telephone company in planning. Information provides data for cutover/turnover of system from AT&T to the operating company.

Table E. Document Contents (Contd)

Practice	Details
AT&T 254-301-810	***Test Equipment*** — This practice provides a description of test equipment required to maintain a 3B20D Model 1 computer system. System test equipment and external test equipment are also described in this practice.
AT&T 254-301-811	***AT&T 3B20D Model 1 Computer Task Oriented Practice*** — This volume provides the routine, acceptance, and company order procedures for a 3B20D Model 1 computer system. The procedures are task-oriented, enabling access to all data necessary to complete a task initiated by some stimulus (eg, alarm, trouble report, service order, etc). Each procedure is presented in three distinct levels of detail (layers) enabling more experienced craft personnel to bypass the more detailed instructions for tasks that can be performed from memory. The trouble clearing procedures are accessed in response to a system malfunction.
AT&T 254-301-812	***AT&T 3B20D Model 1 Computer Task Oriented Practice*** — This volume provides trouble clearing procedures to maintain the 3B20D Model 1 computer system.
AT&T 254-302-213	***AT&T 3B20D Model 2 and 3 Computers General Description Small Computer System Interface Disk Unit Package*** — This practice describes the small computer system interface (SCSI) disk unit package (DUP) used in the AT&T 3B20D Model 2 and Model 3 computers. This practice illustrates the equipment and discusses the DUP as a computer peripheral unit.
AT&T 254-302-216	***AT&T 3B20D Model 2 and 3 Computers Description and Theory of Operation Small Computer System Interface Disk File Controller*** — This practice provides a physical and functional description and theory of operation for the Small Computer System Interface Disk File Controller (SCSI-DFC). The SCSI-DFC is the logic unit that allows the SCSI disk drives to be connected to the 3B20D computer.
AT&T 254-341-000	***Duplex Multienvironment Real-Time Operating System*** — This practice provides an overview of the operating system and a base of reference for succeeding practices. It provides general basic operating system information for reference. The initial introduction to DMERT is via an explanation of the structure and hierarchy, the basic functions that are performed, what is provided, and an overview of available services and how requested a different levels of hierarchy. It presents an introduction to succeeding practices and a resume of basic functions and services to be described in each. Also, this practice contains a cross-reference for each practice and a program reference of the program listing (PR) number block in which the programs pertaining to each of the areas can be located.

Table E. Document Contents (Contd)

Practice	Details
AT&T 254-341-020	***Glossary and System Calls*** — The contents of this practice is divided into two sections. The first is a glossary of all terms and definitions pertaining to the DMERT Operating System. It is an abstract of the terms and definitions used throughout all sections. The second section is a comprehensive list, with a brief explanation, of the essential system calls and library functions which are used to obtain services from the operating system. These are described by a concise statement of the primary function.
AT&T 254-341-100	***File System*** — This practice provides a description of major input/output functions provided by the kernel process level and includes a description of the file system structure-directory structure-path hunting-types of files with the input/output devices as files-classes of device. The functional relationships are described in terms of the type of operation (read, write, etc) performed.
AT&T 254-341-105	***Input/Output and Data Management*** — This practice contains the functional descriptions of the various devices and associated drivers included in the operating system. The following information is included for each driver and device: the major interfaces and operations between the drivers, the kernel functions and the file system, the equipment configuration table and the configuration manager, driver and device fault detection, and recovery. Access methods and operations, redundancy, backup, and equipment hierarchy are provided. Also described are: ■ Character Input/Output—Initialization and functional relationship between the device, file system, and device driver ■ Block Input/Output—Initialization and functional relationship between the file manager, file system, and device drivers.
AT&T 254-341-110	***Software Management and Basic Kernel Functions*** — This practice provides a general description of the basic DMERT kernel functions, and the major methods of entry and services provided. These are described in terms of process creation, the means used by a process to acquire services, general functional flow between the major elements which accomplish the services, and process termination. Functional sequences are used to describe the essential functions and major processing activities.
254-341-115	***System Utilities*** — This practice provides a general functional description and information relative to the utility functions available.

Table E. Document Contents (Contd)

Practice	Details
254-341-120	***Interface and Integrity Facility*** — This practice provides a functional description of the audits (types and structures), plant measurements, and craft interface features (input/output messages, terminals, and displays) processed by the 3B20D Model 1 Computer software. Also described are the facilities used to determine the integrity (sanity) of the system.
254-341-200	***Initialization and Recovery*** — This practice describes general processor management operation and error handling. It defines basic terms and provides a functional overview of critical activities. Also, described are initialization and recovery, explanation of bootstrap activities, dead start, and processor switching.
254-341-210	***Configuration Management*** — This practice describes system configuration control functions. It covers basic definitions, general system structure, status keeping, reconfiguration, and peripheral error recovery. It includes the following basic topics: general definitions and descriptions of key data elements, general functional description of the configuration supervisor (administering sanity timers, status registers, etc). Also described are: the equipment configuration table description, access, and management; interaction and relationships between the configuration manager, equipment configuration table, and drivers. The practice also includes general explanations of the equipment structure, hierarchy, redundancy, and backup methods.
254-341-220	***Maintenance Management and Diagnostics*** — This practice contains the essential aspects of processor and peripheral diagnostics. It provides an explanation of the diagnostic philosophy, basic definitions, and general diagnostic methods. Topics include initiation of diagnostics, request handling, options, and a functional description of the diagnostics. A list of diagnostic tests, the equipment areas these apply to, what is tested, and the expected test results are provided.

9. Glossary

9.01 The following terms are defined to aid in using and understanding this practice:

Central Control—Control section of a 3B20D Model 1 computer. It consists of control circuitry, arithmetic and logic unit (ALU), rotate mask unit (RMU), general and special registers, maintenance channel, store address translator circuit, and optional cache memory.

Control Unit—That part of a 3B20D Model 1 computer which is switched on- or off-line as a unit. It consists of a CC, Main Store, DMA unit (when equipped) I/O channels, and the power unit.

Duplex—A duplex 3B20D Model 1 computer consists of duplicated control units interconnected via the maintenance channel, and all peripheral hardware required for system operation. The peripheral units may include a system status panel, TTY controller, tape data controller, and moving head disk units.

Simplex—A 3B20D Model 1 computer installation which is equipped with only one CU.

Cache Store Unit—An optional system unit which provides a high speed random access memory buffer used to reduce the apparent main store access and cycle times.

CCIO Bus—A group of leads used to interconnect the CC with its I/O channels and DMA unit. This bus is used to carry data, address, and control information.

Data Manipulation Unit—This circuit contains the rotate mask unit, logic and arithmetic functions of the CC.

Direct Memory Access Unit (DMA)—This optional system component provides main store access control for I/O devices and other processors without requiring direct control from the CC.

DMA Controller—Control circuitry for the DMA.

DMA I/O Bus—A group of leads which interconnect the DMAC with four DMA channel controllers (DCC).

Dual Serial Channel (DSCH)—Provides a 16- or 32-bit interface to I/O devices, and uses two serial signal paths in each direction.

Duplex Dual Serial Bus Selector (DDSBS)—A system component which provides the capability to connect two DSCHs from duplex CUs to a single peripheral device.

Emergency Action Interface (EAI)—System component which provides the interface between the maintenance teletypewriter and the CC.

Gating Bus—A multilead bus (usually 36 leads) which carries data between the various sections of the CC.

Hardware Sanity Timer—A hardware timer in each CC which must be periodically reset. Time-out of the timer results in fault recovery initiation.

Main Store Array—A main store memory array which provides storage for 32K words of 36 bits each.

Main Store Bus (MASB)—A group of leads which interconnect the main store, CC, MASU and DMA.

Main Store Controller (MASC)—Provides the control interface between MASB and memory devices.

Main Store Module—A system component consisting of one MASC and from 1 to 16 MSA initially providing a maximum of 2 megabytes of storage.

Main Store Update Unit (MASU)—A circuit which interconnects the MASB of duplex CCs to permit reading, writing, and updating of each main store by each CC.

Maintenance Channel (MCH)—Provides serial access to the microinstruction structure between duplex or master-slave CCs for maintenance and diagnostic purposes.

Microcontrol (MC)—That portion of the CC which controls the sequencing of the MIS and decoding of microinstructions.

Microstore (MIS)—A random access, read-only memory which contains microprograms to control CC operations and to execute instructions brought from MAS.

Off-line—See "on-line".

ON-Line—A system component which is actively performing its function and is engaged in executing system commands is said to be "on-line". A CU which is actually in control of its system in a duplex configuration is on-line, while its companion CU is off-line. The off-line unit may be performing some functions such as diagnostics, but it is not in control of the 3B20D Model 1 computer.

Serial Channel (SCH)—A system component which provides a 16- or 32-bit serial interface, using one signal path in each direction.

Special Registers—A group of registers in the CC which perform unique functions within the CC. These registers contain specialized data concerning system operation, and are not usually available for external use. These registers include the channel data register, bidirectional gating register, pulse point register, interrupt set register, interrupt mask register, timer program status register, hardware status register, system status register, error register, and related circuitry.

Stop-and-Switch—A hardware signal generated by error detection circuits within the on-line CC which causes the on-line CU to be halted and the off-line CU to be switched on-line.

10. Acronyms and Abbreviations

10.01 The following is a list of acronyms and abbreviations used in this practice.

ACHI	Application Channel Interface
ALU	Arithmetic Logic Unit
CC	Central Control

CH	Channel
CCIO	Central Control Input/Output
CCIOB	Central Controll Input/Output Buss
CU	Central Unit
CSU	Cache Store Unit
CTRL	Controller
DDSBS	Duplex Dual Serial Bus Selector
DFC	Disk File Controller
DHA	Device Handlers
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DMA I/O	Direct Memory Access Input/Output
DSCH	Dual Serial Channel
DUP	Disk Unit Package
EIA	Electronic Industries Association
IB	Instruction Buffer
IM	Interrupt Mask
IOMI	I/O Microprocessor Interface
IOP	Input/Output Processor
IS	Interrupt Source
MAS	Main Store
MASA	Main Store Array
MASM	Main Store Module
MCH	Maintenance Channel
MHD	Moving Head Disk
MLTS	Microlevel Test Set
MT	Magnetic Tape
MTTY PC	Maintenance Teletypewriter Peripheral Controller
PC	Peripheral Controller
PD	Power Distribution
PDF	Power Distribution Frame

PIC	Peripheral Interface Controller
PSW	Program Status Word
RMU	Rotate Mask Unit
SAR	Store Address
SCC	Switching Control Center
SCH	Serial Channel
SCR	Store Control
SCSI	Small Computer System Interface
SDR	Store Data
SMD	Storage Module Drive
TTYPC	Teletypewriter Peripheral Controller

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