AT&T 3B20D Model 1 Computer Input/Output Interfaces Description and Theory of Operation

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1. Overview

1.01 This practice provides a physical and functional description and theory of operation of the input/output (I/O) interfaces between the 3B20D Model 1 Computer control unit (CU) and its periphery.

1.02 This practice is being reissued to include information about the Small Computer System Interface (SCSI). Since this is a general revision, revision arrows used to denote significant changes have been omitted. The Equipment Test lists are not affected.

1.03 This practice contains no admonishments.

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1.07 The I/O interfaces within the 3B20D Model 1 computer consist of the following:

- Direct memory access controller (DMAC)
- Serial channel (SCH)
- Dual serial channel (DSCH)
- Application channel interface (ACHI)
- Maintenance channel (MCH)
- Duplex dual serial bus selector (DDSBS).

Purpose

1.08 The purpose of the I/O interfaces is to provide a facility for connecting the CU to a number of various types of peripheral devices.

1.09 Four types of main channels are provided to facilitate communications between the CU and its peripheral devices (Figure 1). These channels are the SCH, the DSCH, (four DSCHs maximum) the ACHI, and the DMAC. These channels are located in the CU frame.

1.10 The DMAC provides a means of transferring blocks of data directly between high-speed peripheral devices (PDs) and the main store (MAS) in the CU. The DMAC is controlled by the Central Control (CC) via the central control input/output (CCIO) bus but is related functionally to the MAS and the PDs that have access to the direct memory access I/O (DIO) bus via the DSCHs.

1.11 The SCH is used to provide low- and medium-speed data transfers between the CC and PDs.

1.12 The MCH provides serial access to the microinstruction structure between duplex or master-slave CC for maintenance and diagnostic purposes (CC to CC communications). Detailed information on the MCH is contained in AT&T 254-301-010 *3B20D Computer Central Control, Theory of Operation, 3B20D Model 1 Computer.*

1.13 The ACHI provides the facility for connecting to a CC. The ACHI can be custom designed for each interfacing application.

1.14 The DSCH provides the interface between the CU and PDs requiring medium- and high-speed data transfer. Two serial data streams are simultaneously transferred between the CU and each PD via the DSCH.

1.15 The DDSBS selector provides the interface between the DSCH and its associated PDs.

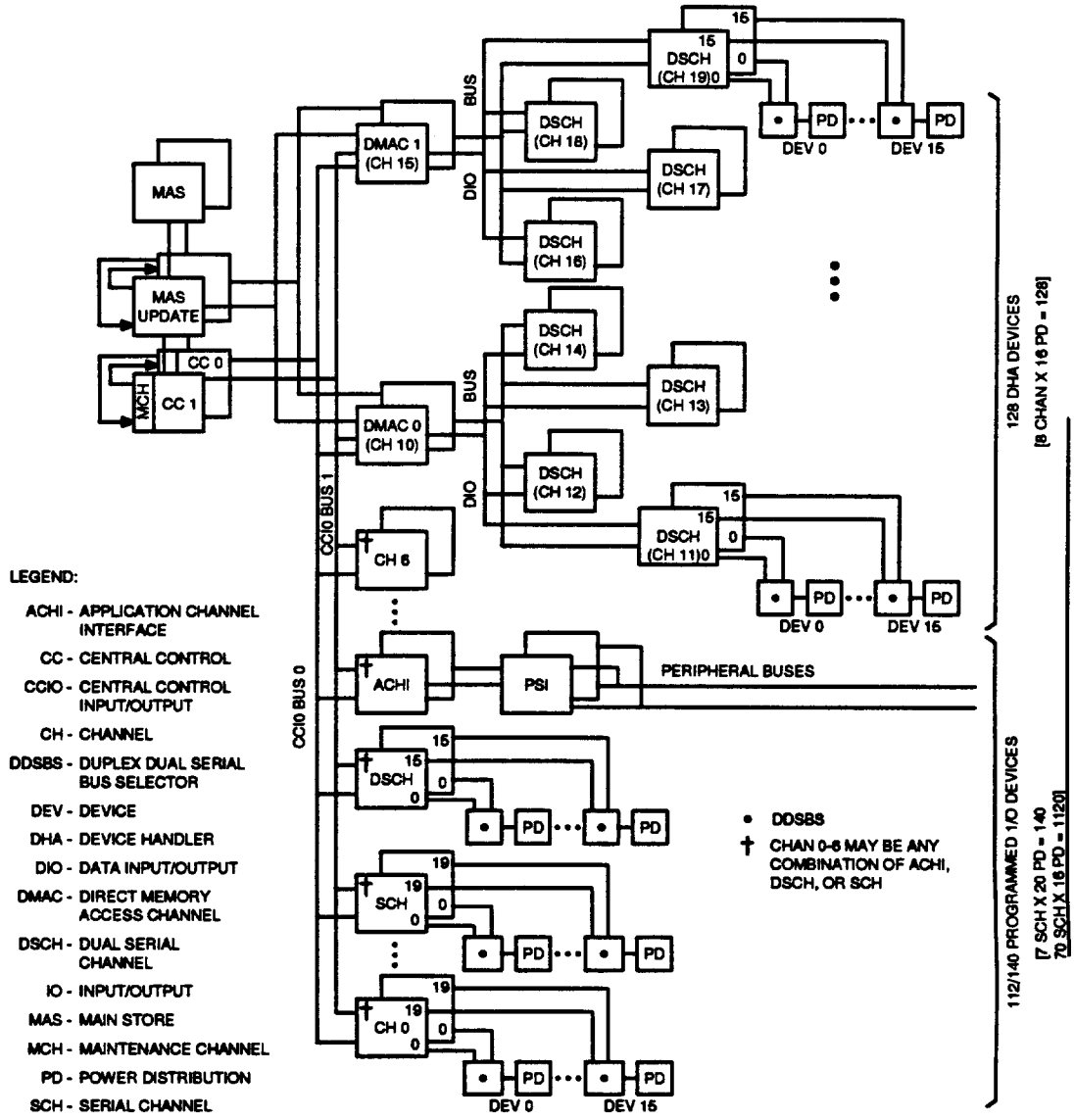


Figure 1. 3B20D Computer I/O Interfaces

Configuration

1.16 The CU can be equipped with as many as seven programmed I/O channels (SCH, ACHI, and DSCH) and as many as two DMACs. Programmed I/O channels are controlled directly by CC microcode via the CCIO bus. The DMAC provides the capability for direct memory transfers between the MAS and PDs. This reduces the real time for the CC to process I/O requests. The DIO unit can contain one or two DMACs, each of which can control a maximum of four channels (DSCH) over the DIO bus.

1.17 The SCH interfaces up to a maximum of 20 PDs via 20 pairs of private serial data cables.

1.18 The DSCH interfaces with up to a maximum of 16 PDs via 16 sets of 5-pair private serial data cables.

1.19 The ACHI is provided, as required per application, it is connected to the CC via the CCIO bus and to the PD(s) via differential DC-coupled lines. This channel extends the CCIO bus to a peripheral system interface (PSI), which is part of the application equipment. This is a 2-way transmission system that requires eight 11-pair cables.

1.20 The interface between the DSCH and PD is provided by the DDSBS selector, one per PD is required to connect a device to duplex 3B20D computers. The DDSBS selector is located within the unit requiring its functions, and is considered a subunit of the unit.

1.21 Main channels 0 and 1 (SCH, ACHI, or DSCH) are located in the CC. Main channels 2 through 6 and the DMAC (each with maximum of four DSCHs) are located in the direct memory access I/O (DIO) unit (Figure 2).

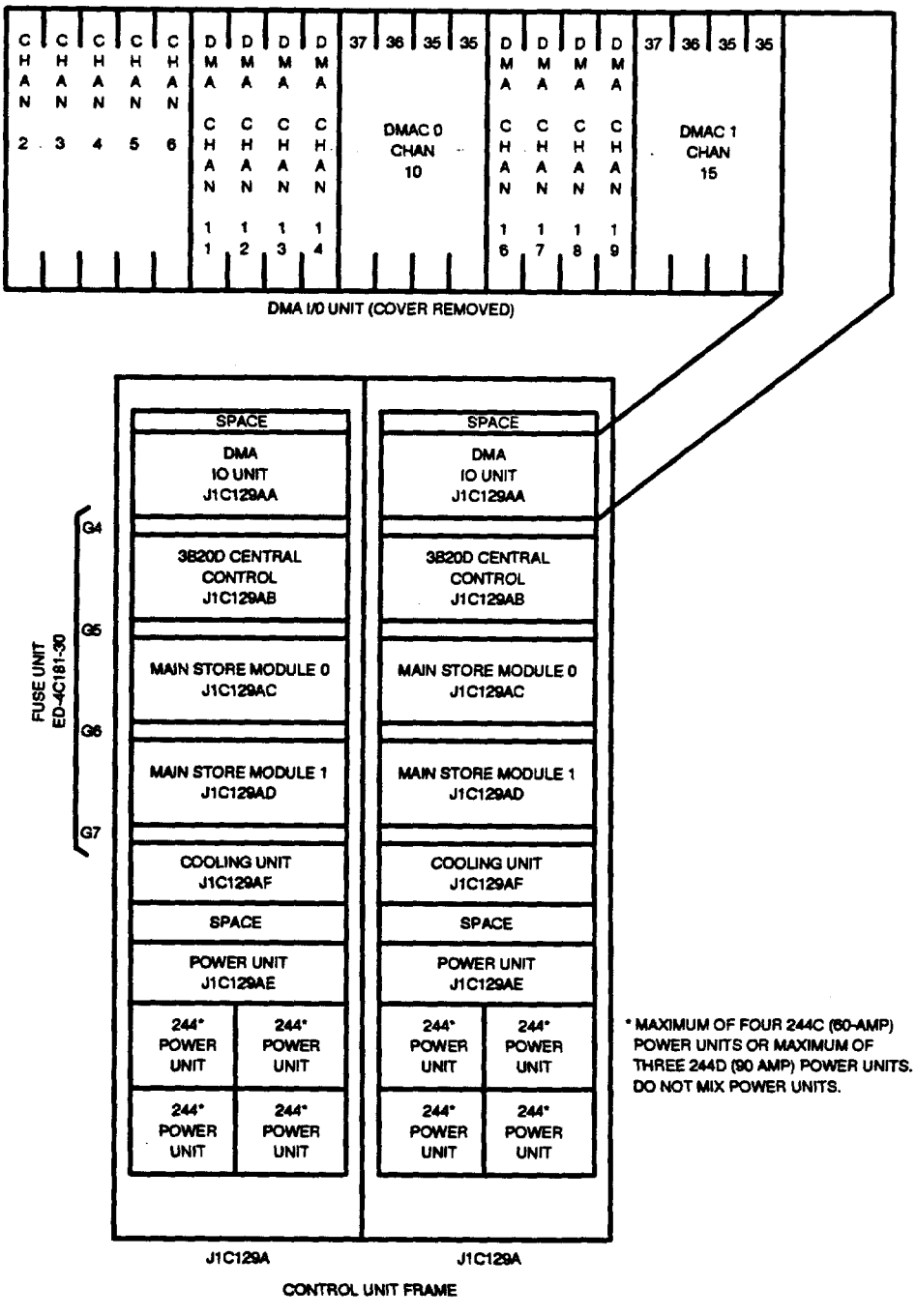


Figure 2. Control Unit Frame

2. Interfaces

2.01 The DMAC interfaces to the CC via the CCIO bus and to the MAS via the MAS bus system. The DMAC interfaces with up to four DSCHs via the DIO bus (the DSCHs are controlled by the DMAC). The DSCH interfaces to the DDSBS selector via 5-pair private serial data cable bus and the DDSBS selector interfaces to the PDs via a transistor-transistor logic (TTL) DC bus.

2.02 The SCH interfaces the CC via the CCIO bus and interfaces the PDs via an AC bus comprised of two 100-ohm serial transformer-coupled coaxial cables. The PDs are low- and medium-speed peripheral units requiring a SCH interface with the CC.

2.03 The DSCHs also can be used as a program controlled channel (not controlled by a DMAC). This DSCH interfaces the CC via the CCIO bus and interfaces the DDSBS selector via 5-pair private serial data cable bus (private serial point-to-point link). Also, the DDSBS selector interfaces the PD via a TTL DC bus.

2.04 The ACHI interfaces the CC via the CCIO bus and the application devices via differential DC paths comprised of eight 11-pair cables.

2.05 All signals transmitted between the CC via CCIO bus to the I/O channels are active low (0 volt) using TTL levels. These are described in the following paragraphs.

2.06 ***Main Channel Address:*** The CC selects a single I/O channel by transmitting the selected channels designated 3-out-of-6 code address on the 6-main channel address leads. Each CCIO bus position has a unique 3-out-of-6 code (position dependent, not device or software dependent).

2.07 ***Data and Control:*** Data and control information are transmitted from the CC to the addressed I/O channel via the (32+4 parity) data leads. Data and status are transmitted from the addressed I/O channel to the CC over these same leads. Odd parity over each of the data bytes is maintained in both directions, with the entire (32+4 parity) data word having even parity.

2.08 ***Channel Error:*** The detection of failures in the I/O channel will result in the channel error (CER) lead being set. The CC error register will then institute an error interrupt.

2.09 ***Main Channel Acknowledge:*** The I/O channel selected by the main channel address leads gates its 3-out-of-6 code main channel address onto the 6-main channel acknowledge leads in response to a control signal. A 3-out-of-6 code check circuit in the CC will detect a no response or multiple channel response condition. This will result in a bit being set in the CC error register, initiating an error interrupt.

2.10 ***Main Channel Responses:*** The channel ready (RDY) signal is used to indicate to the CC when an I/O operation has completed. The CC transmits a control signal (RD) to the channel and tests the RDY signal to determine whether the operation

has completed. Requests to read channel data will not initiate a ready response until the data has been received from the PD, latched into the channel data buffer, and gated onto the CCIO bus. The RDY response to other control signals is determined by the channel addressed. It is immediate to all other control signals addressed to channels on the CCIO bus. However, if the addressed channel is on the DIO bus (connected to a DMAC), RDY will not be returned immediately because the DMAC can not gate the command to the DSCH immediately. The microcode will transfer to an RD loop waiting until the DMAC responds to the command with an RDY. The absence of an all seems well (ASW) signal is used by the channel to signal the CC that an I/O operation was terminated because of an error condition in the PD. Data parity errors are detected by the CC and DMAC but not by the other channels. Errors signified by the CCIO bus ASW lead do not initiate hardware checks but are registered in the condition code register. A maintenance response (MR) signal is returned by a SCH (if a 101 return code was received from the PD), however, the DSCH, ACHI, and DMAC will never activate (set) the MR lead.

2.11 The CC controls the operation of the I/O channels by transmitting control signals (pulses) to the channels. Each control signal initiates an operation to be performed by the channel. The 12 control signals are described in the following paragraphs.

2.12 ***Write the Channel Control/Address Register (WCA):*** The WCA is used as the control signal to latch control information and device address data into the control/address register of the addressed I/O channel. The acknowledge (ACK) and the channel RDY response signals will be returned to acknowledge reception of the control signal. The channel will report an error via the CER signal if its control/address register is presently full. Once the control information and address data has been successfully loaded into the control/address register, the channel initiates the requested operation (except for the ACHI).

2.13 ***Write the Channel Data Buffer (WD):*** The WD is used as the control signal to latch data into the data buffer of the address I/O channel. Signals ACK and ASW are transmitted to the 3B20D computer CC to acknowledge reception of the control signal. If the addressed channel (DSCH) is on the DIO bus, the DMAC gates the data into the DMAC CCIO data buffer register but does not transmit it to the channel until reception of a WCA signal. After the WCA is received by the DMAC, the DMAC transmits data contained in the CCIO status buffer and the CCIO data buffer to the addressed channel (specified during the WCA operation).

2.14 ***Read the Channel Data Buffer (RD):*** The RD signal usually follows a series of control pulses that have initiated an action in the channel. The channel utilizes the RD to indicate when the requested action is completed. At this time, the channel will return RDY on reception of the RD signal. If the operation is supposed to return data, the channel data buffer register will send the results to the CC. If no errors were detected during the operation, ASW will also be returned to the CC. However, if a PD error is detected during the I/O operation, the ASW signal is not sent to the CC during the acknowledgment sequence. An MR is set by the SCH if it received an MR from the PD. The RDY signal is not transmitted to the CC if the channel data buffer register is not full (this indicates that the I/O operation is incomplete). The DMAC does not

transmit the RDY signal for an RD signal to one of its DSCHs until the DSCH status and data information have been read into the DMAC status and data buffer registers. All CC to DMAC via the DSCH communications initiate a read the channel status register (RST) signal to that channel by the DMAC before the RDY signal is returned to the CC.

2.15 ***Read the Channel Status Register (RST):*** Reception of a RST signal from the CC by the addressed channel results in the gating of the channel status onto the CCIO bus. Also, the channel sends the ACK, ASW, and RDY signals to the CC. If the addressed channel is connected to the DIO bus, the DMAC transmits the data in its CCIO status buffer register to the CC.

2.16 ***Idle Channel Sequencer (IDLE):*** Upon the reception of the IDLE signal from the CC, the addressed channel is initialized. However, channel errors are not cleared. The DMAC will only reset its CCIO interface.

2.17 ***Read Channel Service Request (RSR):*** The reception of an RSR signal causes the addressed channel to gate the contents of its service request registers onto the CCIO bus. Signals ACK, ASW, and RDY are transmitted to the CC to acknowledge receipt of the RSR signal (RDY is not provided for DMAC channel). This signal (RSR) is acknowledged only by the DSCHs, ACHI, and when a DMAC DSCH is addressed (not by the SCH or DMAC.

2.18 ***Read Channel Interrupt State (RINT):*** Receipt of RINT from the CC results in the channel gating its interrupt state onto the CCIO bus. The channel also transmits ACK, ASW, and RDY signals to the CC (RDY is not provided for DMAC channel).

2.19 ***Clear Channel Errors (CLRER):*** When the channel receives the CLRER signal from the CC, it initializes and clears its channel error registers. Then the channel transmits ACK, ASW, and RDY signals to the CC (RDY is not provided for DMAC channel).

2.20 ***I/O Interrupt Acknowledge (IACK):*** On reception of the IACK signal from the CC, each main channel gates its interrupt state onto an assigned data bit lead. Bit 0 is assigned to channel 0, and bit 1 is assigned to channel 1, etc. Bits 10 through 19 are assigned to the DMAC and its associated I/O channels. Also, the channel responds to IACK by transmitting ACK, ASW, and RDY signals to the CC.

2.21 ***Channel Error Acknowledge (EACK):*** Receipt of the EACK signal from the 3B20D computer CC causes the channel to gate its error state onto assigned data leads. Bit 0 is assigned to channel 0, bit 1 is assigned to channel 1, etc. Bits 10 through 19 are assigned to the DMAC and its associated I/O channels. The main channels return ACK, ASW, and RDY signals to the CC.

2.22 ***Service Request Acknowledge (SRACK):*** Receipt of the SRACK signal from the 3B20D computer CC causes the channel to gate its service request state onto assigned data leads. Bit 0 is assigned to channel 0, bit 1 is assigned channel 1, etc. There is no response to this signal by the DMAC and its associated I/O channels. The

addressed channels return ACK, ASW, and RDY signals to the CC. This signal (SRACK) is not acknowledged by the SCH.

2.23 ***I/O Inhibit (INH):*** The INH signal is generated by the CC, as a DC signal that is held active by the off-line CC to disable I/O operations in the off-line CC. To facilitate I/O channel diagnostics, INH can be made inactive on any channel via an override command loaded into the channel control/address buffer register.

2.24 The DMAC interfaces the DSCHs (maximum of four) via the DIO bus (Figure 1). All signals are at 5-volt TTL levels and are active low. These signals are described in the following paragraphs.

2.25 ***DMAC Channel Request:*** Each of the four DMAC channels (DSCHs) has an assigned service input to the DMAC (one lead for each DSCH). These requests are identified and executed by the DMAC using fixed priority assignments.

2.26 ***Main Channel Address:*** This signal is used by the DMAC to select a single DSCH. The DMAC transmits the assigned 3-out-of-6 code address signal onto the address leads of the DIO bus.

2.27 ***Main Channel Address Check:*** After the DSCH receives this signal from the DMAC, the addressed DSCH gates its 3-out-of-6 code address onto the DIO bus acknowledge leads. A check circuit in the DMAC sets the channel error lead if an invalid 3-out-of-6 code is detected.

2.28 ***Data and Control:*** Data and control information are transmitted between the DMAC and its DSCHs via the 36 data leads (32 data +4 parity). With odd parity maintained over the 8-bit segments and even parity maintained over the entire data word (32 data bits +4 parity bits).

2.29 ***Channel Responses:*** The channel (DSCH) ready and ASW leads are used to check the DMAC to DSCH communications. The DMAC transmits a control signal to the channel and tests the ready and ASW signals to determine if the operation was successfully completed. (The DMAC expects RDY and ASW on every communication to its DSCHs.)

2.30 ***Control Signals:*** These are identical to those described in paragraph 2.11 through 2.23 with the exception that the IACK, EACK, and SRACK signals are not used.

2.31 ***Interrupts:*** The interrupts from the assigned DSCHs combined with one from the associated DMAC are transmitted directly to the CCIO bus. The DMAC transmits the channel (DSCH) interrupts as well as its interrupt via assigned data leads in response to reception of the IACK signal.

2.32 ***Channel Errors:*** The channel (DSCH) errors from the assigned DSCHs are individually terminated in the DMAC. The error signals are ORed with the DMAC error signal for a single error signal and sent to the CC. In response to an EACK signal,

the DMAC transmits its error state and the error states of the DSCHs to the CC over the CCIO bus data leads.

2.33 ***Communication with the MAS:*** The DMAC communicates with the MAS using the parallel MAS bus. The MAS bus consists of 74 leads that support six major functions: control, error, response, command, data, and address. Detailed information on the MAS bus and communications to the DMAC is provided in AT&T 254-301-200 *AT&T 3B20D Computer, Main Store, Description and Theory of Operation.*

2.34 ***DSCH to DDSBS Interface:*** The DSCH includes differential DC line driving and receiving circuitry to provide a serial data link for each DDSBS selector. All signaling is compatible with the RS422 EIA standard. Each DDSBS interfaces with the DSCH via two bidirectional data leads, a transmit clock, a receive clock, and a request lead. Also, data is transmitted in nonreturn to zero form and is simultaneously transmitted via both data links in conjunction with either transmit or receive clock pulses. Two channel options (clock frequency of 10 MHz or 5 MHz) are provided to facilitate the transmit clock to operate at 10 MHz for cable distances up to 100 feet and at 5 MHz for cable distances up to 250 feet.

3. Direct Memory Access Controller (DMAC)

Introduction

3.01 The CU can be equipped with up to two DMACs; each DMAC can be equipped with up to four DSCHs. Each DSCH can be interfaced to a maximum of 16 peripheral devices (PDs). A fully equipped DMA (2 DMACs, 4 DSCHs per DMAC) interfaces with a maximum of 128 PDs (2 DMACs X 4 DSCHs X 16 PDs). The DMAC provides a means of transferring blocks of data directly between the main store (MAS) and PDs without the CC performing each individual word transfer. Figure 2 illustrates a fully equipped DMA I/O with DMAC 0 and DMAC 1. (The DMAC 0 channel identifiers are 10 through 14, and DMAC 1 channel identifiers are 16 through 19).

A. Physical Description

3.02 The DMAC comprises four circuit packs (7-3/4 inches by 14 inches). These are:

- UN35 (2)
- UN36 (1)
- UN37 (1).

3.03 These circuit packs are located in the DMA I/O unit (Figure 2) in the upper portion of the CU frame. The DMA I/O unit is contained in a 2-foot 2-inch wide by 8-inch high enclosure and consists of the following subunits:

- DMAC—four circuit packs per DMAC
- DMAC I/O—four positions are provided for DSCHs for each DMAC
- Program Controlled I/O Channels—five positions (main channels 2 through 6) are provided for channel interfacing with the CCIO bus (SCH, DSCH, and ACHI).

B. Interfaces

3.04 The DMAC provides:

- An interface to the MAS via MAS bus system (74 leads)
- An interface to assigned DSCH(s) via DIO bus (66 leads)
- An interface to the CC via the CCIO bus (66 leads)
- Sequencer and tables to control data transfers.

See Figure 3 for an illustration of interfacing.

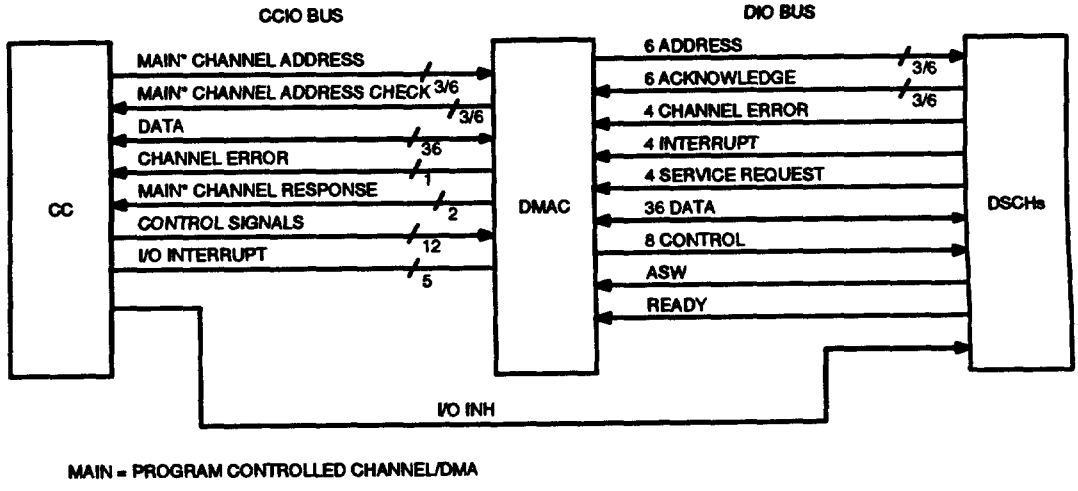


Figure 3. DMAC Interface

C. Functional Description

3.05 The DMAC (Figure 4) contains the following circuits:

- Data registers
- Address registers
- Interrupt register
- DMA I/O (DIO) bus control
- Error register
- Store bus control
- Channel error register
- Priority circuit and priority latch
- Request inhibit register
- 3-out-of-6 check circuit
- CCIO bus control
- Status buffer register
- Parity generator checker
- Incrementer
- DMAC read only memory (ROM) sequencer (512 X 40)
- DMAC random access memory (RAM) 256 X 36.

3.06 The communication among the CC and DMAC via CCIO bus is composed of the following:

- Main channel address (6 bits)
- Main channel address check (6 bits)
- Data (32 data bits + 4 parity bits, this is four 8-bit bytes with 1-parity bit, with odd parity for the 8-bit bytes and even parity for the entire 36 bits)
- Channel error (1 bit)
- Main channel response (1 bit)
- Control signals (12 bits)
- I/O interrupts (5 bits).

Communication between the CC, MAS, DSCH, and the DMAC is in parallel form.

3.07 Fifteen interrupt levels are assigned to the I/O channel. Each I/O channel has a predetermined interrupt and service request output. In response to an interrupt acknowledge (IACK) signal, each channel will report its interrupt state over an assigned lead of the data bus. Channel 0 is assigned lead 0, channel 1 is assigned lead 1, etc.

The DMAC 0 will respond over lead 10 and its channels (DSCHs) over leads 11 through 14. Interrupts are described in AT&T 254-301-010.

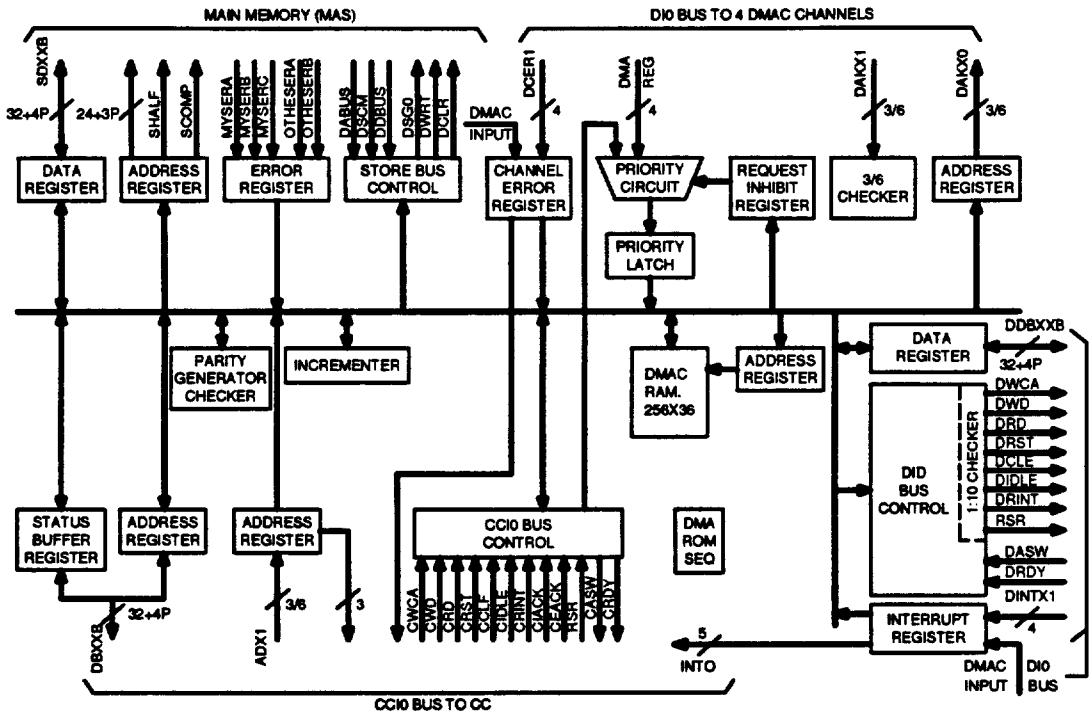


Figure 4. DMAC Functional Block Diagram

3.08 All signals transmitted between the CC via CCIO bus to the I/O channels are active low (0 volt) using TTL levels. These are described in Part 2 of this practice.

3.09 The MAS bus interfaces to the DMAC and is used to latch address data, control commands, and data format information in the DMAC. The MAS interface circuitry generates handshaking signals to the MAS, latches the data read from the MAS, and signals the DMAC sequencer on completion of the operation.

3.10 The CCIO bus provides the interface between the CC and DMAC over which the CC writes and reads the DMAC tables using the DMAC channel address data. Also, the I/O orders to the PDs (connected to the DSCH interfaced to the DMAC) are executed by the channels after receiving data from the CC via the DMAC and DSCH. Separate buffers are provided in the DMAC for data and status information gated to or received from the DSCHs.

3.11 Interfacing between the DMAC and the DSCH is provided by the DIO bus. This bus is similar to the CCIO bus lead number and designation. The DSCH service requests are wired individually into a priority resolution circuit in the DMAC. The request lead from the CC interface circuit is connected to the priority resolution circuit as the highest priority request.

3.12 Information about data transfers in progress is stored in the DMAC tables. The tables have separate entries for each I/O device (PD) connected to the DMAC. A count of the number of data transfers to be completed is maintained in the DMAC tables. The maximum count (and maximum block transfer) is 131072 bytes. The mode of transfer (read, write, and read and clear) and word or block mode are also stored in the DMAC tables (Figure 5).

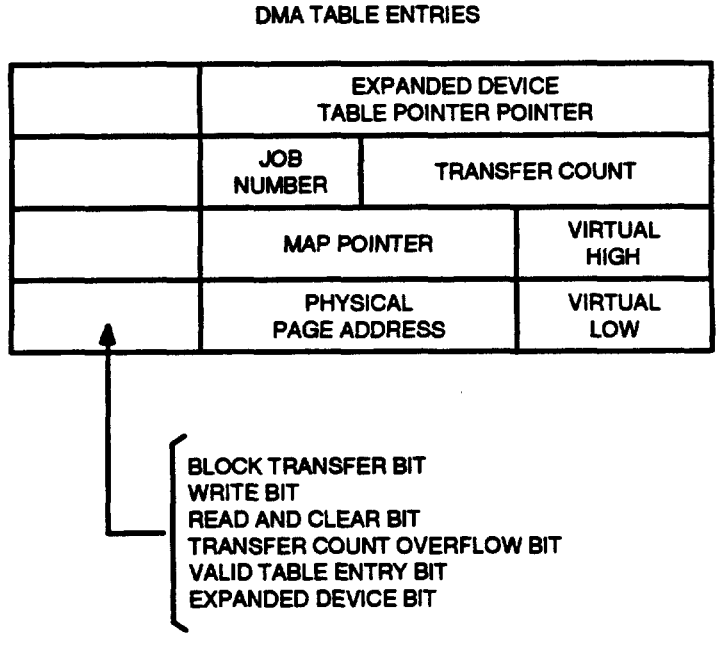


Figure 5. DMAC Table

3.13 An address of the next location to be read or written in the MAS is also needed for each PD. The maximum block transfer count (131072) involves 64 -2K byte pages of memory. Physical addresses of the 64 pages do not necessarily have to be in consecutive order; therefore, 64 separate physical addresses must be stored for each

PD. To keep the DMAC tables (Figure 5) at a reasonable size, the 64 page addresses are stored in the MAS. The CC transmits to the DMAC, as part of the initialization, the starting address of the block of 64 words containing the page addresses. This map pointer will point to a 64-word boundary, with its least significant 8 bits set to 0. During set up, the DMAC links together the map pointer and the six most significant bits of the virtual address, to format the address from which the DMAC reads the page address. This 13-bit page address is linked with the least significant 11 bits of the virtual address to provide the physical address of the MAS that is to be read or written (Figure 6) by the PD.

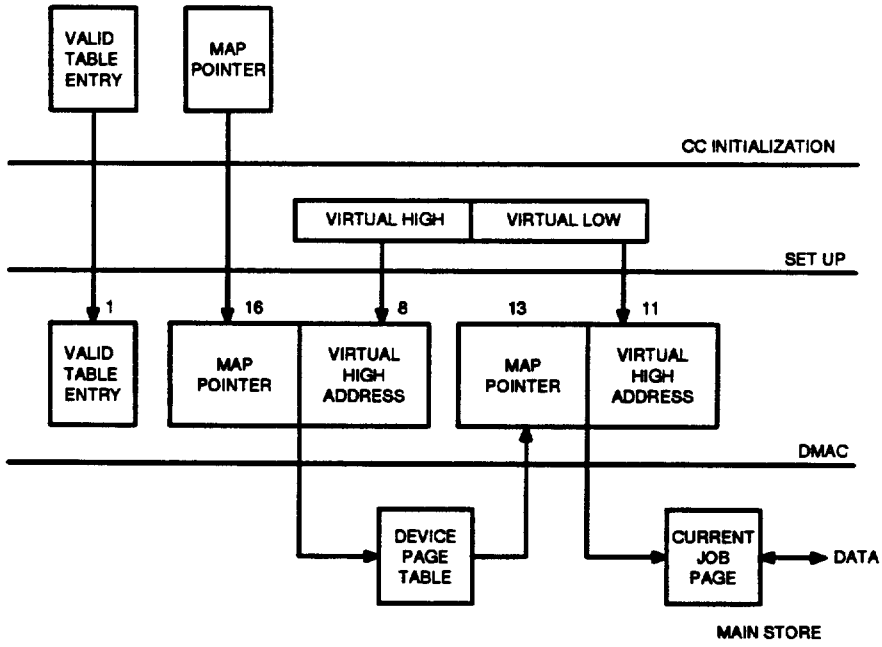


Figure 6. Unexpanded Device Address Translation

3.14 The DMAC may also be set up to accommodate PDs that are front-end processors, this is accomplished by expansion of the DMAC tables to provide 256 address translation maps per PD. Therefore each job on a PD is provided with access to its assigned block of memory in the MAS (to a maximum of 128K bytes), with the restriction that two jobs on a PD cannot be active at the same time. A new setup command must be issued whenever a different job by the PD requires access to the MAS. Also, to minimize the size of the DMAC tables, these maps are retained in the MAS. Memory only has to be allocated for as many PDs as are to be expanded. Each expanded PD has a dedicated block of 128 words (Figure 7). One bit in each PD entry of the DMAC table identifies whether the PD is expanded or not. If the PD device expansion bit is not set, the CC must provide the single 16-bit map pointer.

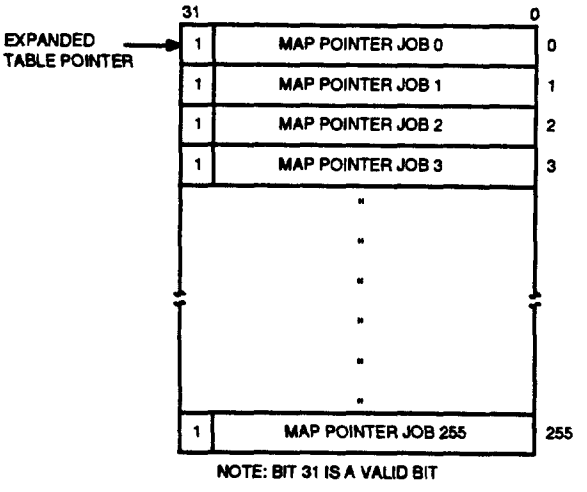


Figure 7. Expanded Device Table Layout

3.15 If expansion is provided for, an 8-bit job number is provided as part of the setup data (either by the PD or by the CC). The DMAC then fetches a pointer to the map pointer table; adds on the 8-bit job number, then indexes into the map pointer table to derive the 16-bit map pointer which is stored into the DMAC table. Address translations then proceed as described previously (Figure 8).

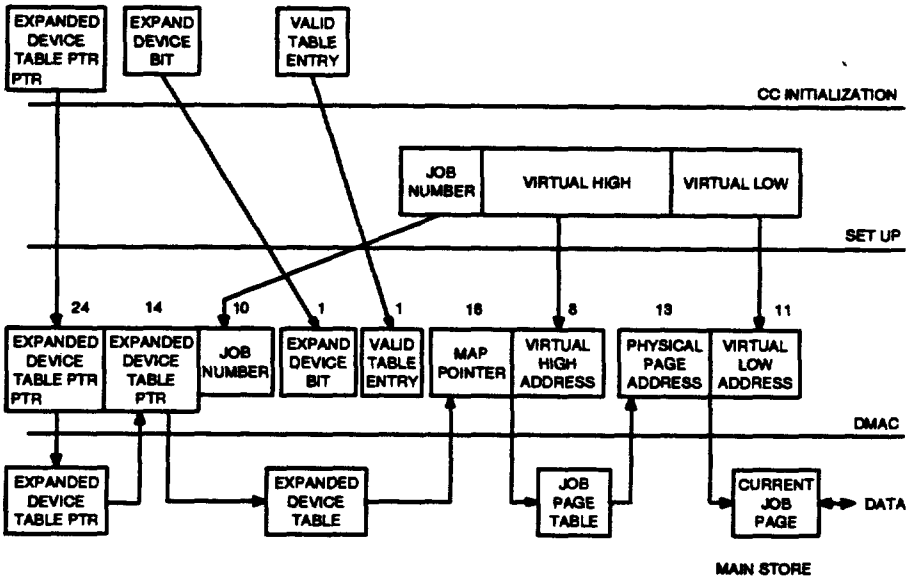


Figure 8. Expanded Device Address Translation

3.16 Many information transfers involve only one or two pages; the map pointer still points to a 64-word boundary. The map entry will indicate read and/or write access to the corresponding memory page. Page table entries, which are not equipped, will have both DMAC access bits reset. Expanded PDs will have the map pointers for unequipped operations pointing to a memory page address with the DMAC access placed in the off state. The DMAC will perform an access check on each new memory page fetch to verify that the DMAC access requested matches that specified for the page. The memory map table (Page Table) stored in the MAS is shared with the CC address translation buffer circuitry.

3.17 The DMAC table is implemented using 256-by-4-bit RAMs. Each DMAC associated PD is allocated four 32+4 parity bit words. Figure 9 illustrates the DMAC RAM layout.

3.18 ***DMAC Transfer Sequence:*** The DMAC must be properly set up with address and transfer count information before the start of a DMAC block transfer. The physical address translation map and a map pointer must be set up by the CC. After this operation, the PD can initiate a data transfer. The CC sets up the transfer to the DMAC via the CCIO bus. The PD sets up the transfer (through the DSCH and DIO bus) by requesting service via its setup lead and sending data over the channel data leads on request by the DMAC. The following data is transmitted to the DMAC for each setup request:

- Transfer mode (read, write, or read and clear)
- Job number (if an expanded PD)
- Starting address
- Optionally, total number of data transfers to be performed. (Required for expanded PDs.)

3.19 If the transfer count is not provided, the DMAC sets the count to maximum. A PD can set up a transfer by providing a starting memory address and mode, transmit a variable number of times, and set up the transfer again by providing another starting address, without regard to the transfer count in the DMAC. If the DMAC transfer count indicates all data has been transferred, the DMAC will transmit a command to the PD to indicate the end of the data transfer. The PD can then interrupt the CC (via the DSCH and DMAC), as an acknowledgment of job completion.

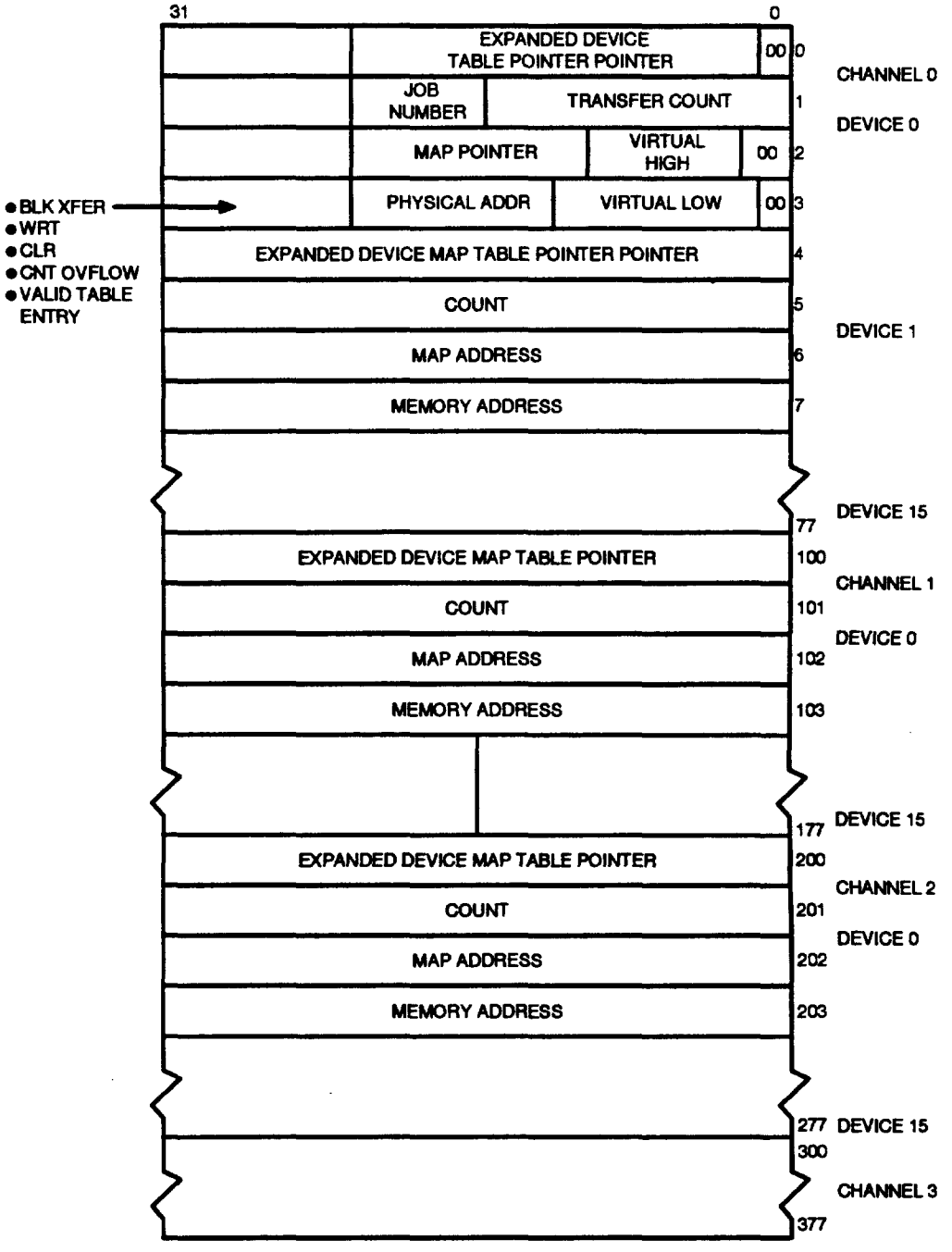


Figure 9. DMAC RAM Layout

D. Theory of Operation

3.20 The DMAC provides the interface between the CC (via CCIO bus) and up to four DSCHs (via DIO bus). Also, the DMAC provides the interface between PDs (via DSCH) and the MAS in operations requiring the transfer of blocks of data directly between the MAS and PD without direct use of the CC. The operations performed are:

- Write transfer
- Read transfer
- Transfer setup
- Programmed I/O operations via DMAC.

3.21 ***Write Transfer:*** The following operations occur when an I/O PD is reading data from the MAS during a DMA transfer: After a PD is ready to receive data, it activates an XFER request to the DSCH. The DSCH registers the request and activates its DMAR lead to the DMAC indicating the request. The DMAC resolves multiple requests from the DSCHs by identifying the DSCH priority (the highest priority receives first opportunity). The DMAC reads the service request register in the DSCH with transmission of an RSR instruction and identifies priorities of the requests from the PDs using the DSCH. For data transfer request, the address of the highest priority PD with a request active is used to index into the DMAC table to determine if the CC has initialized the DMAC table entry for that PD. Also, if the PD is in the read or write mode and it needs to transfer a single word or block of 16 words, the DMAC then fetches the next word from the MAS and transmits it to the DSCH for the PD. If the DMAC is set up for a block transfer, it will gate an additional 15 words from the MAS to the DSCH. After completion of the data transfer to the DSCH, the DMAC transmits a command to the DSCH to gate the data to the requesting PD and PD service request bit is set to logic 0. After the DSCH completes the transfer, it returns another request to the DMAC. This is used by the DMAC to verify that the transfer was completed without errors. The DMAC then places the DSCH in an idle state.

3.22 If a page boundary is encountered (crossed) during a transfer, the DMAC must use the map pointer to retrieve the next page address, check that correct DMAC access can be made to the page, and start the next read operation. The map pointer is then incremented. The address is incremented by four and stored in the table after every memory access operation. The count is incremented once for each transfer and stored in the DMAC tables. If the DMAC is in the block mode, the count should indicate the number of 16-word blocks to be transferred. When the count becomes 0, a count overflow bit is set in the DMAC table. On the next PD request, an end-of-transfer (EOT) command is gated to the PD via the DSCH.

3.23 ***Read Transfer:*** A read transfer from the PD to the MAS via DMAC is performed in the following sequence: When the PD has data ready to write into the MAS, it activates an XFER request to the DSCH. The DSCH registers the PD request and gates it to the DMAC via the activation of the DMAR lead. Then the DMAC resolves any multiple requests from the DSCHs by priority. The DMAC reads the service request register in the DSCH by activating the RSR lead on the DIO bus. The response from the DSCH is loaded into the DMAC priority circuit to identify which PD on the DSCH is next

to be serviced. Again, the DMAC tables are read to determine the mode of the PD (read/write, word/block) and whether the CC has allocated memory for the selected PD. For read transfers, the DMAC transmits to the DSCH the command to read the data from the PD and to reset the PDs service request bit. On completion of the I/O operation, the DSCH again requests DMAC service (DMAR lead activated). The word or block to be written is transferred from the DSCH to the MAS via the DMAC. The DMAC idles the DSCH after the last word has been read from the DSCH.

3.24 If a page boundary is crossed, the DMAC uses the map pointer to retrieve the next address, checks that the DMAC write access is available for the page, and then initiates the write operation. The map pointer is then incremented. The address is incremented by four and stored in the DMAC tables after each memory (MAS) access. The count is incremented once per transfer and stored in the DMAC tables. If the transfer was performed in 16-word blocks, the transfer count should identify the number of 16-word blocks to be transferred. When the count becomes 0, the DMAC count overflow bit is set in the DMAC table entry for the PD. And, if the PD requests service again without initiating a new setup, the DMAC will transmit an EOT command to the DSCH for the PD. After the word or block transfer is completed, the DMAC processes the next priority PD requesting action.

3.25 ***Transfer Setup:*** The DMAC tables must be initialized during CC initialization, this is accomplished by setting the valid table entry bit of each PD to an inactive state. The DSCH mask circuitry for the PD requests must also be initialized. Before DMAC memory transfers can be initiated, pointers in the DMAC tables to address translation maps in the MAS, must be set up by the CC and the valid table entry bit set. After initialization and setup, the PD can initiate a transfer.

3.26 The CC sets up the address translation for PD by gating data to the DMAC. This data word consists of:

- Valid table entry bit
- Nonexpanded PD flag bit
- 24-bit expanded table pointer pointer (for all expanded PDs), or
- 24-bit map pointer address (lower 8 bits are treated as 0s) if the PD is not expanded.

3.27 When the nonexpanded PD flag is 1, the 24-bit map pointer address points to a 64-word page boundary which is the start of a table of page addresses for the PD. If the nonexpanded PD flag bit is 0, the map pointer will be obtained from an area of the MAS pointed to be the expanded table pointer, indexed by the job number sent with the setup data. The expanded table pointer pointer points directly to the expanded table pointer. After the address translation data is provided, transfer operations may be issued.

3.28 The CC sets up the transfer via the CCIO bus. The PD sets up the transfer by transmitting a setup request to the DSCH (which is gated to the DMAC via DIO

bus DMAR lead), then sending data via its normal path (PD to DSCH to DMAC) on request. In each setup, the DMAC receives the following data:

- Mode of transfer (read, write, or read and clear)
- Single word or block transfer
- Starting address (virtual)
- Job number for expanded PD
- Optional (transfer count) 2s compliment of the total number of transfers to be completed (required from expanded PDs).

If the transfer count is not received, the DMAC will set it to the maximum count. Thereby, the transfer count in the DMAC will be ignored.

3.29 ***Programmed I/O Operations via DMAC:*** The CC performs I/O operations to a programmed I/O (PIO) channel via the DMAC, in the same manner as I/O operations to a programmed I/O channel connected directly to the CCIO bus. The main channel RDY signal is used by the DMAC for synchronization with the CC during CC PIO operations. The CC generates the data, address, and control information for one of the I/O channels connected to the DMAC. The DMAC detects that one of its channels is being addressed, buffers the incoming data, address, and control information from the CC, then acknowledges reception of the information. The DMAC sets a high priority request bit in the priority register, so the sequencer will initiate the CCIO job when the designated channel becomes idle. The DMAC elevates the requests from the channel with I/O operations to be performed to the highest priority to finish any DMAC operation in progress. The DMAC then transmits data and control information (sent by the CC) to the designated channel. The channel autonomously executes the CC instructions and requests the DMAC to transfer the channel status and data reply to the CC. The DMAC buffers the channel status and data reply in its registers, signals the CC by returning RDY when the CC sends an RD command, then sends the status and data reply to the CC upon receiving the read channel status and read channel data control signals from the CC. The DMAC does not return RDY to the CC reception of information from the channel on RD commands.

3.30 Three types of I/O operations the CC via DMAC will perform on the channel are:

(1) CC expects no data on the CLE and IDLE commands,

(2) CC expects data on the read channel interrupt state (RINT) and RSR commands,

(3) and the WCA sequence.

To initialize a DMAC connected DSCH, the CC can send a CLE or IDLE command. The DMAC detects that a command is present for one of its channels and sets the high priority request bit for that channel, but does return RDY to the CC. When the DMAC becomes idle, it will gate the command to its channel and gate (set) RDY to the CC. When the CC issues an RD command it will receive RDY only after the DMAC has completed the command. The procedure for RSR and RINT commands is the same as

for the CLE and IDLE commands except the data the CC receives is valid only on the RD signal that returns RDY. The WCA sequence is described in paragraph 3.28.

E. Maintenance

3.31 The DMAC has internal hardware circuits for maintenance purposes. These are:

- 3-out-of-6 check circuit on the DIO acknowledge address bus
- Parity
- 1-out-of-10 check circuit in the DIO bus control
- Registers for processing error indicators.

3.32 The primary maintenance on the DMAC is performed by the CC. The DMAC can be set into a maintenance state in which it will only execute maintenance routines. Using normal DMAC operations and looping techniques, the CC exercises the DMAC and verifies the reply data from the DMAC.

3.33 The DMAC and associated DSCH are dedicated to a CC and MAS. After a valid fault has been detected, the CC and dedicated I/O channels are switched off-line and the off-line CC is switched on-line. This duplication ensures that the addressed PD can be communicated with by a CC and that its services are not lost. However, if the PD is faulty, a switch of the CC is not made and the PD is essentially placed out-of-service (OOS), this is accompanied with an appropriate TTY printout.

4. Serial Channel

Introduction

4.01 The SCH provides a semiautonomous serial I/O interface between the CC and a maximum of 20 PDs. These PDs include teletypewriter controller (TTYC), tape data controller (TDC), RS232 interface (RSI), 3ESS™ switch network frames, etc. The SCH contains 20 subchannels with each of the 20 PDs assigned to a dedicated subchannel.

A. Physical Description

4.02 A SCH consists of one circuit pack, UN26. This circuit pack is 7-3/4 inches by 14 inches and is installed in the 3B20D computer CC or in the programmed I/O portion of the DMA I/O unit located in the upper part of the 3B20D computer CU frame (Figure 2). The number of SCHs provided is dependent upon the application, therefore more than one SCH may be supplied.

B. Interfaces

4.03 The SCH is an I/O channel and interfaces to the CC through the CCIO bus. The SCH is connected to the PDs via a transformer coupled AC bus. All PDs connected to the SCH are dual port devices. Each PD is connected to the SCH by a pair of coaxial cables, one cable for each direction of data transmission. In the NORMAL mode, these cables have a maximum distance between the SCH and PD of 60 feet. In the SLOW mode, these cables have a maximum distance between the SCH and PD of 120 feet. The outer conductors of the coaxial cables are grounded at the SCH side only, to prevent ground current loops between interconnecting equipment frames.

C. Functional Description

4.04 The SCH (Figure 10) consists of the following circuits:

- Shift register (21 bits or 39 bits)
- Control and address register
- Sequencer (driven by free running clock)
- Subchannel decoder and check circuit
- 20 subchannel drivers and receivers (in pairs)
- Handshake logic circuit (to CCIO bus)
- Single interrupt receiver.

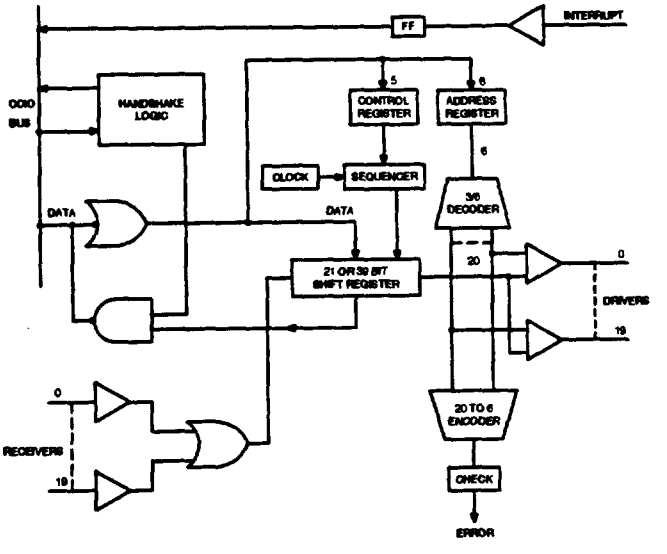


Figure 10. SCH Simple Block Diagram

Communications SCH to PD and Return

4.05 The SCH shift register is loaded with the message from the CC via the CCIO bus. The next order from the CC sets up one of the 20 subchannels selected with the write command address (WCA) signal. The trailing edge of the WCA signal starts the sequencer circuit. The data in the shift register is shifted out serially to the PD via the selected subchannel. When the data has been completely shifted out of the shift register, the sequencer then goes into the receive state. The PD must generate a reply for each message received from the SCH subchannel. This reply from the PD is shifted serially into the SCH shift register. After the PDs reply message has been shifted into the shift register the sequencer stops, locks the reply message, and sets an internal ready flag (IRDY). The CC monitors the IRDY signal by looping on the read data (RD) command. When the SCH responds with the ready flag (RDY) in answer to the RD command, the CC is signaled that a reply has been received (by the SCH from the PD) and data is available on the CCIO bus data leads. This sequence is repeated for every I/O operation via the SCH.

4.06 Figure 11 illustrates the functional block diagram of the SCH. The shift register is normally a 39-bit register (32 data bits, 4 parity bits, and 3-bit start code). Data and parity bits are parallel loaded into the shift register on the leading edge of the WD command. The start code bits are parallel loaded on the leading edge of the WCA command.

4.07 The control register is a 5-bit register that is loaded on the leading edge of the WCA command. These five bits are:

- Override I/O inhibit (1 bit)
- Maintenance states (2 bits)
- The 32/16 data bit mode (39/21) (1 bit)
- SLOW/FAST mode (1 bit).

4.08 The subchannel address register is a 6-bit register, which is also loaded on the leading edge of the WCA command. These 6 bits are coded to select the subchannel designated by the CC.

4.09 The 3-out-of-6 decoder decodes the subchannel address that is to receive the data. For error checking, the 20 outputs of the decoder are encoded into six leads and then checked for a valid 3-out-of-6 code. The check circuit is strobed during the receive state. The sequence is driven by a 4-phase free running clock. This clock generates a 3-phase pulse train in the SLOW mode, and a 4-phase pulse train in the FAST mode.

4.10 The sequencer has four control states; ready, idle, transmit, and receive. Ready indicates that a message has been received from the PD. Idle indicates, the sequencer is at rest. Transmit indicates, the SCH is prepared to transmit the message. Receive indicates the SCH is prepared to receive a message. The sequencer also synchronizes the serial data output data stream with two clock phases to drive the serial data encoder.

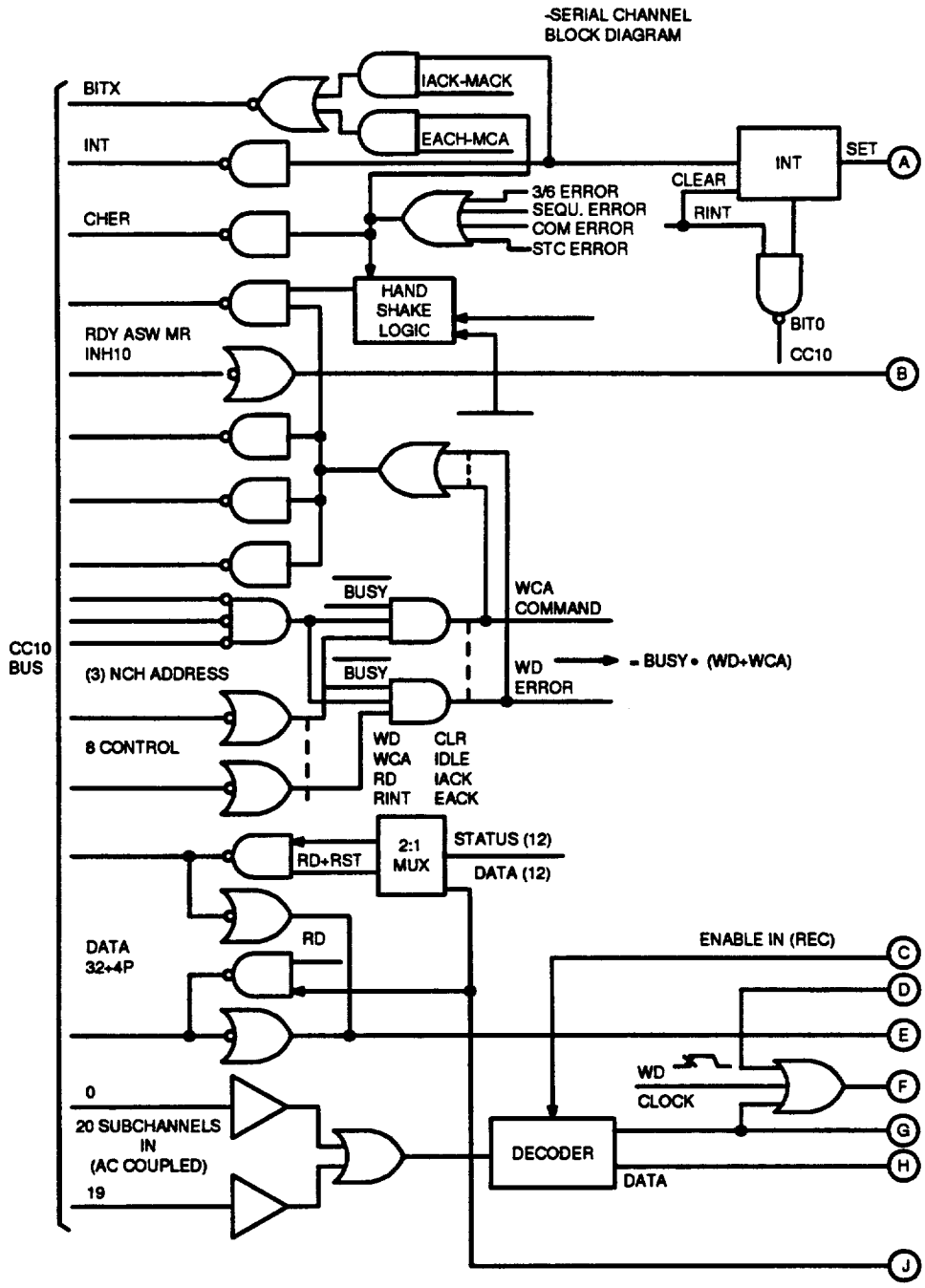


Figure 11. SCH Functional Block Diagram (Sheet 1 of 2)

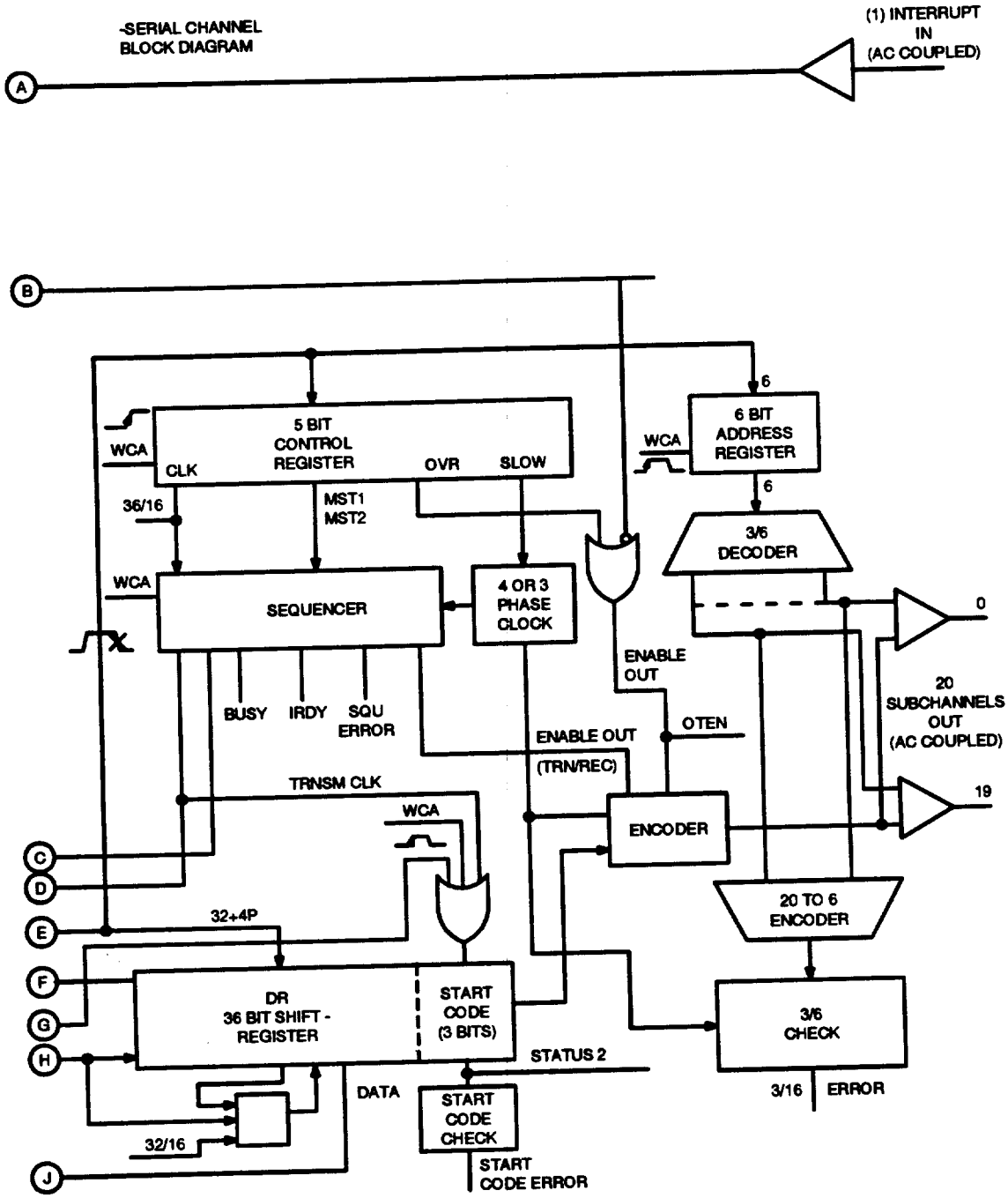


Figure 11. SCH Functional Block Diagram (Sheet 2 of 2)

4.11 The data shifted out serially by the shift register is converted to bipolar pulses by the data encoder and the transformer of the selected subchannel output for use by the PD. The bipolar pulses received from the replying subchannel (PD) input ports are decoded to separate the clock pulse and data to be shifted into the shift register. The decoded clock pulse gates the shift register into the receive state.

4.12 All commands from the CC are ANDed with the three main channel address signals. Command signals WD and WCA are inhibited when the SCH is in the busy state. Responses all seems well (ASW), maintenance response (MR), and ready (RDY) are acted on by the handshaking logic circuit. The 12 status bits from the SCH are multiplexed and gated onto the CCIO bus data leads during the read status (RST) command sequence.

Control Signals

4.13 The CC controls the operation of the SCH by the use of 10 control signals. A total of 12 signals is available from the CC; however, two are not used by the SCH. These control signals are active low (0 volt), and operations are not initiated by control signals unless the appropriate SCH main channel address is present.

4.14 ***Idle the Channel (Idle):*** The idle command initializes the SCH to a known state, and any control state is reset. If a transmission to a PD is in progress, the transmission is terminated. Also, the data channel register is cleared. The SCH responds to the CC idle command with the following signals: address acknowledge, all seems well, and ready.

4.15 ***Write Data (WD):*** This command is used to load data into the SCH channel data register. The CCIO bus data lead state is clocked into the data register on the leading edge of the WD control signal. Normally, the SCH responds to the CC with signals address acknowledge, all seems well, and ready. However, if the WD command is set when the SCH is in the busy state, the channel error (CER) bit is set, the SCH ignores the WD command, and the normal responses are not sent to the CC by the SCH.

4.16 ***Write Command Address (WCA):*** This command is used to load the SCH control and subchannel address register. The data on the CCIO bus data leads are gated into the registers on the leading edge of the WCA command signal. The trailing edge of the WCA signal is used to set the SCH sequencer into the transmit state. Normally, the SCH responds with address acknowledge, all seems well, and ready response signals to the CC. However, if WCA is set when the SCH is in the busy state, the channel error bit is set and the SCH ignores the WCA signal command. The normal responses, address acknowledge, ready, and all seem well, are inhibited.

4.17 ***Read Data (RD):*** On reception of the RD signal, the SCH gates the state of the data register onto the CCIO bus. The SCH always returns an address acknowledge signal. A return of ready, all seems well, and maintenance response signals depend on the state of the sequencer internal ready (IRDY) bit. If a reply is present in the data register, the ready (RDY) is activated. Also, all seems well and maintenance response signals depend on the state of the returned start code. The all

seems well (ASW) signal is active when the reply has a 011 return start code. The maintenance response (MR) signal is active for a 101 return start code. If the ready (RDY) signal is not set, the data on the CCIO bus data leads, ASW, and MR are not valid.

4.18 ***Read Status (RST):*** When the RST signal is received by the SCH, the status of the SCH is returned to the CC on the CCIO bus. The SCH returns the address acknowledge, RDY, and ASW signals to the CC on receiving the RST signal.

4.19 ***Read Interrupt (RINT):*** On reception of the RINT signal from the CC, the SCH gates the state of the single interrupt bit onto bit 0 of the CCIO bus data leads. The SCH interrupt flip-flop is reset on the trailing edge of the RINT signal. Address acknowledge, RDY, and ASW signals are also gated to the CC via the CCIO bus.

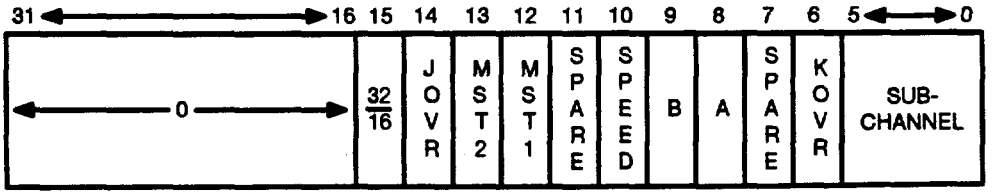
4.20 ***Interrupt Acknowledge (IACK):*** When the IACK signal is received by the SCH, it gates the state of the interrupt flip-flop onto an assigned bit of the CCIO bus data leads. The IACK signal does not clear the interrupt flip-flop. Address acknowledge, ready, and all seems well response signals are also gated to the CC when IACK is received by the SCH.

4.21 ***Error Acknowledge (EACK):*** The EACK signal is used by the SCH to gate the state of its error flip-flop onto the assigned bit of the CCIO bus. This signal (EACK) does not clear the error flip-flop. Address acknowledge, ready, and all seems well response signals are also gated to the CC when the EACK signal is received by the SCH.

4.22 ***Clear Error (CLR):*** This signal (CLR) is used by the SCH to reset its error register and also performs the same functions as the idle signal (paragraph 4.14). The SCH responds to the CLR signal with transmission of address acknowledge, all seems well, and ready response signals to the CC.

4.23 ***I/O Inhibit (INH):*** This is a DC signal and is held active by the on-line CC to disable I/O operations in the off-line CC. The INH signal can be overridden by setting an assigned bit in the SCH control register. The INH signal inhibits the output signals of all 20 subchannels. The SCH sequencer is not affected by the INH signal.

4.24 Figure 12 illustrates the format of the command word. The word configuration (on the CCIO bus), when the WCA lead is activated, identifies the operations to be performed by the SCH. The trailing edge of the WCA signal always starts the SCH sequencer in the transmit mode and sets the busy lead. The only exit out of the busy state is by use of the idle signal command.



BIT	FUNCTION
0-5	SUBCHANNEL ADDRESS
6	K INPUT I/O INHIBIT OVERRIDE
8	START CODE BIT A
9	START CODE BIT B
10	FAST/SLOW
12	MAINTENANCE STATE
13	MAINTENANCE STATE
14	J INPUT I/O INHIBIT OVERRIDE
15	32/16 BIT OPERATION

Figure 12. Command Word Format

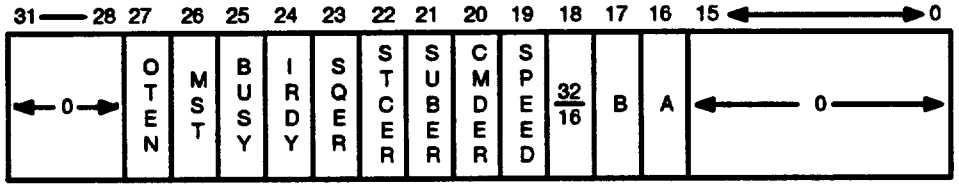
4.25 Bits 0 through 5 define the selected subchannel that will receive the data. There are 20 valid 3-out-of-6 codes. Subchannel assignments are in ascending order 0 to 19. If an invalid code is sent by the CC, the SCH will detect the code error and set the channel error flag. Bit 6 is the K input to the I/O inhibit override J-K flip-flop. When bit 6 is a 1 and bit 14 is a 0, the I/O inhibit override is reset. However, if both bits 6 and 14 are 1, the override flip-flop toggles from its present state. This bit configuration should not be used by the CC. To set the override flip-flop, bit 6 must be 0, and bit 14 must be a 1. Bits 8 and 9 are used to set the start code bit format. If bit 8 is a 1, the 011 start code is added to the outpulsed data. If bit 9 is a 1, the 101 start code is added to the outpulsed data. If both bits 8 and 9 are 0s, the start code is set to 001; and if both bits are 1s, the start code is set to 111. Start codes of 001 and 111 are invalid, if these occur in the start code register, a check circuit in the SCH generates a channel error signal.

4.26 When bit 10 is a Logic 1, the SCH is set into the SLOW mode. The message to the PD will be transmitted at a rate of 225 nanoseconds per bit. The SLOW mode facilitates the cable length between the SCH and PD to be extended to 120 feet from the 60-foot limit in the FAST mode. If either bit 12 or 13 is a 1, the SCH is placed into one of two maintenance states. These are described in paragraph 4.60. Bit 14 is the J-input to the I/O inhibit override J-K flip-flop. This flip-flop is used to inhibit the function of the CC I/O inhibit signal. When the I/O inhibit signal is set and not inhibited by the override flip-flop, the SCH will shift the data out without transmitting the data to the PD and then stay in the receive state until idled by the CC. The 32-bit mode is selected when bit 15 is a 1, while the 16-bit mode is selected when bit 15 is a 0. When

the 16-bit mode is used, the most significant bits (the upper half of the 32-bit word) of the data register retain the values in which it was set during the WD sequence.

Status

4.27 Figure 13 illustrates the status word format returned to the CC during the read status (RST) command. Bits 0 through 15 and bits 28 through 31 are always 0. Parity is not generated for the status word. However, the 4 parity bits are always 0. Bits 16 and 17 are the two start code bits. During the RST command a signal is transmitted to the CC identifying the state of the SCH start code register. If serial shift operations are in progress, an invalid start code may be indicated. Therefore, the start code bits are valid only when the SCH shift register has stopped shifting. Bit 18 indicates the use of the 32-bit or 16-bit mode of operation. When bit 18 is a 1, the 32-bit mode is used by the SCH; if bit 18 is a 0, the 16-bit mode is used. The shift register is a 39-bit register in the 32-bit mode (32 data bits, 4 parity bits, and 3-bit start code) and a 21-bit register in the 16-bit mode (16 data bits, 2 parity bits, and 3-bit start code). Bit 19 indicates the speed at which data is transmitted to the PD. When bit 19 is a 1, the SLOW mode is used, when a 0, the FAST (normal) mode is used.



BIT	FUNCTION
16	START CODE BIT A
17	START CODE BIT B
18	32/16 BIT OPERATION
19	FAST/SLOW OPERATION
20	COMMAND ERROR
21	SUBCHANNEL ERROR
22	START CODE ERROR
23	SEQUENCER ERROR
24	INTERNAL READY
25	BUSY
26	MAINTENANCE STATE
27	OUTPUT ENABLED

Figure 13. SCH Status Bit Assignments

4.28 Bit 20 is the command error bit. It is set when the CC attempts to execute the WD or WCA commands when the SCH is in the busy state. When the command error flip-flop is set, the channel error signal is also activated. Bit 21 is the subchannel

error bit. The subchannel error flip-flop is set when the SCH has received an invalid 3-out-of-6 address code from the CC or there is a hardware fault in the subchannel decoder circuit. When the subchannel error flip-flop is set, the channel error signal is activated. Bit 22 is the start code error bit. The start code error flip-flop is set when the CC has transmitted a 001 or 111 start code to the SCH start code register during a WCA signal command. When the start code error flip-flop is set, the channel error signal is made active. Bit 23 is the SCH sequencer error bit. The sequencer error flip-flop is set when the SCH sequencer is in simultaneous transmit and receive states. This is caused by an SCH hardware fault or a maintenance state bit is set. Bit 24 is the internal ready bit. When bit 24 is a 1, the SCH has received a full message from one of its 20 input ports. If bit 24 is valid, the SCH returns the ready signal during any subsequent read data (RD) command. Bit 25 is the busy bit. When bit 25 is set, the SCH is in the process of communicating with a PD. Busy remains set from the trailing edge of the WCA signal until the SCH is idled with the idle or clear error command signal.

4.29 Bit 26 when set (1) indicates that the SCH is in either one of its two maintenance states. The outputs of the two maintenance flip-flops are ORed into one bit to derive bit 26. Bit 27 when set (1) indicates that the serial output ports are enabled. If the inhibit I/O is set at the CC, bit 27 is a 0 unless the I/O inhibit override in the SCH is set.

3B20D Computer CCIO Bus Sequence

4.30 The sequence to perform an I/O operation between the CC and SCH is as follows: First, the main channel address must be set up, the SCH will not accept a command unless its address is present on the main channel address leads (CCIO bus). The 32-bit data word for the PD must be gated onto the CCIO bus data leads. Second, the write data (WD) control lead is activated. The SCH clocks the state of the CCIO bus data leads into its data register on the leading edge of the WD signal. Third, the control address information is gated onto the CCIO bus data leads. The bit format signifies to the SCH which one of the 20 subchannels is to be used, which start code is to be transmitted, the mode of operation to be used (16 or 32 bit), and rate to be used (FAST or SLOW). The inhibit I/O override function is also controlled with this WCA word. The WCA word can also force the SCH into the maintenance state if the correct bits are set (used for diagnostics). While this information is on the CCIO bus data leads, the WCA lead is pulsed.

4.31 The address and control registers are clocked on the leading edge of the WCA signal. The trailing edge of WCA starts the sequencer, and the data with the appropriate start code bits are sent to the selected subchannel. After the data is gated out, the sequencer shifts into the receive mode. An all 0s bit stream follows the data and is used by the subchannel PD to transmit a reply to the SCH. The time required to get a reply from the PD is 12 microseconds plus PD cycle time in the 32-bit mode, and more than 6.6 microseconds in the 16-bit mode. The CC detects that a reply has been received from the PD by the SCH by looping on the RD command. An indication of a reply is given via the RDY lead. If RDY is set, then a reply has been received by the SCH. An indication of which start code has been received is given by the ASW and MR leads. If the start code is a 101, then MR is activated. The states on the ASW and MR

are valid only when RDY is active. Also, the data on the CCIO bus data leads is valid only when RDY is active. After the CC has identified a reply and has clocked the reply off of the CCIO bus, the SCH is idled with the idle command. Idle clears all control states in the SCH and facilitates the next I/O operation to be initiated.

4.32 The SCH autonomously transfers data to a PD. While the SCH is busy, the main channel address may be removed (for as long as setup and hold times are satisfied on the control leads). This lets the CC process another main channel while the SCH is busy. The reading of information from the SCH does not interfere with the data transfers to and from the PD. Channel error and interrupt outputs are asynchronous and are not gated to the CC with the main channel address.

4.33 ***32/16 Bit Mode of Operation:*** When the 16-bit mode is used, the SCH does not shift the upper half of the word to the selected PD. The sequencer goes into the receive state after 21 bits have been shifted out to the PD. The reply from the PD is shifted into the lower half word. The receive state is terminated when 21 bits have been gated into the data register. When the CC performs an RD command, the entire 32-bit word with 4 parity bits is gated onto the CCIO bus data leads. The CC must therefore have loaded the entire 32 bits with correct parity even though only the lower half of the word is shifted to the PD. In the 32-bit mode, the entire 32-bit word is shifted out to the PD. The sequencer goes into the receive state after 39 bits (32 data bits, 4 parity bits, and 3-bit start code) have been shifted out to the PD. The PD reply is shifted through the 39-bit register. The receive state is terminated when the first 1 (1st bit of the start code) is shifted into the least significant bit of the 39-bit register.

4.34 ***NORMAL/SLOW Mode of Operation:*** The SCH can be operated in the SLOW mode to extend the distance over which usable signals can be transmitted to the PD. In the SLOW mode, the bipolar signal lobes are doubled to a time interval of 75 nanoseconds from the normal time interval of 37.5 nanoseconds. The dead time of a given bit is kept at 75 nanoseconds. In the SLOW mode the SCH sequencer is driven from a 3-phase clock instead of the 4-phase clock for the NORMAL mode. This results in a bit time of 225 nanoseconds instead of the normal 150 nanoseconds. The PDs do not contain any options for operation in the SLOW mode because the PDs obtain timing information from the bit stream generated by the SCH.

4.35 ***SCH Time-Out:*** The SCH is not provided with a time-out function. However, if a transfer is attempted to an unequipped subchannel or the PD connected to the selected subchannel does not reply, the SCH remains in the receive state until the CC times out and idles the SCH.

4.36 ***Error Checks:*** The SCH tests for four error conditions. All are the result of hardware failures. When one of these occurs, the channel error (CER) bit is made active, to generate an error interrupt to the CC. An error indication is given if an invalid 3-out-of-6 code is loaded into the subchannel address register (this should never occur because of a program error). A hardware fault in the subchannel decoder also would create this error. A bus lead stuck in the wrong state also would create the subchannel error. A second error situation is checked for on the CCIO bus control leads when the CC attempts to activate the WD and WCA control leads and the SCH is busy. This sequence caused by the CC is detected in the SCH. When WD and WCA are

activated while the SCH is busy, the SCH sets the CER bit and ignores the CC commands. Signals RDY, ASW, and ACK are not gated to the CC during this error situation. A third error detector monitors the SCH sequencer. If the sequencer, because of a hardware fault, is in simultaneous transmit and receive states, a channel error indication is given. A fourth error indication is given when an invalid start code (001 or 111) is loaded into the start code register.

4.37 ***Message Format:*** Figure 14 illustrates the message format of the communications between the SCH and PDs. In the 16-bit mode, the message contains 21 bits (16 data bits, 2 parity bits, and 3-bit start code) and in the 32-bit mode, the message contains 39 bits (32 data bits, 4 parity bits, and 3-bit start code). The first bit of the 3-bit start code is always a 1. This 1 is used for message registration in the SCH receiver circuits. Two start codes are valid: a 011 identifies a data word or a normal reply, a 101 start code identifies a control word or an error reply message. Each 8 bits of data is followed by a parity bit. Parity is odd over each 8-bit data byte and even over the entire 32-data bits (4 bytes). When the message is transmitted to the PD by the SCH, it is followed by a 0 bit stream from the SCH. The PDs use this 0 bit stream to drive its sequencer logic and use timing signals derived from the bit stream to transmit a reply to the SCH. When the SCH has received the reply, the 0 bit stream is terminated.

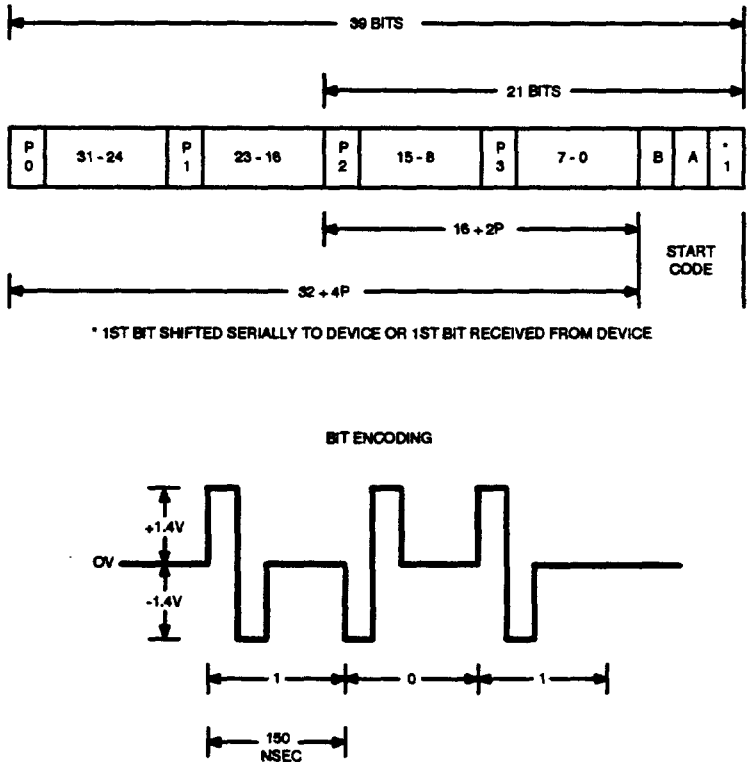


Figure 14. SCH to PD Word Format

A. Theory of Operation

4.38 ***Command Interface:*** The command interface provides the interface between the control leads of the CCIO bus and the SCH. All command interface signals are buffered with noninverting Schmitt trigger circuits. The command signals are ANDed with the three main channel address signals ADAIO, ADBIO, and ADCIO. The SCH ignores all commands unless the main channel address is valid (true). The inhibit I/O signal INHIO is not gated with the main channel address. The busy signal BUS1A is generated by the sequencer. When BUS1A is active and the CC gates signal WCAIO or WDIO, an error latch in CDECODE is set and and CMDER1 is activated. The ACK1 activates the address acknowledge signals AKAO0, AKBO0, and AKCO0. The ACK1 also clocks the handshaking flip-flop HRDY. The HRDY signal enables gating of RDY signal to the CC in response to a command. The RDY signal is always set, except during the RD command. During RD, the HRDY flip-flop is set only when IRDYO is a logic 1. During RD, the ASWO0 and MRO0 signals depend on the states of the start code register. The MRO0 is activated when the start code register contains a 101 start code (RSCB21 is set). The ASWO0 is activated when the start code register contains a 011 start code (RSCB11 is set). The ASWO0 is never activated when the channel error signal CHER1 is activated. Signal GBOX0 when active gates the CCIO bus transceivers for bit 0 and bit x (x is system defined). Signal 0001 is the information for data bit 0. Signal DR001 is gated to the CC during the read data (RD) command. Signal INT1 is gated to the CC during the read interrupt command.

4.39 ***I/O Inhibit:*** The I/O inhibit signal INHIO is buffered by the CBD circuit and used to generate a 1-shot pulse to clear the I/O inhibit override flip-flop INHOR. This 1-shot clears INHOR on the high-to-low transition on the INHIO lead. Signal WCPBO clocks INHOVR on a high-to-low transition. When the J-input is high and the K-input is low, INHOVR flip-flop is set. Also when the J-input is low and the K-input is high, INHOVR is reset. Therefore, when signal INHI1 is active and flip-flop INHOVR is reset, signal INHOTO is active and the serial output of the SCH is inhibited. When flip-flop INHOVR is set, signal INHOT0 is inactive, regardless of the state of signal INHI1.

4.40 ***Command Buffering:*** Signals WCPO and WDPO are double buffered to provide additional drive capabilities. Signal INITO is used to initialize the SCH; it is derived (ORed) from the idle command, clear error command, and bus power clear signal. Signal GDSTO gates the CCIO bus transceivers that gate status signals onto the CCIO during a read status command to ON.

4.41 ***Control and Address Register:*** Control and subchannel registers are clocked on the low-to-high transition of the WCP1 signal. Signal WCP1 is derived from the write command address signal. Subchannel address register (CRA) contains the address of subchannel that is to receive the message data. Control register (CR) bit 15 determines the 16- or 32-bit mode of operation, bit 10 determines the normal or slow transmission rate. Bit 12 forces the SCH into maintenance state MST1 and bit 13 forces the SCH into maintenance state MST2. The data register is cleared via the CLRDRO signal.

4.42 ***Clock Circuit:*** The clock circuit drives the sequencer and provides two clock phases for the serial data encoder. The clock circuit is driven from a 26.67 MHz free running clock oscillator, which is coupled into the multiplexor (TMUX). (For testing, an external clock can be applied to the TSTCK lead with the ETSTO signal held low.) Flip-flop CLK1 divides the clock signal by two for the SLOW mode. The normal or slow clock is coupled into the SPMUX multiplexor. The output of SPMUX is at the fast (normal) rate when signal FST1 is active and SLW1 is inactive. When SLW1 is active and FST1 is inactive, the output of SPMUX is the divided-by-two clock. Flip-flops CKA, CKB, CKC, and CKD provide a self-correcting ring counter that provides for three clock phases: CKA1, PHA1, and PHBUB1. When signal FST1 is active, the ring counter provides the three clock phases with a 150-nanosecond period. When signal FST1 is inactive, the ring counter provides three evenly spaced clock phases with a 225-nanosecond period.

4.43 ***Sequencer:*** The sequencer consists of a presettable 6-bit counter, seven flip-flops, and decoding gates. The sequencer has two modes of operation (16 bit and 32 bit). The mode is determined by the states of signals 39BT1 and 39BT0. The 6-bit counter is preset to the values determined by the 39BT1 and 39BT0 signals. The counters are normally held in the parallel load mode. In the 16-bit mode the counters are preset to the 1110 1011 state, and in the 32-bit mode preset to 1101 1001 state. The two counters are connected in a ripple mode. That is, the carry of counter CNTA is connected to the count-up input of counter CNTB. The carry signal of counter CNTB idles the TA flip-flop. In the 16-bit mode a carry signal is outputted from counter CNTB on the 21st pulse gated out of gate circuit CTCKO. In the 32-bit mode a carry signal is outputted from counter CNTB on the 39th pulse gated out of gate CTCKO.

4.44 The sequencer is started by the trailing edge of a ground level signal on the WCPBO lead. Signal WCPBO is the buffered WCA command signal, and is used to clear flip-flop TA. When TA is cleared, it sets the busy flip-flop (BUSY0 and BUSY1). Signal BUSY1B removes the clear function from the clock circuit, and clock phase PHBO sets flip-flop TB. When TB becomes set and flip-flop TC is cleared, a strobe signal is generated on the CSET1 lead. This strobe signal is used to strobe the start code error circuit. Flip-flop TC, when set, sends the counter into the count mode, and clock pulses are gated to the counter via gate CTCKO. Shift pulses are gated to the data register via gate circuit TSHPO, and the serial data encoder is enabled via gate EOT1. When the counter has counted 21 or 39 pulses of clock phase CKA1, 20 or 38 transmit shift pulses have been generated at the output of gate TSHPO, and a carry signal from counter CNTB presets flip-flop TA. When the flip-flop TA is idled, two more transmit shift pulses are generated because two more clock cycles are required to clear the TC flip-flop. When flip-flop TC is cleared, flip-flop RA is cleared. When flip-flop RA is cleared, the sequencer starts the receive state. On the next two clock cycles, flip-flops RB and DL become set. Signal EOT1 is still active to facilitate the transmission of the all 0 bit stream while the sequencer is in the receive state. Flip-flops RA and RB outputs enable the SCH receivers in gate EIN1. When a full message has been received (loaded) in the data register, signal SCBOA0 goes low. This sets the RA flip-flop, on the next sequencer cycle flip-flop RB resets and signal EOT1 becomes inactive. This terminates the all 0 bit stream in synchronization with the two clock phases provided to the serial data encoder and full signal lobes are sent on the last 0 bit being transmitted to the PD. Flip-flop DL generates a 1-cycle delay before the flip-flop IRDY

can set so that data can stablize in the parallel gating paths of the shift register. The busy and IRDY flip-flops remain set until the SCH is idled with the IDLE or CLEAR ERROR commands from the CC.

4.45 ***Bus Power Relay:*** The bus power relay K1 is closed by a low-level signal on the BPENIO lead. Diode CR3 is a 3-volt shunt regulator. The output of the 3VDR regulator is the source supply to the serial output drivers. When the relay contacts are open, resistor R48 provides for a low-level signal on the BPCLR0 lead. The low-level signal is used to reset the SCH sequencer and control logic circuitry.

4.46 ***Interrupt Circuit:*** Transformer T41 receives the interrupt signal (unipolar). The interrupt signal sets the flip-flop INT, gate EINTO inhibits the interrupt signal when the signal INHOTO is made active. Flip-flop INT is cleared on the trailing edge of the read interrupt (RINTMC1) signal. The INTO0 gate couples the interrupt signal to the CC via CCIO bus.

4.47 ***Error Register:*** The error register is cleared by the BPCLRO and CLRMCO signal (BPCLRO is the bus power clear signal and CLRMCO is the clear error signal from the CC). The subchannel error signal SCERO sets the error latch 3, and the start code error signal SCDERO sets the error latch 2. Signal SCDERO is active when the CC has loaded a 111 or 001 start code into the start code register. The sequence error signal SQERO sets the error latch 1, signal SQERO is active when the sequencer is simultaneously in the transmit and receive states. Signal CMDER1 is active when the CC has pulsed the write data or write command address leads while the SCH is in the busy state. Signal CMDER 1 is latched into the command decoder (CDECODE). Outputs of the error registers are ORed to generate the channel error signal CHER1, and signal CERO0 is used to gate the channel error signal (CHER1) to the CC.

4.48 ***Data Register:*** The data register consists of eight 4-bit shift registers connected in series for the serial shift operations. The register can be parallel loaded or unloaded from or to the CCIO bus. The register normally is in the parallel load mode (signal BUSIA is low). To set the register into the serial shift mode (for shifting to/from PD) signal BUS1A is set high by the sequencer. Data for the low numberered bits is obtained from the least significant bit of the high bits in the 32-bit mode or directly from the clock and data recovery circuit in the 16-bit mode. Data into the high numbered bits are obtained directly from the data and clock recovery circuit.

4.49 ***Start Code Register:*** The 3-bit start code register is composed of flip-flops SCBOA and SCBOB. Flip-flop SCBOB is clocked on the leading edge of the SHP1 signal; flip-flop SCBOA is clocked on the trailing edge of the SHP1 signal. During transmit operations, flip-flop SCBOA stablizes the data over the trailing edge of the second clock phase. During the receive mode, signal SCBOA0 inhibits any more shift pulses from being received by the data and clock recovery circuit when the first 1 bit is clocked into the SCBOA flip-flop. Signal SCDERO is the output of the 2-input exclusive OR circuit. When strobed by signal CSET1, signal SCDERO is active whenever the two start code bits RSCB11 and RSCB21 are both 0s or 1s.

4.50 ***Serial Data Encoder:*** The serial data encoder outputs are inhibited when the INHOT0 signal is active. Signal EOT1 enables the encoder in synchronism with the two clock phases PHA1 and PHB1B. The encoder uses the complementary outputs of flip-flop SCBOA to generate the encoded signal gated on the NLO1 and PLO1 leads (two each). Test points TPO11 and TPO21 are provided for testing. In the normal mode output pulses are 37.5 nanoseconds wide and 75 nanoseconds wide in the slow mode. Signal BLKOT0 inhibits 1 signals from entering the encoder when a 1 is shifted into flip-flop SCBOA at the end of the receive state.

4.51 ***Subchannel Decoder/Checker:*** This circuit is composed of a 3-out-of-6 decoder, a 20-to-6 encoder and a check circuit. The check circuit is strobed by the RB1 signal. The decoder has 20 outputs, only one of which is active at any one time (this selects the PD). Signal SCERO is the subchannel error signal; when strobed by signal RB1 signal, SCERO is active when an invalid 3-out-of-6 code is present at the decoder input or when a hardware fault exists in the decoder.

4.52 ***Channel Drivers:*** Twenty channel drivers are provided (one per PD). For each output driver a 1 to 1 transformer is used. These circuits transmit bipolar pulses to the PD.

4.53 ***Channel Receivers:*** Twenty channel receivers are provided (one per PD). For each input receiver a 1 to 1 transformer is used. These circuits receive bipolar pulses from the PD.

4.54 ***Data/Clock Recovery:*** This circuit recovers data and clock from the bit stream. This is accomplished using flip-flop circuitry.

4.55 ***Shift Pulse Distribution:*** The following is a list of shift pulse distribution:

Shift Pulse	Operation/Circuit
TSHP0	Transmit mode
SHP1	Data register
SHPLB1	Data register (low bits)
SHPSC1	Start code register
SHPHB1	Data register (high bits).

4.56 ***Data/Status Selectors:*** The data/status selectors are composed of 2-to-1 multiplexors that select either data information from the shift register or status information from the 12 status bits. Normally, data is routed through the multiplexors. During the read status (RST) command lead RSTMC1 is high and status bits are routed through the multiplexors. The outputs of the multiplexors are gated onto the CCIO bus.

4.57 ***Bus Transceivers:*** These are used to interface the SCH to the CCIO bus and are controlled by the CC command signals.

B. Maintenance

4.58 Maintenance of the SCH implements hardware checks such as parity, start code, and error checks (invalid 3-out-of-6 code, decoder, stuck bus lead, sequencer, busy).

4.59 If a fault is detected in the SCH, and is verified by a second attempt, the CC and its dedicated periphery are switched off-line and the off-line units switched on-line. However, if the fault is detected in the PD, the PD is functionally switched to OOS and an appropriate TTY message is printed out.

4.60 The SCH has two maintenance states MST1 and MST2. State MST1 tests the sequencer error circuit and state MST2 tests the return start code flags and the sequencer internal ready flip-flop IRDY. These maintenance states are set up when inhibit I/O signal is set to prevent interference with PD communications, however if these states are erroneously set up during normal operations, an error condition is identified, and the results are transmitted to the CC. State MST1 generates a channel error and MST2 forces a clear of the data register that will generate parity errors on any subsequent read operation.

4.61 State MST1 forces the sequencer to simultaneously go into the transmit and receive states, to exercise the check circuit. Because it is abnormal for the sequencer to be in both states at the same time, when this occurs, a hardware fault is present. State MST2 forces the sequencer to terminate the receive state without having received a message from the PD. This facilitates testing of the sequencer internal ready flip-flop IRDY. All combinations can be loaded into the start code register to test the handshake ready flip-flop, the ASW response lead and the MR response lead.

5. Dual Serial Channel

Introduction

5.01 The DSCH is a semiautonomous unit providing an interface between the CC and 16 high-speed PDs. The DSCH also is used to provide an interface between the DMAC and the PDs. A maximum of four DSCHs per DMAC is allowed. The DSCH can provide the interface between the CC and another computer with or without a DMAC unit. The DSCH may be used to transfer 32-bit words or 16-word blocks of data. Data from/to the CCIO or DIO bus is in parallel form but data to the DDSBS is serial.

A. Physical Description

5.02 The DSCH consists of one circuit pack UN9, which is 7-3/4 inches by 14 inches. The DSCH resides in the DMA I/O unit (Figure 2) located in the upper portion of the CU frame or in the CC. When a DSCH is used with the DMAC, it is positioned in one of the positions (DMA I/O unit) DMAC CHAN 1 through 4 or DMAC CHAN 6 through 9. A DSCH not used with a DMAC can be positioned in one of the positions CHAN 2 through 6 (DMA I/O unit) or CHAN 0 and/or 1 (CC) as assigned.

B. Interfaces

5.03 ***Main Channel:*** The DSCH interfaces (Fig. 5) the CC via the CCIO bus and the PDs via 5-pair private serial data cables. Since the DSCH can provide for 16 PDs, 16 sets of these cables (maximum) are required. The DSCH interfaces the DMAC via the DIO bus and the PD via 5-pair private serial data cables. These cables contain two bidirectional data leads, a transmit clock, a receive clock, and a request lead. The PDs are interfaced to the DSCH via the DDSBS.

C. Functional Description

5.04 The DSCH (Figure 15) is a semiautonomous unit providing an interface to a maximum of 16 high-speed PDs. Differential DC line driving and receiving circuits provide a serial path for each PD. All signaling is compatible with EIA standard RS 422. Each PD interfaces the DSCH via five cables (two bidirectional data leads, transmit clock lead, receive clock lead, and a request lead). Two options are provided (based on requirement) to facilitate cable distances using the transmit clock frequency; 20 MHz for distances to 100 feet, and 10 MHz for distances to 250 feet (a backplane option strap is required).

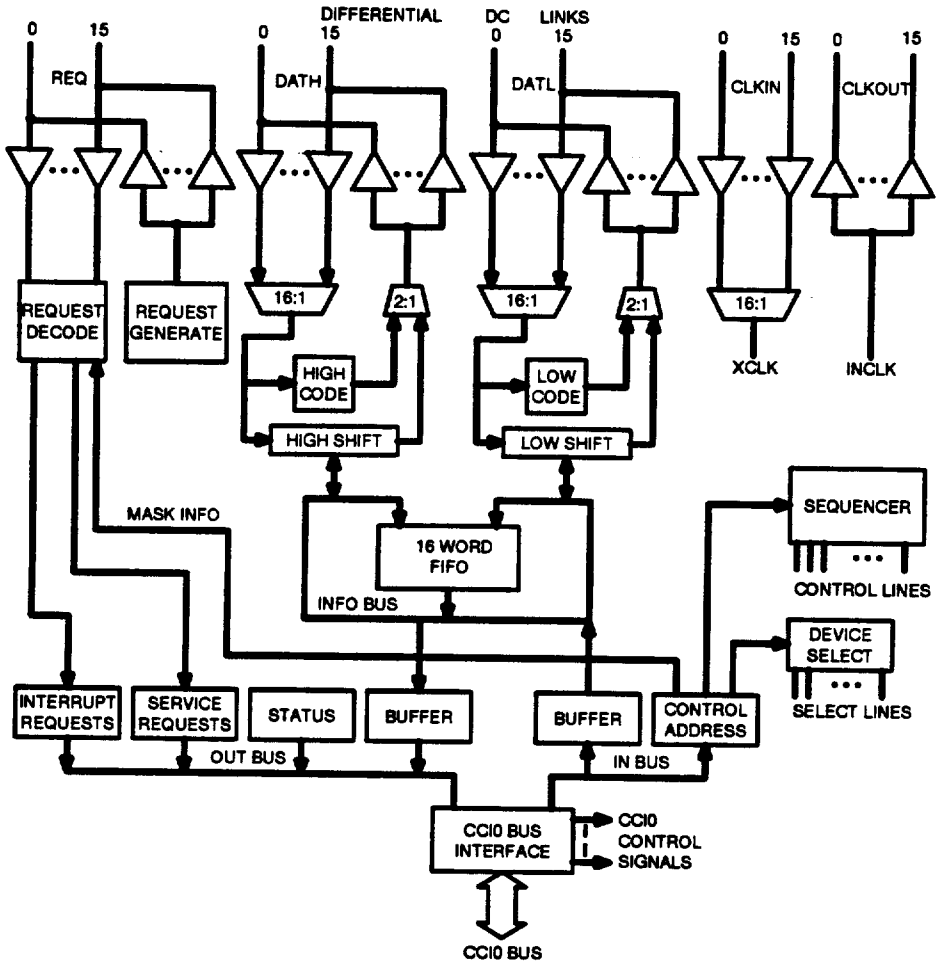


Figure 15. DSCH Block Diagram

5.05 Data message transmission is preceded by the start code (dual data messages, or twin start codes), all start codes begin with a leading 1 followed by a 1-out-of-3 code. The three possible start codes are 0011(3), 0101(5), and 1001(9). The two start codes transmitted to the PD specify the operation (see Table A).

Table A. Start Codes

Start Code		
High	**Low**	**Operation**
0011	0011	Write data (word mode)
0011	0101	Send PD command
0011	1001	Write data (block mode)
0101	0011	Read data (word mode)
0101	0101	Sense status
0101	1001	Read data (block mode)
1001	0011	End-of-transfer (EOT)

5.06 The two return codes transmitted to the CC are encoded by the PD to specify the success or failure of the operation (see Table B).

Table B. Return Codes

Return Code		
High	**Low**	**Outcome**
0011	0011	All seems well (ASW)
0011	0101	PD reported error
0101	0011	Invalid DDSBS command
0101	0101	Illegal start code received

5.07 The DSCH is capable of transferring 32-bit words with associated parity bits (each 8 bits has 1 parity bit - odd parity is maintained over the 9 bits; however, even parity is maintained over the entire word) or 16- word blocks of data and is specified by mode signals.

5.08 Write operations require 23-shift cycles for transmission; 4-shift cycles are required for reception. Read operations are the reverse of write, and require 4-shift cycles for transmission and 23-shift cycles for reception. A single start code and a single return code is sent with the sixteen 32 bits plus 4 parity bits when operating in the block transfer mode. Each data word is separated by a single bit of dead time to facilitate the DSCH transferring the next data word between its shift register and first-in first-out (FIFO) register.

5.09 The DSCH consists of the following circuits:

- Drivers and receivers
- Sequencer
- Registers

- Shift registers
- Decoder and encoder circuits
- Flip-flops
- Mask circuit
- Multiplexors.

5.10 Before each data transfer, the DSCH must be set up properly with address, control, and data information. An internal sequencer controls the serial transmission of data within the DSCH. Loading the DSCH control address register initiates the data transfer by the DSCH. If the control/address register contents specify a write operation, the sequencer loads the corresponding start codes and initiates transmission of data to the PD. The contents of the data buffers are serially transmitted until the buffers are empty, this is detected by the sequencer. On detection of empty data buffers, the sequencer goes into the receive mode, and the output data leads become the input data leads. Transmit clock pulses, still transmitted to the PD, are used by the PD to derive timing information. Data returning from the PD is recovered from the two bit streams and shifted into the DSCH return code shift registers. When the first "1" of the return message is shifted through the return code shift register and detected, the code is checked and outpulsing is terminated. For 100 feet of cable (10 MHz clock) the time for a single word transfer is approximately 4.5 microseconds. This includes a 900 nanosecond delay in PD and a 300 nanosecond delay for bus operations.

5.11 ***Reading Data/Status:*** The twin start codes are first transmitted to the PD. Then the sequencer goes into the receive state, the output data leads now are the input data leads. Data returning from the PD (via DDSBS) is recovered from the two bit streams and shifted into the data buffer. When the buffer is full, the return code is verified, and outpulsing is terminated. This operation has a time duration of approximately 4.5 microseconds per 32-bit transfer. When operating in the data block transfer mode, the DSCH will serially shift the incoming data bit stream into the shift register. When the shift register is full, it is parallel loaded into the FIFO register. This occurs a total of 16 times until the block transfer is complete. Approximately 40 microseconds are required for a 16-word transfer.

5.12 The PD interrupts and DMAC requests are received by the DSCH via request leads. Pulse-width modulation signals are used for service or maintenance interrupt requests. Two types of service requests are provided for the DMAC: a DMAC setup request and a DMAC data transfer request. The 16 interrupt and 32 service request (2 x 16) states are connected to the CC interrupt levels via the backplane wiring. Requests are identified to the PD by reading the PD request register via the data bus. Two 16-bit registers in the DSCH store the mask bits to inhibit requests from any of the 16 PDs. When masked, the request receivers are locked in an inactive state.

5.13 The DSCH can be used to directly link the CC with another computer. Computer-to-computer communications using DSCHs require special sequencing within each DSCH because the added computer in this configuration is considered a PD. Therefore, a DSCH must be able to transmit request signals to interrupt or request DMAC service of the remote computer. To prevent mutual interferences during

transmission between computers, the request lead is unidirectional. Two ports are required to let either computer initiate a transfer. The DSCH also has the ability to function similarly to a PD by generating a transfer request, receiving a start code from the remote DSCH/computer, identify if data accompanies the start code or data is requested. Then performing the requested transfer with the local computer (CC), and returning the proper return code with data/status if required. The DSCH can also be used to directly interface DMAC units of multiple computers in a multiprocessing situation.

5.14 ***DSCH PD Interrupts:*** Separate interrupt receivers are provided in the DSCH for each of the 16 PDs using the DSCH. The contents of these receivers can be read via request interrupt (RINT) and request service (RSR) command signals from the CC. Also, the CC can individually clear each of these requests via a clear command to the DSCH.

D. Theory of Operation

5.15 ***DSCH I/O Transfer-Write Data to PD:*** First, the DSCH and the PD to receive the data are selected. Each is tested for busy, if idle, the DSCH is loaded with the address, then data for a write operation followed by the WCA command, and the I/O sequence is initiated.

5.16 The DSCH simultaneously transmits the two serial data messages over the HI and LO serial data cables to the addressed PD (the PD is interfaced to the DSCH via a DDSBS selector). Data transfer is at a rate of 100 nanoseconds per bit. The DSCH then goes into the receive mode, and the output data bus now becomes the input data bus. While the PD is returning data, the DSCH continues to transmit the outgoing clock signal.

5.17 The DDSBS selector registers receive the input data from the DSCH. Then the DDSBS performs the parallel write data operation via the peripheral bus interface (PBI). The DDSBS gates the twin return codes response indicating the success or failure of the operation.

5.18 The DSCH is idle waiting for the twin return code response. On detection of a 1 in the zero position, 0 bit of both return code registers the DSCH terminates shifting and gating, then perform tests on the return code. If return code is valid, the DSCH signals the CC that a reply from the PD is available. If the return code is invalid, the DSCH signals the CC of an error condition.

5.19 ***Drivers and Receivers:*** These circuits are provided to interface the DSCH and the cabling to/from the PD (via DDSBS).

5.20 ***Multiplexors:*** The multiplexors are provided to select 1 of 16 devices.

5.21 ***Control and Address Register:*** This is loaded with the control and address data sent by the CC. The address data is used for the PD select circuit, the control data is gated to the sequencer that provides internal sequencing for the DSCH, mask

outputs are also provided for the request decode circuitry. A 3-out-of-6 decoding circuit is used for the address of the PD.

5.22 ***3-Out-of-6 Codes:*** The following is the 3-out-of-6 code for the PDs:

Device (hexadecimal)	3-Out-of-6-Code (binary)
0	000111
1	001011
2	001101
3	001110
4	010101
5	010110
6	011001
7	011010
8	100101
9	100110
a	101001
b	101010
c	110001
d	110010
e	110100
f	111000

This code is used to select and enable the PD requested by the CC.

5.23 ***Sequencer:*** The sequencer using the data from the control and address register, sequences the DSCH through the operation requested, such as write, read, idle, and maintenance operations.

5.24 ***Shift Register:*** This is used as an input/output FIFO shift register for the data and parity bits to/from the CC via CCIO bus and to/from the PD. Data gated out to the PD also has a DSCH generated twin start code.

5.25 ***Request Circuits:*** The request circuits (request decode, request generate, and multiplexor) provide the circuit to process request from the PD. The service request register (SER) contains a position for a request from each PD. Each PD may have its request inhibited by setting a bit in the mask register.

5.26 ***Clock Circuits:*** The transmit clock circuit in the DSCH generates a clock pulse for the PD to use for internal timing. The receive clock from the PD to the DSCH is gated though a 16 to 1 circuit.

5.27 ***CCIO Bus Interface:*** This circuit provides the interface between the CCIO bus signals and the DSCH. This interface uses transceivers for CCIO bus to DSCH circuit connections.

5.28 ***Status Bits:*** The contents of the status register are used to signal the CC of the status state of the DSCH.

Bit	Assignment
0-2	High 3 bits of low return code
3-5	High 3 bits of high return code
6	Channel busy flip-flop state
7	I/O inhibit override flip-flop state
8	Sequencer error
9	Illegal 3-out-of-6 PD address
10	Command error
11	Channel error
12	Maintenance flip-flop state.

5.29 ***DSCH Operations:*** The following is a list of available DSCH operations:

OPERATIONAL
Read Word*
Read Block*
Read Status*
Write Word*
Write Block*
Write Command*
NOP*

Send End of Transfer/Clear
Service Request

Set I/O Inhibit Override

Clear I/O Inhibit Override

*Available alone or with clear service request or clear interrupt.

INTERPROCESSOR
Request Word
Request Block
Ship Word
Ship Block
Generate Interrupt

MAINTENANCE
Set Read Flag
Set Illegal Bit
Send Data as Code
Generate Setup
Generate Transfer
Maintenance NOP
Send Data as Code/Response.

E. Maintenance

5.30 The occurrence of a fault in the computer CC or DSCH initiates a switch of the CC and its dedicated periphery. The DSCH is considered dedicated to a CC, and usually the PDs are connected to duplicated DSCHs (and CC). Therefore, a fault in a CC or DSCH does not result in loss of the PDs functions. However, if the PD is determined to be faulty, the CC places the PD OOS and an appropriate TTY message is printed.

5.31 The DSCH can be placed in the maintenance mode and tested by the CC. This test is performed by looping the input message through the DSCH and testing the output message. Additionally, the CC can test the state of various circuits in the DSCH

by the contents of the status register and test responses. The CC inhibits signals to the PDs, by the generation of an I/O inhibit command set to the DSCH.

5.32 The DSCH also has the following hardware circuits for maintenance performed during normal operations:

- 3-out-of-6 code
- Sequencer operations.

6. Application Channel Interface

Introduction

6.01 The application channel (ACHI) is a general purpose parallel interface between the CC and application (designed) circuits. The CC considers the ACHI as a programmed I/O channel. The ACHI provides a peripheral device (application designed) access to the CCIO bus and hence to the CC.

A. Physical Description

6.02 The ACHI is comprised of one circuit pack, the UN19B. The UN19B is 7-3/4 inches by 14 inches and resides in the DMA I/O unit channels 2 through 6 or in the CC channels 0 and 1. These unit channels are located in the CU frame (Figure 2). The number of ACHI provided is determined by the applications required.

B. Interfaces

6.03 The ACHI interfaces the CC via the CCIO bus. Two unidirectional parallel data busses interface the ACHI to the PD interface (PDI) unit. Normally, only one PD is used per ACHI, however multiple ACHIs may be provided. The maximum distance between the ACHI and the PD is 50 feet. Each signal between the ACHI and the PD is transmitted on DC differential lines. There is a total of 83 signal pairs.

C. Functional Description

6.04 The ACHI (Figure 16) accomplishes its functions via the following circuits:

- 32 + 4 parity bit input register
- 32 + 4 parity bit output register
- Flag flip-flops
- CCIO bus interface logic.

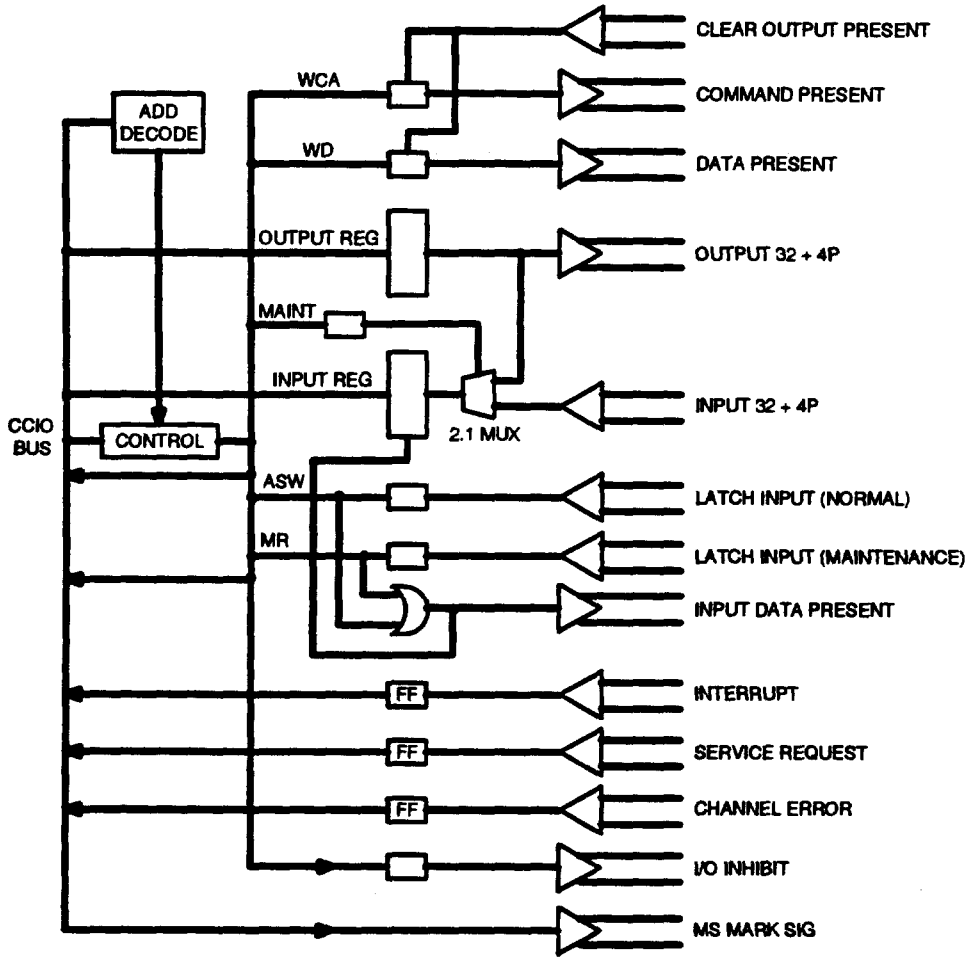


Figure 16. ACHI Block Diagram

6.05 Two flags are associated with the 32 + 4 parity bit output register, the data present (DP) flag and the command present (CP) flag. These two flags perform the handshaking between the CC and the PD during a write operation from the CC to the PD. On reception of a write data (WD) command signal from the CC, information is gated into the output register if both the DP and CP flags are reset. The information is clocked into the output register following the WD command signal. The DP flag is set on the trailing edge of the WD command signal. The PD clears (resets) the DP flag with its clear output present (COP) signal after the data on the write data leads (ACHI to PD) has been sampled.

6.06 The WCA signal clocks the control address data from the CCIO bus into the ACHI register. The CP flag is set on the trailing edge of the WCA command signal. Also, the COP signal from the PD clears (resets) the CP flag after the data (32 + 4 parity

bits) has been sampled off the write data leads by the PD. All 32 data and 4 parity bits of the data are available to the PD.

6.07 Data is transmitted from the PD to the CC (via ACHI) during a read operation. The latch input normal and latch input maintenance are the two control signals sent to the PD. The PD gates the read data message onto the read data leads (to the ACHI) and pulses one of the two control signals. The read data message is clocked into the input register on the leading edge of the control signal. Either one of the control signals sets the input data flag. Then, on a subsequent read data (RD) operation, the data is transmitted into the CC via CCIO bus and the input data present flag is cleared, following the trailing edge of the RD control signal. The PD should not pulse either of the latch input control leads while the data input present flag is set.

6.08 Latch input normal control signal is used to identify a data word and the latch input maintenance signal is used to identify an error or status message. The latch input normal signal, when set, activates the ASW signal during a read data (RD) command from the CC. The latch input maintenance signal, when set, activates the maintenance response (MR) signal during the RD command from the CC.

6.09 The input and output data registers are independent; therefore, write and read operations can take place at the same time between the ACHI and the PD (that is, the PD can load data into the data input register while data is unloaded from the data output register). The channel error signal lead provides a means for the PD to signal the CC of the occurrence of a hardware fault. A channel error signal is latched into the channel error flip-flop of the ACHI when a PD hardware fault is detected. This flip-flop is reset by reception of the clear error signal from the CC. When the channel error flip-flop is set (signal from the PD) an error interrupt signal is transmitted to the CC via CCIO bus from the ACHI.

6.10 Signal leads provide the following functions:

- Interrupt: A signal on the interrupt lead sets the interrupt latch in the ACHI and an interrupt request is gated to the CC. A priority is assigned to interrupts, and the CC recognizes interrupts in order of priority.
- Service Request: A signal on the service request lead sets the service request in the ACHI and subsequently indicates a service request to the CC.
- I/O Inhibit: When active, the I/O inhibit signal indicates to the PD that the connected CC is off-line and I/O operations disabled. This signal can be overridden for diagnostics.
- Mark Signal (MS): The MS signal lead provides a timing signal interface between the CC and PD (via ACHI). However, the ACHI does not perform any operations on the MS signal.

6.11 The CC controls the operation of the ACHI via 12 command signals. All control signals are active low, and the operations are performed only when the ACHI main channel address is present. Also, there are three address acknowledge signal leads, which are active when the ACHI main channel address is correct and one of the

12 control signals is active. Additionally, three handshaking response signal leads are used; these are all seems well (ASW), ready (RDY), and maintenance response (MR).

6.12 ***Write Data (WD):*** Command signal WD is used to load data from the CC via CCIO bus into the ACHI output register and set the data present (DP) flag signal to the PD. Data is clocked into the output register in response to the leading edge of the WD command signal. The DP flag signal is set on the trailing edge of the WD command signal. Data is clocked into the ACHI only when the DP and command present (CP) flags are reset before the WD command signal is received. If the DP and CP flags are reset, the ACHI transmits the RDY and ASW signals to the CC. However, if either the DP or CP flag is not reset, the ACHI does not load the output register and the RDY signal is not sent to the CC.

6.13 ***Write Command Address (WCA):*** The WCA command is also used to load data from the CC via CCIO bus into the ACHI and set the CP flag. The CP flag signals the PD that a command word is present and ready in the ACHI output register. Data clocked into the output register in response to the leading edge of the WCA signal, and the CP flag is set on the trailing edge of the WCA signal. Data are clocked into the output register only when the DP and CP flags are in the reset state before the reception of the WCA signal. If the DP and CP flags are in the reset state, ASW and RDY signals are sent to the CC by the ACHI. If either the DP or CP flag is set, the ACHI does not load the data into the output register and does not transmit a RDY signal to the CC.

6.14 ***Read Data (RD):*** This command signal provides for transferring the contents of the ACHI input register to the CC via the CCIO bus. The data is valid only when the RDY flag is set during the RD command. The RDY flag is set when either the latch normal or latch maintenance flip-flops have been set by the PD. When the latch normal flip-flop is set, the ASW signal is activated. Also, when the latch maintenance flip-flop is set, the MR signal is activated. Signals MR and ASW during the RD command sequence are only valid when RDY is activated. Latch normal flip-flop or the latch maintenance flip-flop is reset on the trailing edge of the RD command signal if either was set on the leading edge of the RD command signal.

6.15 ***Idle (IDL):*** Command signal IDL is used to put the ACHI into the maintenance mode. Bit format of the data word during the IDL command sequence identifies the operation to be performed by the ACHI. The ACHI maintenance register is cleared with the IDL command by an all zero (0) data word from the CC.

6.16 ***Clear Error (CLR):*** This command signal is used to reset the ACHI into a known state. The DP and CP flags are reset, the latch normal and latch maintenance flags are reset, the read ready flip-flop is reset, the maintenance state register is reset, and channel error flip-flop is reset.

6.17 ***Read Interrupt (RINT):*** The RINT command signal gates the state of the interrupt flip-flop onto the bit 0 of the CCIO bus data leads. Command RINT is a read-and-clear operation with the interrupt flip-flop being reset on the trailing edge of the RINT signal.

6.18 ***Read Service Request (RSR):*** Command signal RSR gates the state of the service request flip-flop onto bit 0 of the CCIO bus data leads. The RSR command is a read-and-clear operation, with the service request flip-flop being cleared on the trailing edge of the RSR signal.

6.19 ***Interrupt Acknowledge (IACK):*** This command gates the state of the interrupt flip-flop onto the designated bit position of the CCIO bus data leads. The designated bit depends on the main channel address that the ACHI has been assigned on the CCIO bus, ie, for main channel address 0, the designated bit would be bit 0 on the CCIO bus data leads.

6.20 ***Error Acknowledge (EACK):*** The EACK command gates the state of the channel error flip-flop onto the designated bit of the CCIO bus data leads. The designated bit depends on the main channel address the ACHI is assigned on the CCIO bus (that is, main channel address 0, the designated bit would be 0 on the CCIO bus data leads).

6.21 ***Service Request Acknowledge (SRACK):***
The SRACK command gates the state of the service request flip-flop onto the designated bit of the CCIO bus data leads. Again, the designated bit depends on the main channel address that the ACHI has been assigned on the CCIO bus (that is, main channel address 0, the designated bit would be bit 0 on the CCIO bus data leads).

6.22 ***Read Status (RST):*** The RST command signal gates the ACHI status bits onto the CCIO data bus. Parity bits are always 0 for the RST reply signal because parity is not valid over the status bit format.

6.23 ***Inhibit I/O (INH):*** When INH is active, this signal indicates that the CC is off-line and I/O operations are to be disabled. Signal INH can be overridden for diagnostics via a command to the ACHI. When the INH signal becomes active, the override I/O inhibit flip-flop and the ACHI maintenance register are cleared. When the INH signal is active, the inhibit signal to the PD is made active. Normal I/O operations can be performed though the ACHI (because the state of INH does not affect any control state in the ACHI).

6.24 Nine response leads on the CCIO bus from the ACHI to the CC. These are ready (RDY), all seems well (ASW), maintenance response (MR), interrupt (INT), service request (SER), channel error (CER), and three address response leads (AKA, AKB, and AKC). The address response signals are made active whenever the ACHI main channel address and a control command is present on the CCIO bus. The INT signal is made active whenever the PD has sent an interrupt signal to the ACHI. The SER response signal is made active whenever the PD has sent a service request signal to the ACHI. Signal CER is activated whenever the PD sends a channel error signal to the ACHI. Signals INT, SER, and CER can be made active by the ACHI during routine diagnostics (ACHI is in the maintenance state). When the ACHI is in the maintenance state, PD inputs are inhibited.

6.25 Signal MR is made active only in the read data operation, when the latch maintenance flag has been set by the PD. However, MR signal is valid only when the RDY signal is active. Response signal ASW is always made active for all control signal inputs except the read data (RD) command. During the RD command, ASW is made active when the PD has activated the latch normal flag; also during RD, the ASW signal is valid only if the RDY signal is activated. Except for RD, WD, and WCA operations, the RDY signal is always active. For WD and WCA commands, RDY is active when data present (DP), or command present (CP) flags have been cleared by the PD (from the last write operation). During the RD operation, if the latch normal or latch maintenance flag has been set by the PD, the RDY signal is set.

6.26 ***Interface ACHI to PD:*** Each signal between the ACHI and PD is through DC differential lines, with a total of 83 signals. Data leads have odd parity over each byte (8 + 1 parity bits) and even parity over entire word (32 + 4 parity bits); a 1 is defined by the positive lead being positive with respect to the negative lead. Also, the active state of the control signal is defined as the positive lead being positive with respect to the negative lead.

Control Signals (ACHI to PD)

6.27 ***Data Present (DP):*** The DP signal is activated when valid data has been loaded into the data output register (ACHI) with the write data (WD) command. The data leads become stable in response to the leading edge of the write data command signal, and the data present flag becomes set on the trailing edge of the WD command signal.

6.28 ***Command Present (CP):*** The CP signal is activated when valid data has been loaded into the ACHI output register with the write control address (WCA) command. The data leads become stable in response to the leading edge of the WCA signal, and the command present (CP) flag becomes set on the trailing edge of the WCA signal.

6.29 ***Data Read Present Flag (DRPF):*** The DRPF signal becomes set when the PD has loaded a data word into the ACHI input register via the latch normal or latch maintenance signals. This flag signals the PD that the CC has not retrieved the last word stored in the ACHI input data register. The PD should not activate the latch normal or latch maintenance input signals while the DRPF signal is set. On a successful read data operation, the CC resets the DRPF signal.

6.30 ***I/O Inhibit (INH):*** When the INH signal is active, the PD is signaled that the CC is off-line and I/O operations should be disabled.

Responses Between ACHI and PD

6.31 ***Latch Input Normal (LIN):*** The PD uses this response signal to load a status or error word into the ACHI input register and to set the maintenance response flip-flop. The data is clocked into the input register on the leading edge of the response signal, and the PD must meet the setup requirements of the ACHI input register. When LIN is activated, the ACHI gates the maintenance response (MR) signal to the CC on the next read data command.

6.32 ***Clear Output Present Flag (CLRF):*** The PD activates the CLRF signal to signal the ACHI that the contents of the output register have been accepted. Signal CLRF clears the command present and data present flags in the ACHI, this informs the CC that new data can be gated into the output data register. This gives added protection against a failure of the ACHI clocking circuits. If the CC cannot load data into the data output register because of an ACHI failure, the PD will sense an all-zero word with the wrong parity.

6.33 ***Channel Error (CHER):*** Activation of the CHER signal (pair) sets the error flip-flop in the ACHI. The ACHI gates the output of the error flip-flop onto the common channel error lead of the CCIO bus, thereby signaling the CC of an error interrupt.

6.34 ***Interrupt (INT):*** Activation of the INT signal sets the ACHI interrupt flip-flop. The ACHI gates the output of the interrupt flip-flop onto the interrupt lead to the CC.

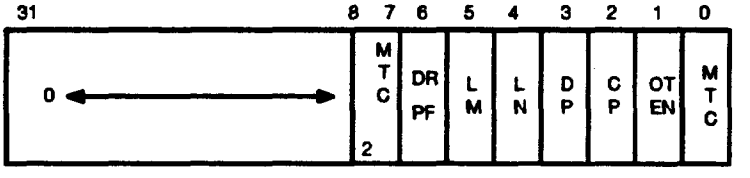
6.35 ***Service Request (SER):*** Activation of the SER signal sets the ACHI service request flip-flop. The ACHI gates this output to the CC via the service request lead.

Communications

6.36 ***Write:*** In order to transmit a word from the CC to the PD via the ACHI, the ACHI must not be in the busy state. The CC sets up the ACHI main channel address via CCIO bus followed by gating the 32-bit data word onto the CCIO bus to the ACHI. The CC then transmits a write data or write command address command signal to the ACHI. If the write data command is sent to the ACHI, the ACHI gates a data present signal to the PD. If the write command address is sent to the ACHI, the ACHI gates the command present signal to the PD. The output register is loaded on the leading edge of the command signal, and the data present or command present flags are set on the trailing edge of the command signal. The data present or command present signal notifies the PD that write data is present on the write data lines. The PD receives the data word and clears the data present or command present flag in the ACHI by activating to clear the output present flag (CLRF) lead. The next word is formatted by the CC while the PD receives the first data word. The CC may use either of two methods of sending the next word to the ACHI: first, the CC gates the data word onto the CCIO bus and goes into a loop of activating the write data or write command address signal and testing for the return RDY response. When the PD has cleared the data present or command present flags, the ACHI returns the RDY signal in response to the write data or write command address command signal and sets the data present and command present flags. The ACHI returned RDY signal indicates to the CC that the second word has been received by the ACHI. second, the CC loops on the read status (RST) command signal after the first word has been transmitted to the ACHI. When the PD has reset the data present or command present flag in the ACHI, the status word reply to the CC indicates that the flags have been cleared/reset. The first method has the advantage of being faster especially in transmission of many words from the CC to the PD.

6.37 ***Read:*** The PD gates the 32-bit word onto the read data leads and activates the latch normal or latch maintenance flags. An indication of either latch normal or latch maintenance flag being set is sent to the PD via the input data present signal. The PD should not activate the latch normal LIN or LIM while the read data present flag (DRPF) signal is activated. Signals LIN and LIM clock the information off the read data leads on the leading edge of the signals. As with the write operation, either of two methods may be used to retrieve the read data word out of the ACHI input register: First, the CC loops on the read data command until the RDY signal is returned to the CC by the ACHI. When RDY is activated, the CC senses that a valid read data word has been gated onto the CCIO bus by the ACHI. The ACHI resets latch normal and latch maintenance flags on the trailing edge of the RD command signal. Second, the CC loops on the read status command until it recognizes that the DRPF is set. On the next RD command signal, the RDY flag output is returned to the CC, and the read data is present on the CCIO bus data leads. The first method is faster and requires fewer instructions.

6.38 ***Status:*** The operational control states can be monitored with the read status (RST) command signal from the CC. This command does not interfere with any data transfer between the ACHI and the PD. There are eight status bits (Figure 17).



0 1 = MAINTENANCE STATE
0 = NORMAL
1 1 = OUTPUT TO PERIPHERAL DEVICE IS ENABLED
0 = OUTPUT TO PERIPHERAL DEVICE IS INHIBITED
2 COMMAND PRESENT FLAG
3 DATA PRESENT FLAG
4 LATCH INPUT NORMAL FLAG
5 LATCH INPUT MAINTENANCE FLAG
6 READ DATA PRESENT FLAG = "OR" FUNCTION OF BITS 4 AND 5
7 2ND MAINT STATE

Figure 17. ACHI Status Bit Assignment

6.39 These status bits (0 through 5), when set, indicate the following:

Bit	Indicated Operation (when set)
0	ACHI is in the maintenance state
1	Outputs to PD are enabled
2	Command present flag is set
3	Data present flag is set
4	Latch input normal flag is set
5	Latch input maintenance flag is set.

Bit 6 is the OR function of the latch input normal and latch input maintenance flags. Bit 7 is the maintenance state 2.

6.40 ***Initialization:*** When power is first applied to the ACHI, some flip-flops may be set in the wrong state. Therefore, to restore the ACHI into a known state, three command signals are sent by the CC. Clear error (CLR), read interrupt, and read service request initializes the handshake logic and clears the channel error flip-flop. The read interrupt (RINT) signal clears the interrupt flip-flop and read service request (RSR) clears the service request flip-flop. The CLR command is also used to reset the handshaking flags after data transmission through the ACHI has been aborted.

D. Theory of Operation

6.41 Buffers provide the interface circuitry for the command signals from the CCIO bus to the ACHI. These buffers are noninverting Schmitt triggers. All command signals are ANDed with the three main channel address signals ADAIO, ADBIO, and ADCIO. The ACHI ignores all commands unless the main channel address is valid. However, the inhibit I/O signal (INHIO) and the millisecond mark signal (MSMIO) are not gated with the main channel address.

6.42 Signals IACK, EACK, and SRACK are ANDed with the main channel address to generate the ready signal (RDYO0). The RDMCBO or the RSTMCO signal activates the EDSTO to gate data or status bits on the CCIO bus. These bits are multiplexed onto the CCIO bus data leads. Signal READO or GATBX1 activate signal GBOXO (gate bit 0 or gate bit designated) to gate bit 0 (or designated bit) onto the CCIO bus data leads. Signal CMGA1 is activated by the ORed result of the RDMCO, WDMCO, and WCAMCO signals. Signal CMDA is connected to a delay line for an internal delay. Signal ACK1 gates the address reply signals ACKAO0, ACKBO0, and ACKCO0 onto the CCIO bus address response leads. Signal MRO0 is activated during the time that signal RDMC1 (read data and main channel address) and the MFAG1 signal are activated. This takes place when the PD has set the ACHI MFLAG with the latch input maintenance reply lead. When signal ACK1 is active and signal RDMC1 is inactive signal, ASWO0 is activated. When signal RDMC1 is active, signal ASWO0 is activated when signal NFLAGO is also active. This occurs when the PD has set

the NFLAG signal with the latch input normal response lead. Signal RDYO0 is activated when one of the 11 inputs to the RDY1 gate is activated.

6.43 The maintenance register consists of 9 bits. The D-triggered register is loaded from the CCIO bus data leads on the leading edge of signal IDLMC0. Leads IOO1 through IO81 are the data inputs from the CCIO bus. These bits (0 through 8), when active, perform the following:

Bit	Operation
0	Sets I/O inhibit override bit
1	Sets ACHI maintenance state
2	Sets channel error
3	Sets interrupt flip-flop
4	Sets service request flip-flop
5	Sets normal message received flag
6	Sets maintenance message received flag
7	Clears the data present and command present flip-flops
8	Sets ACHI maintenance state 2.

6.44 The maintenance register is cleared by three input signals, PCLRO, PG20, and CLRMCO. However, bit 1 (maintenance state 1) is not cleared by signal CLRMCO. Signal PCLRO is active when the bus power enable signal is not present from the ACHI (ACHI is in the power-down mode). Signal PG20 is the output of a monopulser (1-shot), which generates a signal on the inactive-to-active transition of the inhibit I/O signal. Signal CLRMCO is the clear error signal from the 3B20D computer CC.

6.45 ***Handshake Logic:*** The handshake logic is used to arbitrate the asynchronous read and write operations between the CC and the PD.

6.46 ***Read:*** When the PD transmits data to the ACHI, the N, or M flip-flops are clocked by signals SNO or SMO (SNO-N, SMO-M). Signal SNO is used for the normal message, and signal SMO is used for a maintenance message. The leading edge of the SNO signal sets NFF flip-flop and clocks the input data register via signal CKRR1. An indication of the NFF flip-flop being set is gated back to the PD via signal DRPF1. When the CC performs a read operation, signal RDMC1 clocks the HRDY1 flip-flop because; 50 nanoseconds later the RDRDY flip-flop is clocked. Therefore, because flip-flop HRDY1 is set, the RDRDY flip-flop gets set also. Signal RDRDYO is used to gate the ready indication to the CC via the RDYO0 lead. A 50-nanosecond wide pulse is generated on the output of gate TPO after the CC has terminated the RD command signal. This pulse clears the RDRDY flip-flop. The high-to-low transition on the RDRDY1 lead triggers the PG1 monopulser (1-shot). The PD10 signal clears the NFF flip-flop and clears the input data register. Flip-flop NFF being set terminates the DRPF1 signal to the PD, facilitating the PD setting the latch input normal or latch input maintenance flags in preparation for the next data transfer. If the CC performs a read

operation and flip-flops MFF and NFF are not set, flip-flop HRDY1 would not become set and flip-flop RDRDY would remain cleared. This prevents the transmission of the ready indication via the RDRDYO lead. At the end of the read data command, the signal at the output of the TPO gate does not generate a high-to-low transition on the RDRDY1 lead and the PG1 monopulser would not be triggered.

6.47 ***Write:*** Handshaking between the CC and PD for a write operation is accomplished by flip-flops WD, WCA, HRDY2, HRDY3, DP, and CP. The data present (DP) flip-flop is set to signal the PD that the CC generated a write data (WD) command signal. Command present (CP) flip-flop is set to signal the PD that the CC generated a write command address (WCA) command signal. When the DP flag flip-flop is not set and the CC gates the data word for the PD on the CCIO bus, the CC activates the write data (WD) command lead. This generates a low-to-high transition on the WDMC1 lead. The output of the RS1 gate is low; therefore, the WD flip-flop cleared, and the WD1 lead goes high. The signal on D1 lead clocks the HRDY2 flip-flop 50 nanoseconds later; since the WD1 signal lead is high, the HRDY2 flip-flop is set. The WDRDYO signal is activated to clock the output register via signal CKWDR1; also the WDRDYO signal activates the ready signal via the RDYO0 lead. This ready signal is an indication to the CC that the data word has been accepted by the ACHI. When the CC terminates the write data command signal, a 50-nanosecond wide pulse is generated at the output of the TPO gate. This pulse clears the HRDY2 flip-flop. The low-to-high transition on the WORDY signal lead clears the DP flip-flop (cleared state of the DP flip-flop is the active state). The active state of the DP flip-flop is used to indicate that data is present in the ACHI output register and should be retrieved by the PD. After the PD has accepted the data word from the output register, the PD sets the DP flag via a low-level signal on the CLRFO lead. The ACHI output register is also cleared by the CLRFBO signal. If the CC attempts to load a new data word into the ACHI output register before the DP flag is cleared, it must loop on the write data command until the PD has reset the DP flag. This is because as long as the DP flag is set or the CCRFBO signal is active, the output of the RS1 gate is high. Also, the WDMC1 signal in response to the write data command clocks the WD flip-flop; however, since gate RS1 is high, signal WD1 remains low. Additionally, 50 nanoseconds later the D1 signal clocks the HRDY2 flip-flop, but signal WDRDYO remains high, and the output register is not clocked via the CKWDR1 signal lead, and the not-ready response is gated to the CC.

6.48 ***Output Register:*** The output register is 36 bits wide (32 data bits and 4 parity bits). The register is clocked on the leading edge of a high-level signal on the CKWDR1 lead. Signal CKWDR1 occurs 50 nanoseconds after the leading edge of the WCA or WD command signal when the DP or CP flag flip-flop is not set (in the handshake logic). The register is cleared by a low-level signal on the CLRFBO lead. Signal CLRFBO occurs in response to the clear output present flag (CLRF) when the PD has received the data word stored in the output register.

6.49 ***Write Data Drivers:*** Information in the output register is gated to the 36 write data drivers. The write data drivers convert the data information to differential form, and transmit the converted data to the PD. Signal INHOT1, when active, forces the output drivers into the high impedance state. Signal INHOT1 is active only when the ACHI is in the maintenance mode.

6.50 ***Read Data Receivers:*** The read data receivers receive data from the PD and convert the differential data to the single-ended format data.

6.51 ***Data Multiplexors:*** In the normal mode of operation, the MTCB1 signal is low. This causes the read data information on the RXX1 lead to be on the output of the multiplexor MRXX1 lead, etc. In the maintenance mode of operation, signal MTCB1 is high and the write data information on the WXX1 lead is on the output of the multiplexor MRXX1 lead, etc. This establishes the loop-around functions from the output register to the input register.

6.52 ***Input Register:*** The input register is 36 bits wide (32 bits of data and 4 parity bits). The input register contains the read data information from the PD until the CC can retrieve it. The input register is clocked on the leading edge of a high-level signal on the CKRR1 lead. Signal CKRR1 is generated in response to the latch input normal or latch input maintenance signal from the PD. The input register is cleared via a low-level signal on the PG10 lead. The PG10 signal occurs in response to a read operation command from the CC.

6.53 ***Data/Status Multiplexor:*** The multiplexor determines whether the outputs of the input register or the status bits are gated to the CCIO bus data leads. During a read-status operation, the RSTMCO signal is low, and the status bits are gated onto the CCIO bus. At all other times the RSTMCO is high, and the output of the input register is gated onto the CCIO bus.

6.54 ***CCIO Bus Transceivers:*** When the transceivers are enabled, the ACHI outputs data onto the CCIO bus data leads. The IXX1 leads send information to the output and maintenance registers. During a read data operation from the CC, signals RDMCBO, GDSTO, and GBOXO are low, and the 36 bits of data from the input register are gated onto the CCIO bus. During a read status operation from the CC, signals GDSTO and GBOXO are low, and status bits 0 through 7 are gated onto the CCIO bus. During the interrupt acknowledge (IACK), error acknowledge (EACK), and service request acknowledge (SRACK) operations, the GBOXO signal is low, and the state of the BITX1 lead is gated onto the CCIO bus.

6.55 ***Pulse Receivers:*** A low-level signal on the SSRO0 lead sets the SER (service request) flip-flop. An indication is sent to the CC (via SEROO lead) when the SER flip-flop is set. The SER flip-flop is cleared on the trailing edge of a low-level signal on the output of the RSRMCO gate. This signal occurs due to the read service request (RSR) signal generated by the CC. A low-level signal on the SINTO lead sets the interrupt (INT) flip-flop, with an indication sent to the CC (via INTO0 lead). The INT flip-flop is cleared on the trailing edge of a low-level signal on the output of the RINMCO gate. This signal occurs as a result of the read interrupt (RINT) command signal from the CC. The channel error flip-flops (CERL1 and CERLO) are set by a low-level signal on the SCHRO lead, with an indication being gated to the CC (via the CERO0 lead). The channel error flip-flops are cleared by a low-level signal on the CLRMCO signal which occurs as a result of the clear error (CLR) command from the CC. The SER and INT flip-flops can be tested by using the 1HPU1 lead.

6.56 ***Control Drivers:*** The control drivers interface the control signals (ACHI) to the PD. Five differential drivers provide handshaking signals to the PD. A control function is active when the P lead is positive with respect to the N lead. Signal DPF is the data present flag and becomes active when the CC has performed a write data (WD) operation. Signal CDF is the command present flag and becomes active when the CC has performed a write command address (WCA) operation. Signal DRPF is the data read present flag and becomes active when the PD has transmitted data into the input data register via latch normal or latch maintenance signal. Signal MSMK is the millisecond mark signal from the CC. Signal INHOT1 forces the control drivers into the high-impedance mode when the ACHI is in the maintenance mode. Signal INHO is the inhibit I/O signal to the PD and becomes active when the ACHI maintenance state is set or when the inhibit I/O signal is activated by the CC. Relay K1 removes power from the inhibit I/O driver when the bus power enable signal BPENIO is absent from the ACHI. Signal PCLRO is the power clear signal. When relay K1 is open, the PCLRO signal is active to initialize the handshaking logic.

6.57 ***Control Receivers:*** The control receivers interface the control command received from the PD for the ACHI. Six differential control signals are received from the PD. A signal is active when the P-lead is positive with respect to the N-lead. Signal CLRF1 is the signal used by the PD to clear the command present (CP) and data present (DP) flags. Signal CHERI is used to set the channel error flip-flop to indicate to the CC that the PD has detected an error condition. Signal LINI is the latch input normal signal used by the PD to load the input data register and to set the normal message flip-flop. Signal LIMI is the latch maintenance signal used by the PD to load the input data register and to set the maintenance register flip-flop. Signal INT1 is used to set the interrupt flip-flop, and signal SER1 is used to set the service request flip-flop. All outputs of the differential line receivers are active low. The receivers are forced into the high-impedance mode (for diagnostics) when the INHOT1 signal is high. When the ACHI maintenance state is set, the signal on the MTCBO lead is low. This enables maintenance drivers MDRA and MDRB. The inputs to the maintenance drivers are received from the maintenance register. This facilitates the setting of the internal ACHI response signals.

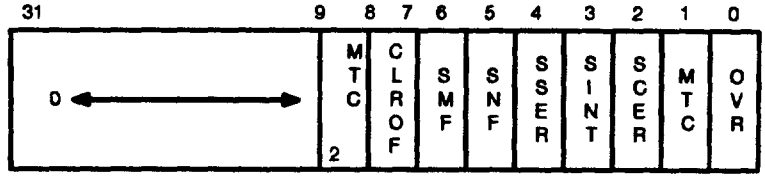
E. Maintenance

6.58 Duplication of the ACHI, that is each CC has a dedicated ACHI, facilitates the switching of the CC and its dedicated periphery (by providing duplicate access to PDs) when a fault occurs and is verified in the CC or its dedicated periphery. However, if the fault exists in the PD, the PD is placed out of service and an appropriate TTY message is printed.

6.59 ***Maintenance Strategy:*** The ACHI has been designed with the following criteria: Faults on either side of the CCIO bus do not require the aid of the peripheral device for fault resolution. Normal inputs from the device and all interface functions between the processor and the ACHI can be exercised using the ACHI maintenance states. For failure detection, 4-parity bits are carried along with every 32-bit data word. For additional failure detection, the output register, the input register, and the differential line drivers and receivers are bit-sliced. For maintainability of the data transfers through the ACHI, the input and output data registers are cleared automatically after each data

transfer. This mechanism provides some degree of self-checking for the ACHI clocking circuits. A failure of the clocking circuits will cause a parity error on a subsequent data transfer.

6.60 ***Maintenance State 1:*** The maintenance command bit assignment is shown in Figure 18. The particular bit configuration on the CCIO data bus when the IDL command is pulsed sets bits in the maintenance register. The outputs of the register perform the functions as outlined in Figure 18. Maintenance state 1 is set by pulsing the IDL command with data bit 1 active. When the ACHI is in this maintenance state, the write data and the control lines to and from the peripheral device are tristated. In maintenance state 1, the Inhibit I/O signal is also asserted to the device. For diagnostic purposes, the outputs of the output data register are looped to the inputs of the input data register. Thus, by writing data into the output register, followed by pulsing the latch normal or latch maintenance leads, the data is looped around and may be read from the ACHI. Before another loop operation may be performed, the latch normal and latch maintenance flags, along with the Data Present (DP) and Command Present (CP) flags, must be reset.



0 INHIBIT OVERRIDE
1 MAINTENANCE STATE
2 SET CHANNEL ERROR
3 SET INTERRUPT
4 SET SERVICE REQUEST
5 SET LATCH NORMAL FLAG
6 SET LATCH MAINTENANCE FLAG
7 CLEAR OUTPUT READ FLAGS
8 2ND MAINT STATE

Figure 18. ACHI Command Bit Assignment

6.61 ***Maintenance State 2:*** A second maintenance state, incorporated into the ACHI, performs a different function than maintenance state 1. Like maintenance state 1, maintenance state 2 tristates the control signals to and from the peripheral device. The write data leads are not disabled as in maintenance state 1, and the output register is not looped to the input register. The only functions that can be performed from the maintenance register are: INHIBIT OVERRIDE, LATCH NORMAL, LATCH MAINTENANCE, and CLEAR OUTPUT READY FLAGS. This allows data to be written into the output register and latched into the input register by pulsing LIN or LIM and then read from the ACHI. This sequence of events with the ACHI connected to a Peripheral Systems Interface (PSI) loops data through the PSI thus checking the ACHIs and PSIs drivers and receivers. Again, LIM, LIN, CP, and DP flags must be reset before any subsequent loop operations.

7. Duplex Dual Serial Bus Selector

Introduction

7.01 The DSCH to PD interface is provided by the duplex dual serial bus selector (DDSBS). Two DSCH signal ports are provided on the DDSBS so that either CC in a duplex configuration can access the PD. The DDSBS performs the serial-to-parallel and signal level conversions to drive the transistor-to-transistor logic (TTL) level peripheral bus interface (PBI) between the DDSBS and the PD.

A. Physical Description

7.02 The DDSBS is physically located in the equipment with the PD requiring its functions. The DDSBS is also equipped with a PBI circuit. Circuit pack TN69 comprises the entire DDSBS; this circuit pack is 7-3/4 inches by 14 inches. The DDSBS is considered a subunit of the unit requiring its functions.

B. Interfaces

7.03 The DDSBS is interfaced to the DSCH via two bidirectional data leads, a transmit clock lead, a receive clock lead, and a request lead. The DDSBS is interfaced to the PD via the peripheral bus interface, which uses a bidirectional data bus (32 data bits and 4 parity bits), control leads (command present, data present, data request, sense status, and end-of-transfer), and response leads (sync, error, data transfer, DMAC setup, and interrupt). The transmit clock from the DSCH may be 20 MHz for cable distance (between the DSCH and DDSBS) of up to 100 feet, and 10 MHz for cable distances up to 250 feet (a backplane option strap is required).

C. Functional Description

7.04 The DDSBS (Figure 19) consists of the following circuits:

- Drivers and receivers
- Selectors
- Registers
- Shift registers
- Sequencers
- Peripheral bus interface.

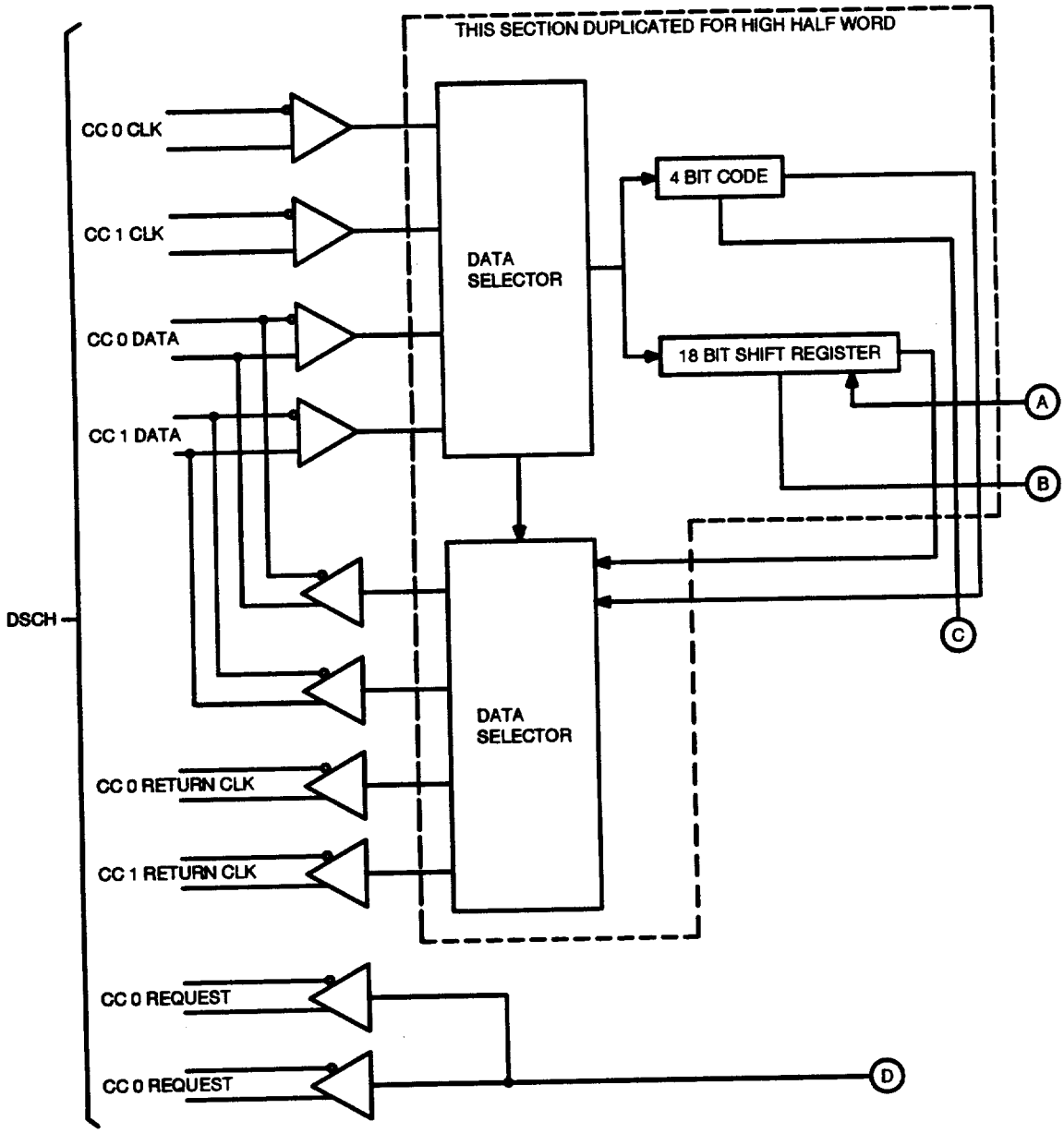


Figure 19. DDSBS Functional Block Diagram (Sheet 1 of 2)

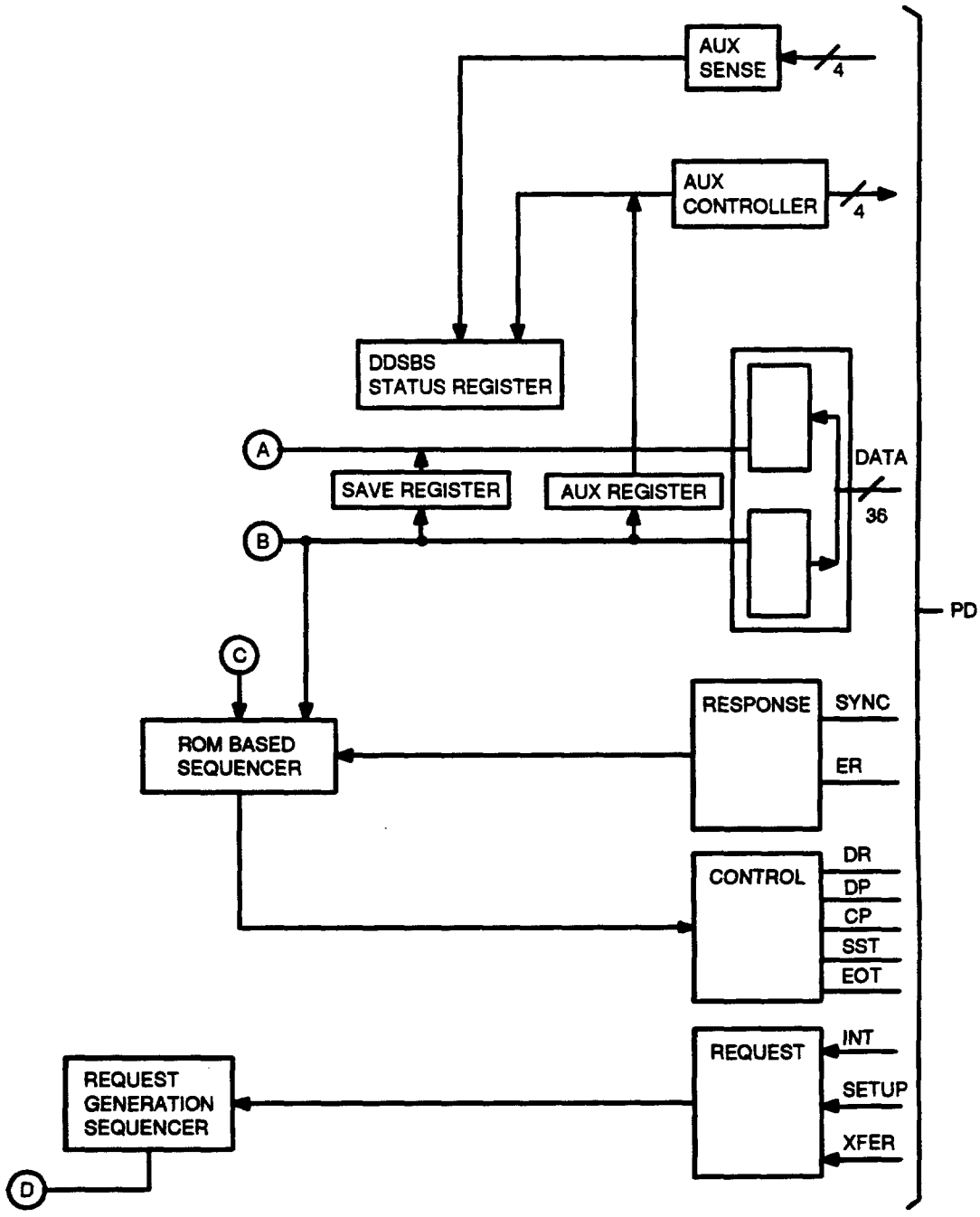


Figure 19. DDSBS Functional Block Diagram (Sheet 2 of 2)

7.05 ***Peripheral Bus Interface:*** The PBI provided in the DDSBS consists of 46 active-low TTL signals, 36 data leads, 5 control leads, and 5 response leads (Figure 20). The 36 bidirectional data leads transmit data/commands, or receive data/status from the PD. The 36 data bits comprise four (8 data bits and 1 parity bit) bytes, with odd parity over each byte and even parity over the 36-bits. The DDSBS accesses 32-bit PDs (only 32-bit PDs can set up DMAC units).

7.06 The five control signals are as follows:

- Command Present (CP)—Instructs the PD to interpret the data on the INF (data leads as a PD command).
- Data Present (DP)—Instructs the PD to interpret the data on the INF leads as PD data.
- Data Request (DR)—The PD is requested to gate its data onto the INF leads.
- Sense Status (SST)—The PD is requested to gate its status onto the INF leads.
- End-of-Transfer (EOT)—The DMAC signals the end of a DMA block transfer via EOT (EOT is not provided by the DSCH).

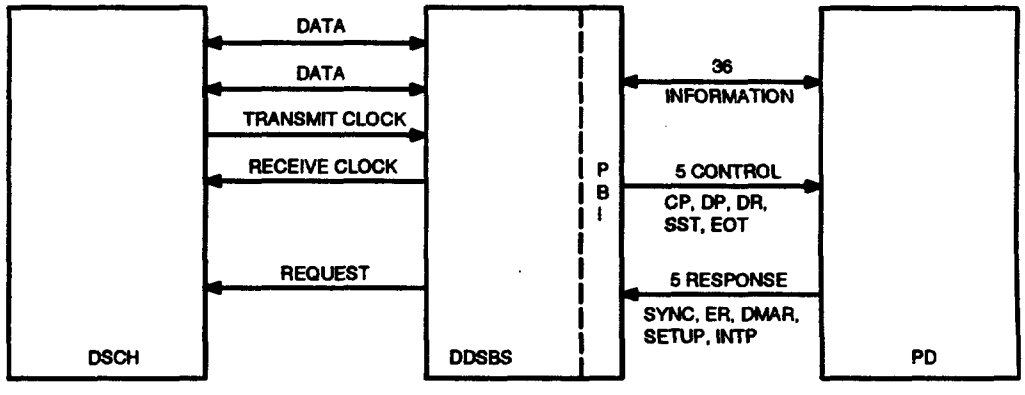


Figure 20. PBI Interface

7.07 The five response signals are as follows:

- SYNC—Upon reception of a control signal, the PD performs the prescribed operation and sets the SYNC signal. The SYNC signal is cleared in response to the removal of the control signal.
- ER—The PD sets the ER signal whenever an abnormal condition has been detected. Signal ER is checked by the DDSBS after it receives the SYNC response.
- INTP—When a PD requests 3B20D computer CC actions, the INTP signal is set to inform the CC of need.

- XFER—The PDs connected to the DSCH set the XFER signal to notify the DMAC that it is ready to transmit or receive another word or block during a data transfer. Also, this signal can be used to generate service request interrupts to the CC for PDs connected to the DSCHs equipped on the CCIO bus.
- Setup—A PD may initiate a DMAC setup by setting the setup signal. The DMAC will acknowledge the request by transmitting the data request (DR) control signal to retrieve the setup information. The setup signal can be used to generate service request for PDs connected to DSCHs equipped on the CCIO bus.

7.08 The DDSBS is a 2-port device and functions as a multipole, double-throw switch connecting the PD to the CCs via DSCH. The drivers and receivers interface the data bus from the DSCH to the DDSBS circuitry. The DDSBS receiving two streams of data along with the twin start code actually is used in two segments, the high-word and the low-word circuits.

7.09 The DDSBS uses a ROM-based sequencer and a request-generation sequencer. The ROM sequencer is used to control the DDSBS internal operations.

D. Theory of Operation

7.10 The DDSBS selector operation is essentially controlled by the command signal (maintenance mode). Bits 1 through 4 determine the operation. Bit 0 of the DDSBS command word is always a 1. This is used as a detection bit in the shift register. Bits 1 through 4 format and corresponding DDSBS maintenance operation is as follows:

Bit 4 Through 1	Operation
0000	Clear DDSBS error register
0011	Set DDSBS in maintenance mode
0101	Set DDSBS in operational mode
1001	Generate setup request
1010	Generate interrupt request
1011	Generate setup and interrupt request
1100	Generate transfer request
1101	Generate transfer and setup request
1110	Generate transfer and interrupt request
1111	Generate transfer, setup, and interrupt request.

7.11 The 16-bit status word for the DDSBS is used to report status information to the CC describing the DDSBS internal conditions. These bits are contained in the status register, and each bit is set by a response pertaining to a circuit operation (normal or abnormal). These bits are as follows:

Bit	Status
0	PD reported error
1	Overflow error
2	Sequencer error
3	Illegal DDSBS command
4	Maintenance flip-flop state
5	PD interrupt state
6	PD setup.

7.12 The input receivers and output drivers to the CC (via DSCH) are wired so that only one CC can be accessed at any given time. These circuits interface the bus connected to the DSCH with the data selectors and request generation sequencer.

7.13 The 36-bit data lead (two) are bidirectional and used to send and receive information between the DSCH and the DDSBS. The request signal lead, when set, notifies the CC that the DDSBS requires its functions. The transmit clock signal lead provides an internal timing for the DDSBS. The receive clock is used to gate timing information to the DSCH from the DDSBS.

7.14 A SYNC signal is generated by the PD in response to any control signal that has been properly received and acted upon by the PD. The SYNC is set to 1 to indicate that a control signal has been understood and data has been gated onto or from the data leads (signals are active low). The interrupt transfer, and setup leads are set to 1 at any time the PD, whether addressed or not, needs to interrupt the CC.

7.15 Data from the DSCH is gated into the DDSBS receivers and then into the data selectors. Data from the data selector is shifted into the 18-bit shift register. Data is checked for start code. Information is gated to the sequencer, which generates the signals to control the internal operations of the DDSBS. After the data is checked and is valid, the appropriate command is sent to the PD, and data transmission follows.

7.16 When the PD has information for the CC, it sets its request signal, and the CC responds with the appropriate command. Then the DDSBS sets up to receive the data from the PD. The data is inputted to the shift register, then shifted out to the data selector, and gated to the DSCH.

7.17 Interrupt information from the PD and also the DDSBS is gated into the DDSBS status register. This information is retrieved by the CC via a read status command. The data in the status register is shifted into the shift register, then shifted out into the data selector and gated to the DSCH.

7.18 The CC also generates the command to clear the status register, error circuits, and gate the DDSBS into a known state. Also, the CC generates the command to set the DDSBS into the maintenance mode for diagnostics.

E. Maintenance

7.19 Maintenance procedures for the DDSBS rely on built-in fault detection techniques and software diagnostic routines. The DDSBS contains no adjustments or test points for local monitoring. The circuit pack is a plug-in unit and is replaceable.

7.20 The DDSBS is set in the maintenance mode (MAINT flag set) and cleared by commands generated by the CC. When the MAINT flag is set, subsequent data and control signals generated by the CC will be received and executed by the DDSBS. These include data loop around and commands.

7.21 If a fault exists, the DDSBS is placed OOS; this also makes the PD OOS. If the fault is in the PD, it is placed OOS. When a unit is placed OOS, an appropriate TTY message is printed. However, if the fault exists in the CC or its dedicated peripheral units (such as the DSCH) a switch is made to the duplicate CC system.

8. Power

8.01 The DMAC, SCH, DSCH, and ACHI units each require +5 volts for operation. The +5 volts is supplied by DC-to-DC converters located in the power unit at the lower portion of the CU frame (Figure 2). Two to four (maximum) 244C or D converters (–48 volts to +5 volts) may be used depending on application. The +5 volts DC output from the 244 type converters are paralleled together (to increase current capability) and distributed to the ED-4C181-30 fuse unit for distribution to the channels.

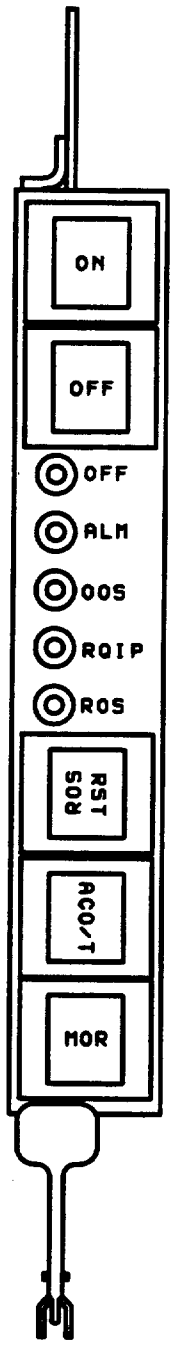
8.02 The DDSBS requires +5 volts DC for its operation. This voltage, power control, and fusing is provided by the frame in which the DDSBS is installed.

ABB1 Power Switch

8.03 The ABB1 (Figure 21) power switch provides the control (application and removal) for the frame power (Figure 22). The ABB1 is located in the MAS 0 unit in the CU frame (Figure 2). Five indicator lights on the front of the switch indicate the state of the unit being controlled. These lights are OFF, ALM, OOS, RQIP, and ROS. Five pushbutton switches provide power control. These are located on the front power panel and are ON, OFF, ROS/RST, ACO/T, and MOR. Input voltage requirements are –48 volts from he office supply and +5 volts from the 244 type DC-to-DC converters controlled by the switch.

8.04 Three-phased start signals are provided by the ABB1 to control the application sequence of logic power, memory power, and input/output bus power. The following functions may be performed by the craftperson:

- Sequentially supply or remove power
- Initiate system request to remove from service or restore to service the associated unit
- Test indicator lights on the power switch
- Retire a major office alarm generated at the associated unit.



LEGEND:

ACO/T	- ALARM CUT OFF/TEST
ALM	- ALARM
MOR	- MANUAL OVERRIDE
OOS	- OUT OF SERVICE
ROS	- REQUEST OUT OF SERVICE
ROS/RST	- REQUEST OUT OF SERVICE/ RESTORE TO SERVICE
RQIP	- REQUEST IN PROGRESS

Figure 21. ABB1 Power Switch, Front Panel

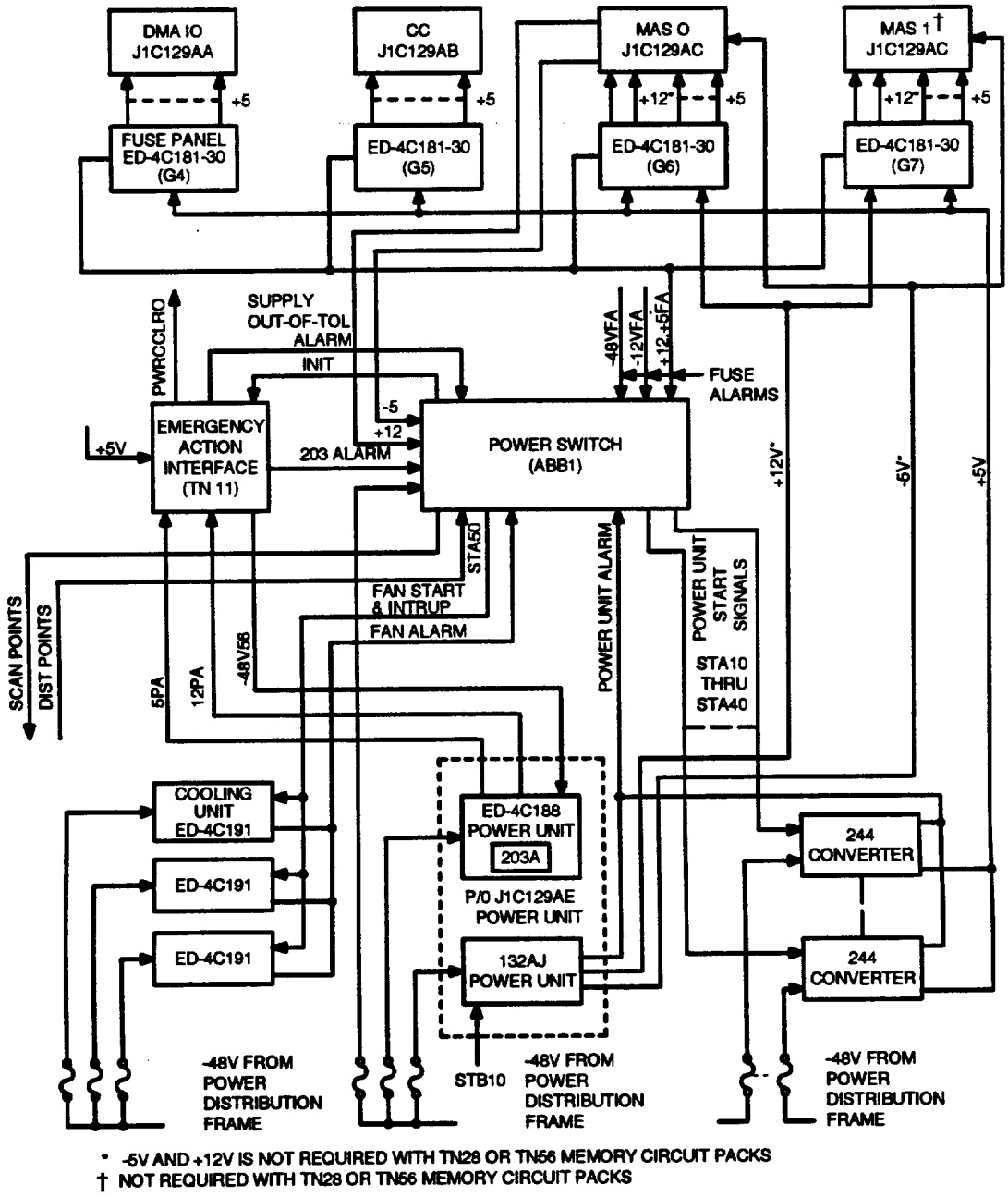


Figure 22. 3B20D Computer Control Unit Frame Power Distribution, Control, and Alarms

8.05 The ABB1 power switch controls are as follows:

(a) ***Lamps/Switches:*** Figure 21 shows a front view of the ABB1 power switch. The ON, OFF, and MOR are momentary pushbutton switches and ROS/RST and ACO/T are two position-latching switches. The five indicators are 549-type light emitting diodes (LEDs).

(b) ***ON Switch:*** Momentarily depressing the ON switch when the ACO/T switch is not in its retire alarm state initiates the power-up sequence. Depressing the ON switch when the ACO/T switch is in its retire-alarm state or when frame power is up causes no change in state of the power switch.

(c) ***OFF Switch:*** Momentarily depressing the OFF switch when the unit is in its out of service state initiates the power-down sequence. Depressing the OFF switch when the unit is in service or when power is off causes no change in state of the power switch.

(d) ***ROS/RST Switch:*** Depressing the ROS/RST switch to the ROS position requests the unit be taken OOS via scan point SCX and lights and the ROS LED. Depressing the ROS/RST switch to the RST position requests the unit be restored to service.

(e) ***ACO/T Switch:*** Depressing the ACO/T switch to the retire-alarm state tests all lamps on the power switch, provides an external lamp test signal, silences the office major alarm originated at the power switch, and extinguishes the ALM LED, if lit.

(f) ***MOR Switch:*** Simultaneously depressing the OFF and MOR switches defeats the interlock between the OFF switch and unit OOS state and initiates the power-down sequence.

(g) ***OFF LED:*** The red OFF lamp is lit when the unit is in its power-off state and extinguished when the unit is in its power-up state.

(h) ***ALM LED:*** The red ALM lamp lights to indicate the presence of power-related faults.

(i) ***OOS LED:*** The yellow OOS lamp is system activated via the OOS signal distribute point when the unit is marked out of service.

(j) ***RQIP LED:*** The green RQIP (request in progress) lamp lights to indicate that the system has received a request to take the unit out of service or restore it to service. This lamp, which is system-activated via the REQIP signal distribute point, flashes to indicate that the request has been denied.

(k) ***ROS LED:*** The green request out of service (ROS) lamp is lit when the ROS/RST switch is in its ROS state.

8.06 ***Scan, Alarm, and Signal Distribute Points:*** Three scan points (SCX, SCY, and BPP), two alarm points (MJ and PA), and two signal distribute points (OOS and RQIP) are provided. Each scan and alarm point consists of an isolated metallic contact. The active "1" state appears as a resistance of less than 200 megohms. The inactive "0" state appears as an open circuit. Each distribute point consists of an optoisolator input diode.

8.07 ***Scan and Alarm Points:*** Table C summarizes the scan and alarm point states. On automatic power off, the MJ scan point closes and remains closed until the ACO/T switch is depressed. When power is left up in the presence of a fault, the MJ scan point remains closed until either the fault is removed (PA scan point also goes inactive) or the ACO/T switch is depressed (PA scan point remains active).

Table C. Scan and Alarm Points

Condition	BPP	SCX	SCY	MJ	PA
Normal in service	1	0	0	0	0
Request out of service	1	1	0	0	0
Manual power off	0	1	1	0	0
Automatic power off	0	1	1	1	0
Power up with major fault present	1/0	0	1	1	1
Power up with minor fault present as supply out of tolerance	1	0	1	0	1

8.08 ***Signal Distribute Points:*** The active "1" state of the RQIP signal distribute point indicates a system software acknowledgment that a request for removal from service or restoral to service of the associated unit has been made. If the request is granted, the RQIP SD point will become inactive ("0" state). If it is denied, the RQIP SD point will intermittently flash under system control. The OOS signal distribute point becomes active when the unit has been taken out of service. The RQIP and OOS indicator lamps provide a visual indication of the state of the RQIP and OOS signal distribute points, respectively. Table D summarizes the signal distribute point states.

Table D. Signal Distribute Points

Condition	ROIP	OOS
Normal in service	0	0
Removal from service or restoral to service requested with disposition pending	1	0
Request denied	FLASH	0
Diagnostic failure after a restore-to-service request	FLASH	1
System grants out-of-service request	0	1

Power-Up Sequence

8.09 ***Start Signals:*** Power up is initiated by momentarily depressing the power ON switch. Control circuitry ensures that frame power is supplied in the proper sequence via three start signals and an initialization phase. In the power-off state, the initialization circuit, which starts the power-up sequence, is powered from a fused –48 V source through a normally open ON switch (momentary contact). Initialization signals enable +5 1V frame converters which power TTL sequence circuitry and initialize power control and alarm circuitry. This allows the power switch to be inserted with –48 V

present without the danger of enabling frame converters until the power ON switch is depressed. Start signals STA and STB are optoisolator outputs used to control converters associated with the power switch. Start signal STC is an open-collector relay driver that enables I/O bus power. On power up, logic power precedes memory power by approximately 1300 ms, and memory power precedes start signal by approximately 500 ms. The power-off LED is lit in the power-off state and does not extinguish until the power-up sequence is complete.

Power-Down Sequence

8.10 ***Normal Power Down:*** To prevent inadvertent removal of frame power, the power OFF switch (momentary contact) is interlocked with a system-granted out-of-service (OOS) signal. Depressing the power OFF switch causes no change in state of the circuit pack unless the OOS signal distribute point is active, in which case frame power is sequentially removed. On power down, the initialization signals and I/O bus power are removed approximately 500 ms before memory power is removed. The start signal is removed approximately 500 ms before logic power is removed. The power-off LED remains extinguished until the power-down sequence is complete.

8.11 ***Emergency Power Down:*** Craft personnel have the option of overriding the power OFF switch/OOS interlock under emergency conditions. Simultaneously depressing the power OFF and MOR (manual override) switches sequentially removes frame power as in the normal power-down case. Additionally, a separate backup timing circuit (approximately 1500 ms) will release the +5 V frame power in the event the power-down sequence circuit fails. With the release of +5 V power to the circuit pack, all start signals, and hence all frame power controlled by the power switch, will release.

8.12 Power should never be removed without consulting the maintenance document (TOP, AT&T 254-301-811). Also, power should be removed before replacing any circuit pack or unit in the CU frame.

9. References

9.01 The following documents contain information relevant to this practice.

PRACTICE	TITLE
AT&T 254-301-005	*AT&T 3B20D Model 1 Computer, General Description*
AT&T 254-301-010	*AT&T 3B20D Model 1 Computer, Central Control, Description and Theory of Operation*
AT&T 254-301-020	*AT&T 3B20D Model 1 Computer, Power Systems, Description and Theory of Operation*
AT&T 254-301-200	*AT&T 3B20D Model 1 Computer, Main Store, Description and Theory of Operation*
AT&T 254-301-811	*AT&T 3B20D Model 1 Computer, Task Oriented Practice (Routine)*

10. Glossary

10.01 A glossary of terms is provided to aid in the understanding of this practice.

Asynchronous—Functional units operate or interface without a fixed time relationship.

Autonomous—The device can perform its primary function without external assistance.

Bit Slicing—Functional grouping of bits of a register on two or more circuit packs.

Buffer—A storage device used to compensate for a difference in the rate of flow of information or time of occurrence of events when transmitting from one device to another. Normally a register.

Bus—One or more conductors over which information is transmitted from any of several sources to any of several destinations.

Channel—A communication path providing 1-way or 2-way transmission between two terminations.

Common Control System—A switching system that makes use of common equipment, is not part of a switching connection, but is used to establish a connection and then becomes available to establish other connections.

Control Unit—This consists of a central control, main store, and dedicated periphery. It is switched as one identity.

Data Link—Electronic equipment that permits automatic transmission of information in digital form.

Diagnostic—A program that functions to isolate a fault within the unit under test.

Flip-Flop—A device capable of assuming two stable states (set or clear), thereby storing a bit of information. It remains in either state until a signal changes it to the other state.

Interrupt—A signal generated by a device to notify the CC that the device requires attention.

Optoisolator—A coupling device consisting of a light sensor. Used for voltage and noise isolation between input and output while transferring the desired signal.

Shift Register—A digital storage circuit in which information is shifted from one flip-flop of a chain to the adjacent flip-flop on application of each clock pulse.

11. Acronyms and Abbreviations

11.01 The following is a list of acronyms and abbreviations used in this practice.

ACHI	Application Channel
ACO/T	Alarm Cutoff/Test
ALM	Alarm
CC	Central Control
CCIO	Central Control Input/Output
CCU	Central Control Unit
CH	Channel
CU	Central Unit
CSU	Cache Store Unit
CTRL	Controller
DDSBS	Duplex Dual Serial Bus Selector
DFC	Disk File Controller
DHA	Device Handlers
DIO	Direct Memory Access Input/Output
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller

DUP	Disk Unit Package
EIA	Electronic Industries Association
EOT	End Of Transfer
FIFO	First In First Out
I/O	Input/Output
IOP	Input/Output Processor
LED	Light Emitting Diode
MAS	Main Store
MASA	Main Store Array
MASM	Main Store Module
MCH	Maintenance Channel
MHD	Moving Head Disk
MOR	Manual Override
OOS	Out of Service
PC	Peripheral Controller
PCF	Peripheral Control Frame
PD	Power Distribution
PDF	Power Distribution Frame
PDU	Power Distribution Unit
PIC	Peripheral Interface Controller
PIO:	Programmed Input/Output
PSI	Peripheral System Interface
RAM	Random Access Memory
ROP	Receive Only Printer
ROM	Read Only Memory
ROS	Request Out Of Service
RMS	Root Mean Square
RQIP	Request In Progress
RSI	RS232 Interface
RST	Request Restore
SAR	Store Address

SCSI	Small Computer System Interface
SCH	Serial Channel
SDP	Signal Distribution Point
SMD	Storage Module Drive
TDC	Tape Data Controller
TTL	Transistor-Transistor Logic
TTYC	Teletypewriter Controller
WCA	Write Control/Address

How Are We Doing?

Document Title: AT&T 3B20D Model 1 Computer General Description

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