AT&T 3B20D Model 1 Computer Input/Output Processor Peripheral Controllers Description and Theory of Operation

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1. Overview

1.01 This practice provides a description and theory of operation of the peripheral controllers used in the input/output processor (IOP) and growth unit (Figure 1) of the computer. Each peripheral controller described is a plug-in circuit pack. The IOP description and theory of operation has been covered in AT&T 254-301-105.

1.02 This practice describes, in general terms, the physical and functional characteristics of the AT&T 3B20D Model 1 computer.

1.03 This practice is being reissued to include information about the Small Computer System Interface (SCSI) and the effects it has on the 3B20D Model 1 computer. Since this is a general revision, revision arrows used to denote significant changes have been omitted. The Equipment Test lists are not affected.

1.04 This practice contains no admonishments.

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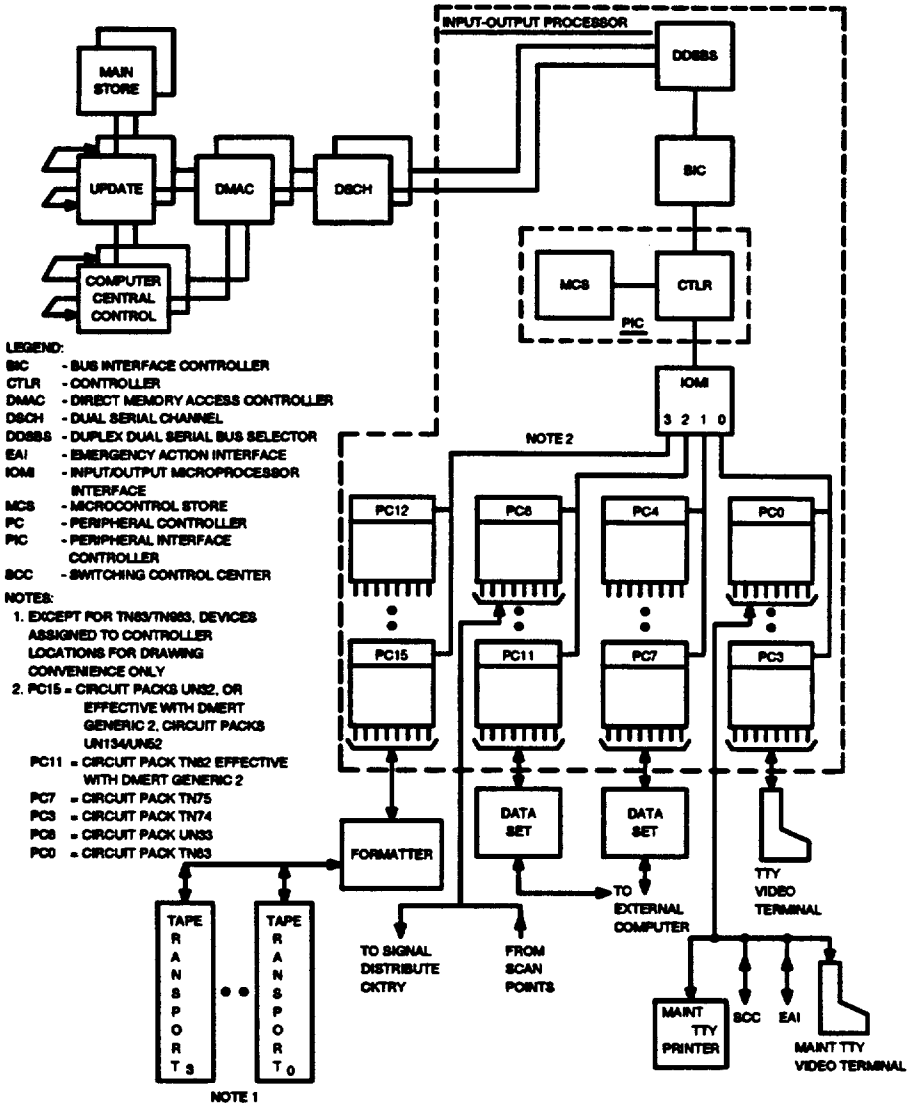

Figure 1. Input/Output 3B Computer Block Diagram and Interfaces

1.08 The peripheral controllers described in this practice are:

- UN32 tape controller
- UN134/UN52 tape controller
- UN33 scanner/signal distributor controller

- TN75 synchronous line controller
- TN74 asynchronous line controller
- TN82 direct user interface controller
- TN83/TN983 maintenance TTY peripheral controller.

A common address and data bus serves the controllers for communication to the computer. The type controllers used and their exact (plug-in) location is determined by the using organization.

2. Physical Description

2.01 Each of the peripheral controllers is identical in size and measures 8 inches high by 13 inches long. Mating connectors are mounted on 1-inch centers.

2.02 The peripheral controllers are plug-in assemblies of the IOP, which is in turn a part of the peripheral control frame (Figure 2). An IOP consists of a basic unit to which a growth unit may be added.

2.03 Each UN-type controller circuit pack contains a 300-pin female connector which mates with captive wire wrap terminals protruding through a backplane wiring board. Each TN-type contains a 200-pin female connector. Hardware common to each controller includes:

- Microprocessor
- Dual access memory
- Programmable read only memory (PROM).

3. Functional Description

3.01 Each controller circuit pack is assigned to a dedicated peripheral interface. The computer selects a controller and stores data in that controller to be transmitted to the peripheral device (Figure 1). The controller is configured with a microprocessor, timing, and related circuitry to transmit data to the peripheral device while generating the proper signal format. When a peripheral device transmits data for use by the computer, the controller stores the data and transmits it to the computer in the proper format.

3.02 Each of the 16 possible controllers interface with the UN25 circuit pack of the IOP. A common 9-bit parallel data bus and common 16-bit parallel address bus connect to each controller location. Data bus leads are bidirectional and the address bus transmits only to the controllers (Figure 3).

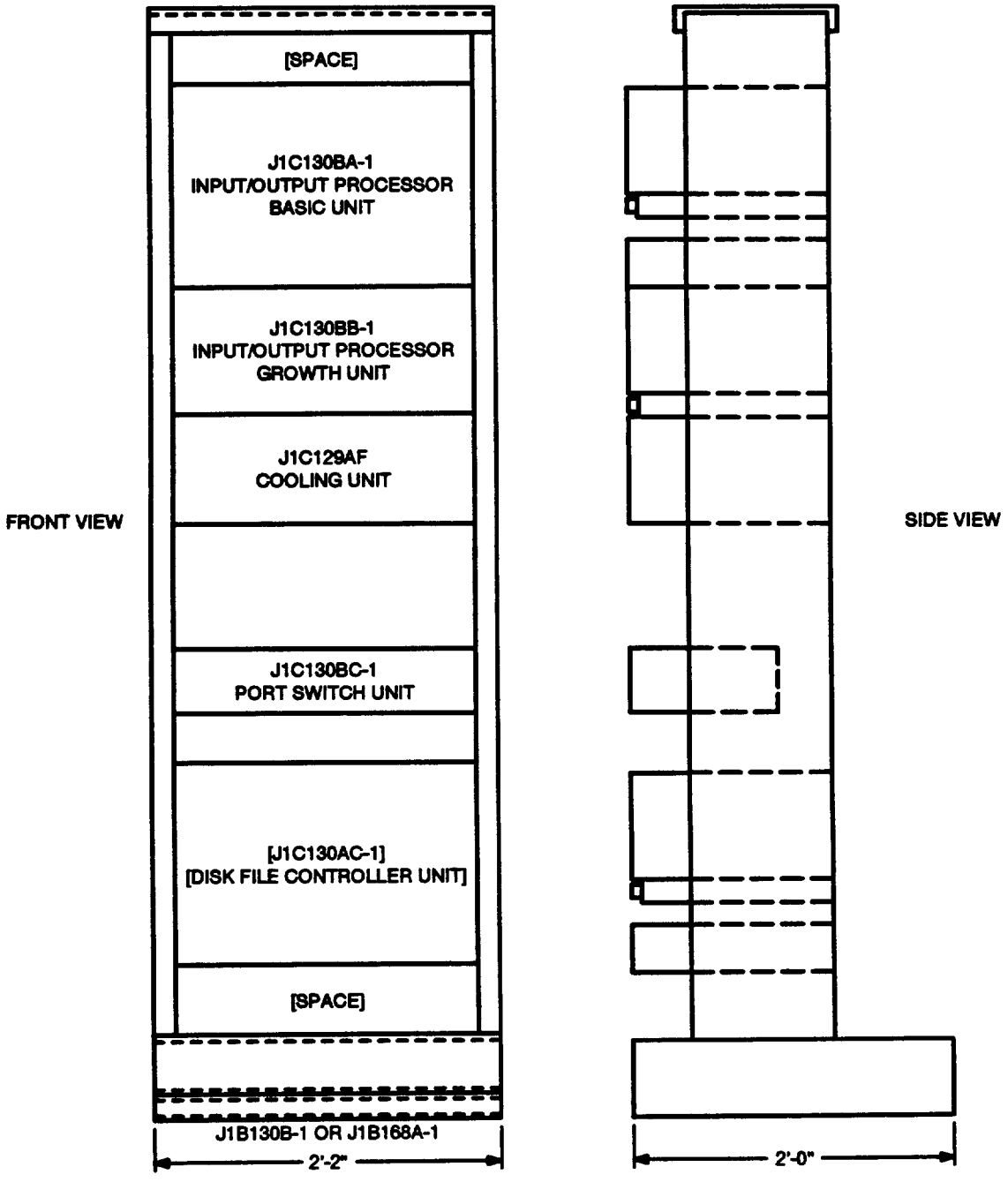

Figure 2. Peripheral Control Frame

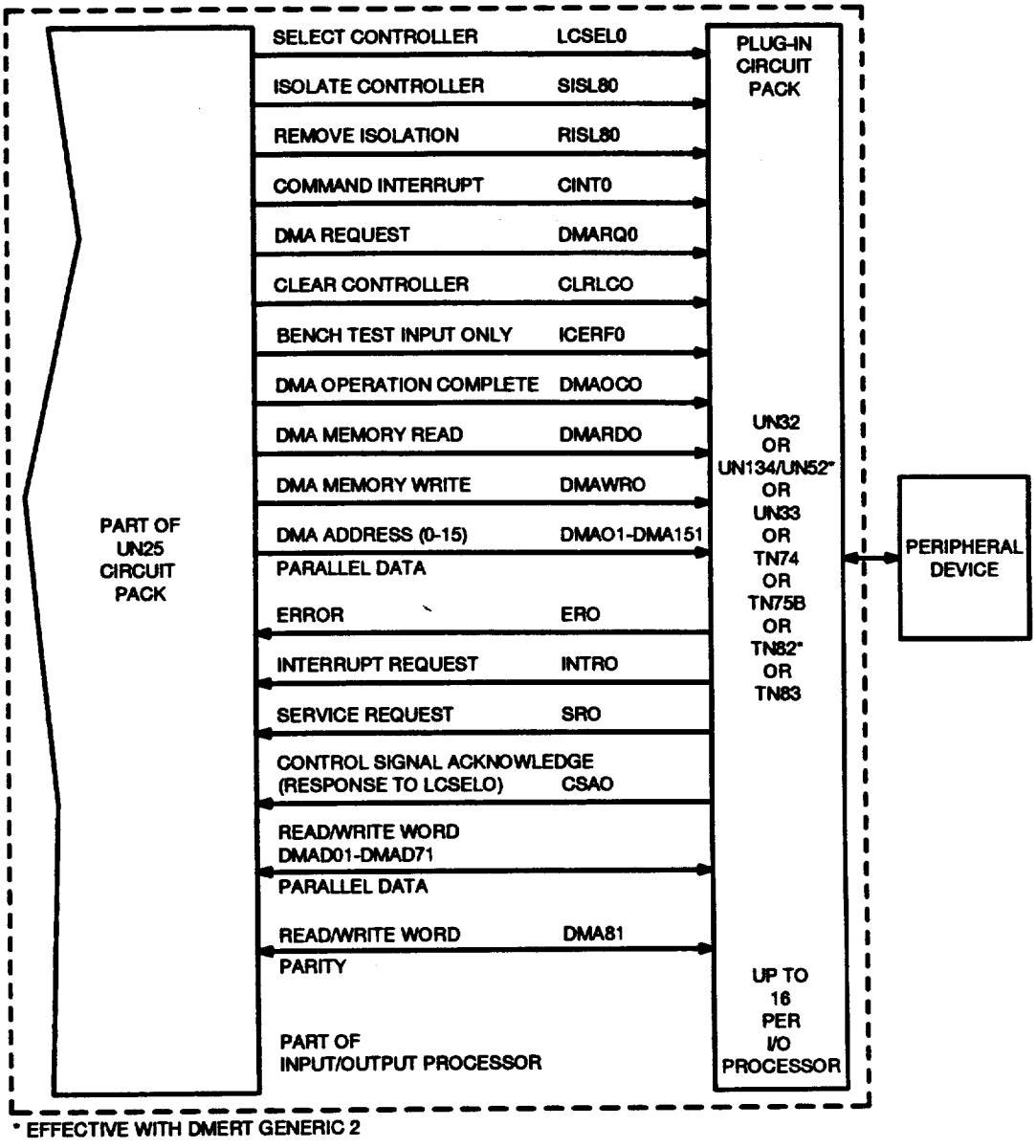

Figure 3. Peripheral Controllers to UN25 Interfaces

4. Theory of Operation

UN32 Tape Controller

4.01 Each UN32 contains circuitry for reading, writing, and controlling up to four 9-track tape transports (Figure 4). The peripheral interface controller (PIC) interface (via UN25) leads apply to each peripheral controller interface. Transistor-transistor logic (TTL) signal levels are used; with address and data leads being true (logic 1) with a positive voltage. The control, response, and status leads are true (logic 1) when low.

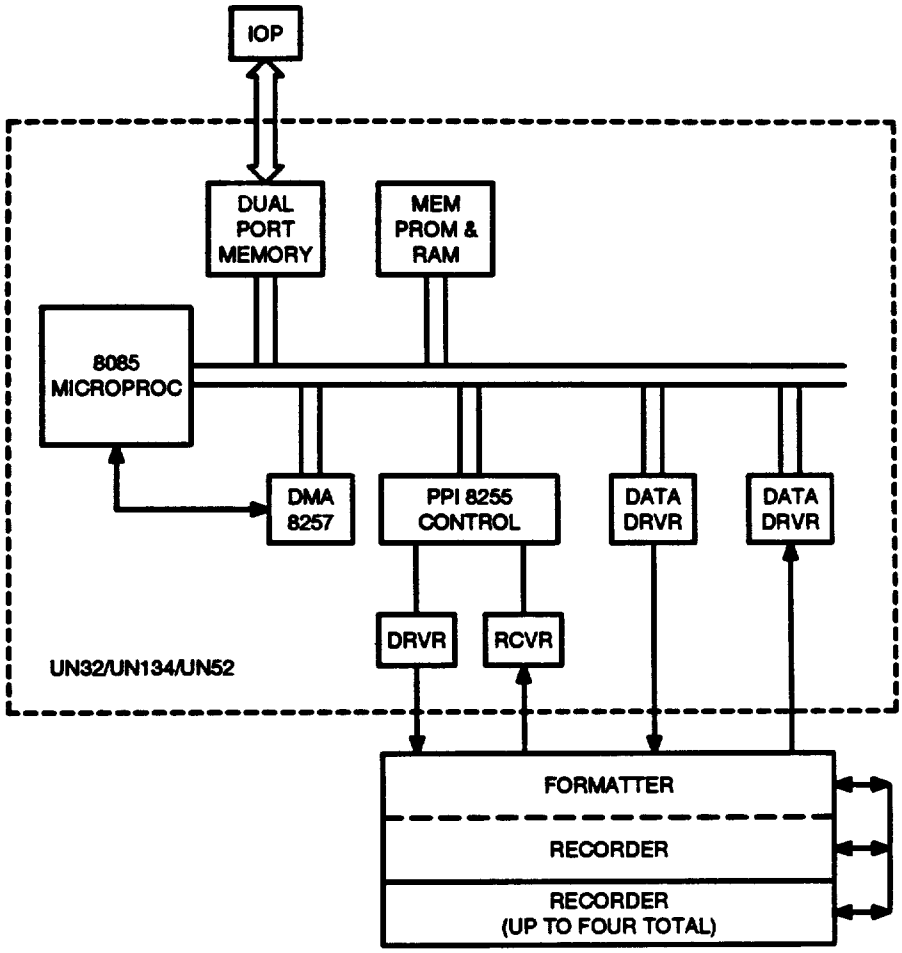

Figure 4. UN32 Block Diagram

A. UN32 Nine Track Tape Write

4.02 The computer requests access to the UN32 by active signals on leads LCSEL and DMARQ. The UN32 responds with control signal acknowledge which allows the PIC to write into the 4104 dual port memory. Twelve of the 16 address bits (from the PIC) accompany a byte of data (8 data and 1 parity bit) for a dual port memory write. A 64-bit command word (8 bytes) is sent to the UN32 for a pending job from the computer. This command contains the job to be done (read, write, seek, etc.), selection of tape transport, byte count of the block, if needed, and special options as required. When a write command is received the 8085 microprocessor addresses its random access memory (RAM) (WE®28A memory circuits) and extracts control data which in turn requests the PIC to move the data bytes into the 4104 dual port memory. When up to 2048 9-bit bytes have been stored, the microprocessor conditions the UN32 to KS-22091, L2 (formatter) interface leads to cause the selected tape transport to write 9-bit words. When writing a block of data, a byte of data is sent to the formatter every 25 microseconds. At a tape speed of 25 inches/second, data is written (or read) at a rate of 1600 bits/inch. All nine data bits are written simultaneously, one on each track with each track having a dedicated write head.

B. UN32 Differential Signal Input/Output

4.03 The UN32 formatter interface signal levels follow the RS422 format. Differential output drivers drive twisted pairs which are terminated by a 100-ohm resistor at the receiving end. Differential signals received from the formatter are also terminated by a 100-ohm resistor. These twisted pairs are labeled 0 and 1. When the 1 lead is positive by at least 0.25 volts relative to the 0 lead, then a logic 1 is defined to exist. Reversal of the relative polarity between the leads defines a logic 0.

C. Tape Transport Commands and Responses

4.04 Tape read, write, and control is accomplished only via the formatter, Table A lists the commands, responses, and data leads between the UN32 and formatter. Each entry in the table contains a pulse or level designation. A pulse signal is 1 microsecond in duration. A level designated signal last as long as necessary for the tape transport controller to perform associated functions.

Table A. UN32 Tape Transport Formatter Interface

Lead	Type Signal	Definition
WOP, WON thru W7P, W7N	Level	Differential data to tape formatter for writing on selected transport
WPP, WPN	Level	Write parity
ROP, RON thru R7P, R7N	Level	Differential data leads form formatter for data read from tape
RPP, RNP	Level	Read parity
LWDP, LWDN	Level	Signal to formatter for last word present
DENP, DENN	Level	Determines formatter write density
PARP, PARN	Level	Directs formatter data parity generator, odd or even
CERP, CERN	Pulse	Corrected data signal. Data corrected at formatter on read
HERP, HERN	Pulse	Hard error. Data error (read) not correctable at formatter
FMKP, FMKN	Pulse	File mark detected
FBYP, FBYN	Level	Formatter busy. Active when formatter receives GO form UN32/UN134*/UN52*
CCGP, CCGN	Level	Identity mark found indicating phase encoded (written) tape.
RDYP, RDYN	Level	Tape transport ready to read or write
ONLP, ONLN	Level	Tape transport is willing to accept commands and data
RWDP, RWDN	Level	Selected tape transport is rewinding
FPTP, FPTN	Level	Addressed file is protected against being overwritten
LPP, LPN	Level	Selected tape transport has reached the load point
EOTP, EOTN	Level	Selected tape transport has reached the end of tape point
NRZP, NRZN	Level	Formatter generated read/write mode status of phase encoded or nonreturn to-zero format
WSTRP, WSTRN	Level	Write strobe from formatter when data in write bus has been gated into formatter
RSTRP, RSTRN	Level	Read strobe from formatter that data is on read bus for UN32/UN134*/UN52* read
TADOP, TADON	Level	Two address bits to formatter for decoding to select one-of-four tape transports
REVP, REVN	Level	Command to formatter to direct tape transport to reverse tape direction
WRTP, WRTN	Level	Command to formatter to read or write tape
WFMP, WFMN	Level	Command to write file mark on selected tape
FADP, FADN	Level	Formatter selected signal. Only FO type formatter used with 3B UN32/UN134*/UN52* generated signal to enable formatter
GOP, GON	Pulse	GO signal to formatter
OFLP, OFLN	Pulse	Directs formatter to put selected tape transport in off-line state. Formatter is then able to accept commands.
REWP, REWN	Pulse	Causes selected on-line tape transport to rewind to load point. Does not cause the formatter to go busy.

*Effective with DMERT Generic 2.

UN134/UN52 Tape Controllers

4.05 Effective with DMERT generic 2, the UN134 tape controller replaces the UN32 tape controller. Optionally, the UN52 high speed tape controller is available for use instead of the UN134. The UN134 and UN52 each contain circuitry for reading, writing, and controlling up to four 9-track tape transports (Figure 4). The PIC interface leads apply to each PIC (via UN25). The TTL signal levels are used. Address and data leads are true (logic 1) with a positive voltage. The control, response, and status leads are true (logic 1) when low.

A. Nine-Track Tape Write

4.06 The computer requests access to the UN134/UN52 by active signals on leads LCSEL and DMARQ. The UN134/UN52 responds with a control signal acknowledge which allows the peripheral interface controller to write into the 4104/61A dual port memory. Twelve of the 16 address bits (from the PIC) accompany a byte of data (8 data bits and 1 parity bit) for a dual port memory write. A 64-bit command word (8 bytes) is sent to the UN134/UN52 for a pending job from the computer. This command contains the job to be done (read, write, seek, etc); selection of tape transport; byte count of the block, if needed; and special options as required. When a write command is received the 8085 microprocessor addresses its RAM and extracts control data which in turn requests the PIC to move the data bytes into the 4104/61A dual port memory. When up to 2048 (6144 with UN52) 9-bit bytes have been stored, the microprocessor causes the selected tape transport to write 9-bit words. When writing a block of data, a byte of data is sent to the formatter every 25 inches per second and data is written (or read) at a rate of 1600 bytes per inch. All nine data bits are written simultaneously, one on each track with each track having a dedicated write head.

B. Input/Output Signal Interfacing

4.07 The UN134-to-formatter interface signal levels follow the Electronic Industries Association (EIA) standard RS422 format. Differential output drivers drive twisted pairs which are terminated by a 100-ohm resistor at the receiving end. Differential signals received from the formatter are also terminated by a 100-ohm resistor. These twisted pairs are labeled 0 and 1. When the 1 lead is positive by at least 0.25 volt relative to the 0 lead, then a logic 1 is defined to exist. Reversal of the relative polarity between the leads defines a logic 0. The interface between the UN52 and the formatter consists of 25 input and 25 output TTL signals with corresponding ground leads.

C. Tape Transport Commands and Responses

4.08 Tape read, write, and control are accomplished only via the formatter. Table A lists the command, response, and data leads between the UN134 and formatter. The leads between the UN52 and the formatter drop the P, N paired notation and instead become signal leads with a paired ground return. Each entry in the table contains a pulse or level designation. A pulse signal is 1 microsecond in duration. A

level-designated signal lasts as long as necessary for the tape transport-controller to perform associated functions.

UN33 Computer Scanner/Signal Distributor Controller

4.09 The UN33 computer scanner/signal distributor controller CP (UN33) consists of circuitry for monitoring 48 scan points and controlling 32 distribute points as shown in Figure 5. A scan point is considered to be a set of open pair leads connected to a monitored current source on the UN33. Each pair (used) is connected to a predefined circuit in the computer where the circuit either shorts the open pair or allows them to remain open. A signal distribute point is considered to be a pair of wires permanently connected to a load (controlled point) in the computer. The UN33 under the direction of the computer determines when current is applied, including duration and repetition rate.

4.10 Each scan point is examined every 48 milliseconds. Scan points are numbered 00 through 47. For a scan point to be considered in a changed state, it must remain in its new state (open or closed) for two successive scan cycles. Only then is the status of that scan point changed in the dual port memory of the UN33. When a scan point is closed, current flows in its assigned location in a 6 by 8 matrix.

4.11 Each scan point has two dedicated bytes in the dual port memory. The first byte contains the scan point address, scan point state bit, and last a look bit. The second byte contains an activity bit which determines whether or not scan point changes are to be reported.

4.12 The 32 distribute points are activated by commands from the computer. Only one distribute point is made active or deactivated at a time, however more than one may be active simultaneously. A distribute point, when used, is connected to dedicated circuitry external to the UN33. The computer may command (direct) up to four states for a distribute point:

- Set operate
- Clear
- Flash continuously
- Flash for 8 seconds after which it terminates in an off state.

Flashing is at a 1-Hz rate with a 50 percent duty cycle.

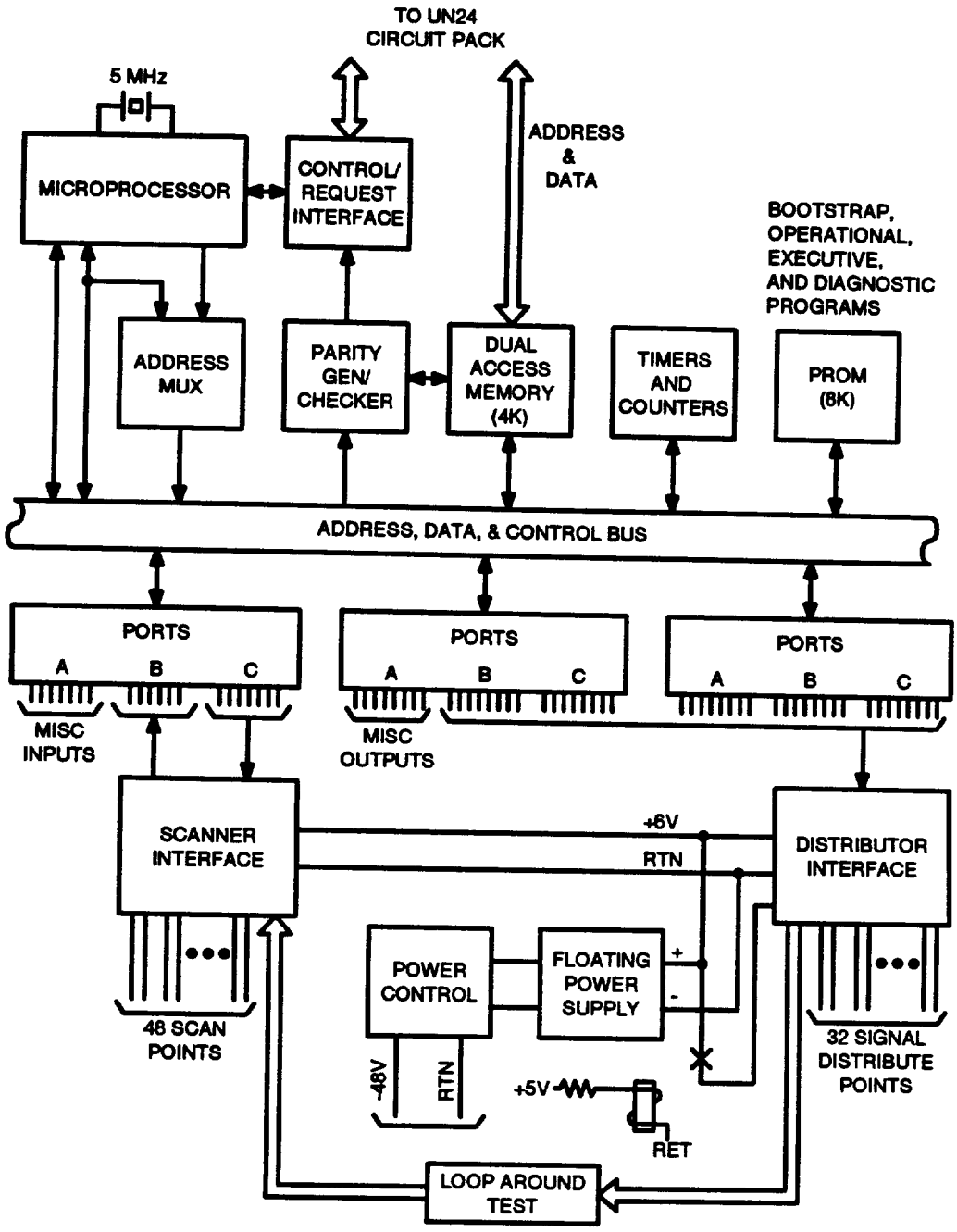

Figure 5. UN33 Block Diagram

4.13 Each of the 32 distribute points has a dedicated byte in the dual access memory. The 32 bytes are called a "flash" table. Contained in the byte is:

- A 2-bit code which determines one of four possible states
- Output of flash rate counter
- Eight second timer output.

4.14 The UN33 reads the scan point map on command from the computer. The UN33 does not contain a 16K dynamic RAM used in other controllers. The UN33 PROM does however contain program data normally found in the 16K memories.

TN75C Synchronous Line Controller

4.15 The TN75C synchronous line controller is the controller interface for the computer to communicate with up to two external data links. The TN75C interfaces with a data set which has compatible transmission rates (Figure 6). Table B lists the automatic dial out interface leads.

4.16 Data words, 8 bits and a parity bit, are received via the parallel data bus from the UN25. Data bytes are gated into the 8K word by 9-bit wide dual access memory (when access has been granted to the TN75C). Should the self-contained microprocessor be busy, access is denied. The TN75C receives command words from the central control which include the number of data bytes to transfer. When the computer reads data from the dual port memory, a memory read command is received by the TN75 and processed by the microprocessor.

4.17 After the dual port memory has been written, the microprocessor selects output channel 0 or 1 and empties the dual port memory by transmitting out one word at a time in serial format. The format change is accomplished in the output circuitry. Serial data words are received by the TN75 from its computer interface. A protocol chip on the TN75 converts the incoming data format from serial to parallel. The parallel (received) data is then written in the dual access memory. The computer then gains access to the dual access memory and reads the data one byte at a time.

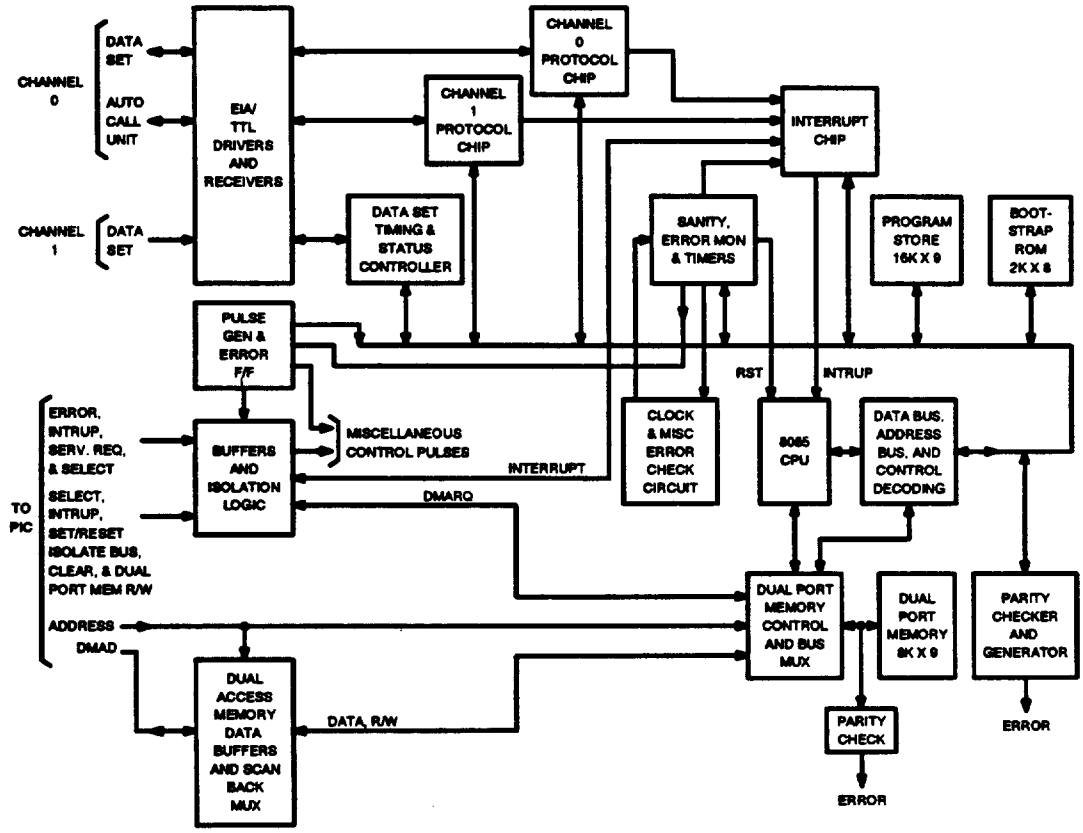

Figure 6. TN75C Block Diagram

Table B. TN75C to External Computer Interface

Terminal Nomenclature		Input or Output	Definition
Channel 0	Channel 1		
RLS0	RL1S0	Output	Remote loop back
LLS0	LL1S0	Output	Local loop back
RS0S0	RS1S0	Output	Request to send
TR0S0	TR1S0	Output	Terminal ready
	1S1S0	Output	In service
NEG0S1	NEG1S1	Output	Constant logic 1 (negative voltage)
POS0S0	POS1S1	Output	Constant Logic 0 (positive voltage)
SD0S1	SD1S1	Output	Transmitted data (-5V = 1, +5V = 0)
ASD0S1 ASD0R0	ASD1S1 ASD1R0	Output Output	Balanced output transmitted data (+5V logic)
RT0R1 RT0S0	RT1R1 RD1S1	Input Input	Receiving timing pulse for incoming data
RD0R0 RD0S1	RD1R0 RD1S1	Input Input	Received data
ST0R0 ST0S0	ST1R1 ST1S0	Input Input	Send timing pulses, used by TN75B when transmitting data
SQ0S0	SQ1S0	Input	Signal quality
DM0S0 DM0R1	DM1S0 DM1R1	Input Input	Data mode
CS0S0 CS0R1	CS1S0 CS1R1	Input Input	Clear to send
RR0S0 RR0R1	RR1S0 RR1R1	Input Input	Receiver ready
DL0S0		Input	Automatic dialing can not complete date line occupied
SB0S0	-	Input	Standby indicator
SS0S0	-	Output	Select standby
Automatic Call Unit Interface			
COSS0		Input	Status of automatic call unit and digits received call origination status
PWIS0		Input	Power indicator form automatic call unit
PNDS0		Input	Present next digit
NB8S1 NB4S1 NB2S1 NB1S1		Output Output Output Output	Binary coded digits to automatic call unit (numbers to be dialed)
DPRS0		Output	Digits present signal to automatic call unit
CRQS0		Output	Call request. 3B computer wants to make call via automatic call unit
ACRS0		Input	Abandon call and retry
TMOS0	TM1S0	Input	Test mode

TN74 Asynchronous Line Controller

4.18 The TN74 asynchronous line controller has the capability to control up to four peripheral devices such as teletypewriters, line printer, and data sets (Figure 7). Interfacing devices must adhere to the RS232 signal interface.

4.19 The TN74 contains a microprocessor which controls the activities of transferring transmit and receive data between the computer and peripheral devices. Data to be transmitted from the computer to the TTY is written into the 4K by 9-bit word dual port memory. A dual port memory controller determines access to that memory. When the dual access memory has stored all the bytes of a message, the microprocessor causes each byte (minus parity bit) to be placed on a common data bus which interfaces with two universal asynchronous receiver transmitters (UART 0 or 1). The selected UART converts the parallel word into an American Standard Code for Information Exchange (ASCII) character, which may be programmed to include a parity bit, with one start and two stop bits. The ASCII character is transmitted serially as TTL level pulses to the port interface logic circuitry. The port interface logic circuitry transmits the serial data bits as a plus and minus 12-volt signal. A logic 1 is minus (-) 12 volts, with plus (+) 12 volts being a logic 0 (EIA RS232 standard). When not transmitting data, the output consists of logic 1 (marking) state.

4.20 Receiving ASCII characters from the TTY is the reverse of writing in that the port interface circuitry converts EIA voltage levels to TTL levels and feeds the selected UART. The UART converts the series bit stream to a parallel byte for storage in the dual port memory. A parity generator adds a parity bit when necessary. The TN74 then informs the computer that data is ready to be read.

4.21 Channels 0 and 1 each have a dedicated control and response interface for two ports. With the exception of data, all other interface leads to the TTY are via the selected channel and port. These control and response leads also use plus and minus 12 volt logic levels. Table C contains a list of interface leads between the TN74 and peripheral devices.

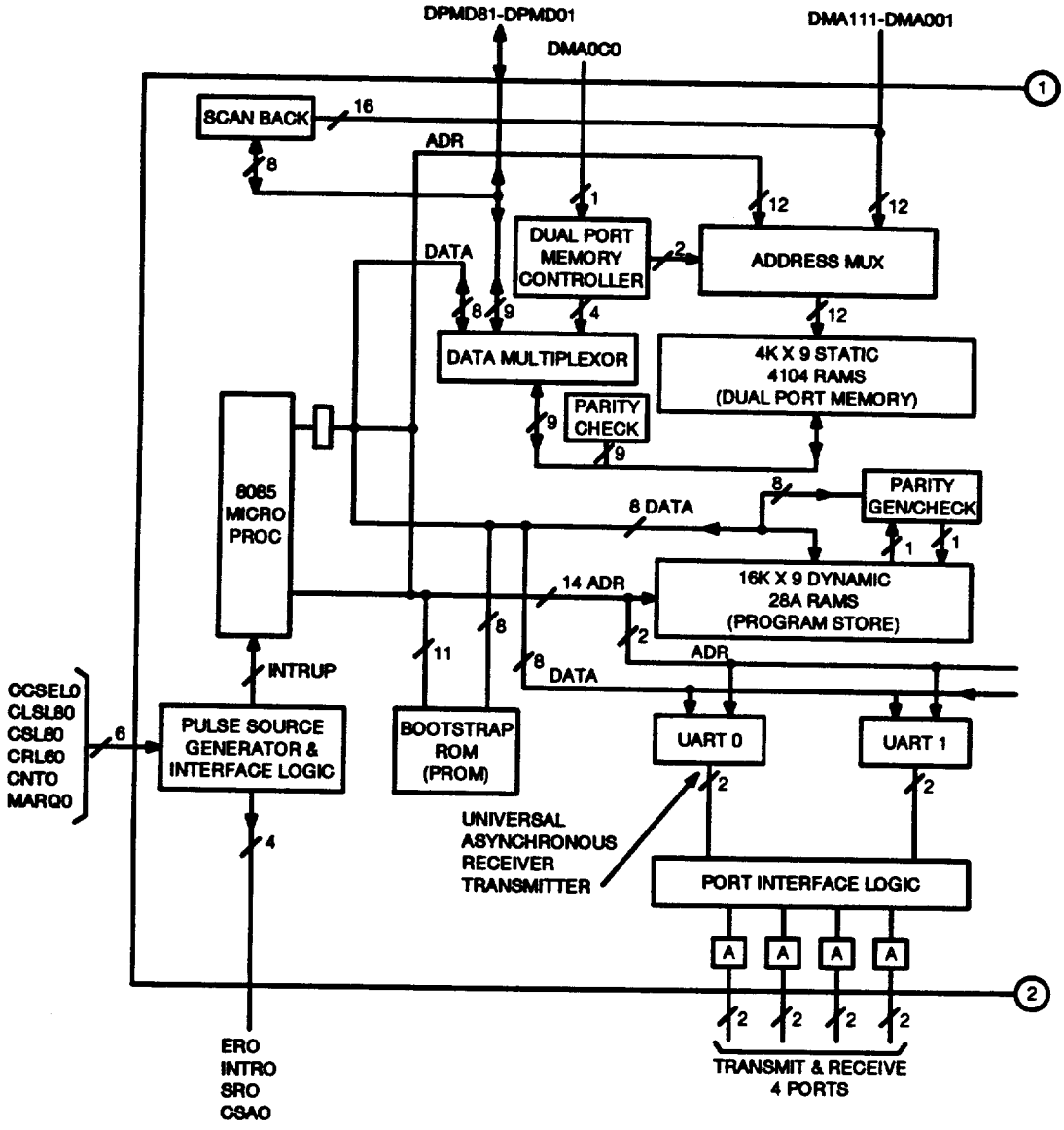

Figure 7. TN74 Block Diagram (Sheet 1 of 2)

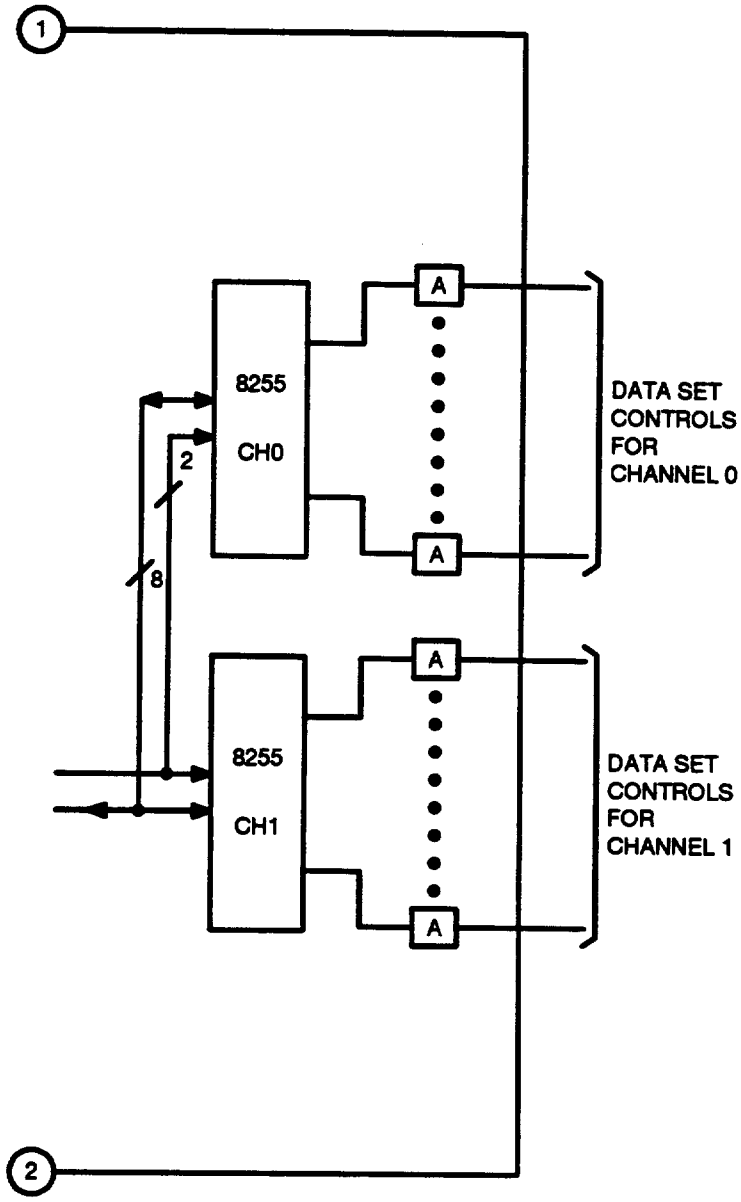

Figure 7. TN74 Block Diagram (Sheet 2 of 2)

Table C. TN74 Inputs and Outputs

Terminal Nomenclature				Input or Output	Definition
Channel 0		Channel 1			
Port 0	Port 1	Port 0	Port 1		
BBRC00P1	BBRC01P1	BBRC10P1	BBRC11P1	Input	Data input
RST0PP0	RST01P0	RST10P0	RST11P0	Output	Request to send
DTR00P0	DTR01P0	DTR10P0	DTR11P0	Output	Data terminal ready
BA00P1	BA01P1	BA10P1	BA11P1	Output	Transmitted data
CCR00P0	CCR01P0	CCR10P0	CCR11P0	Input	Data set ready
CBR00P0	CBR01P0	CBR10P0	CBR11P0	Input	Clear to send
CER00P0	CER01P0	CER10P0	CER11P0	Input	Ring indicator
CFR00P0	CFR01P0	CFR10P0	CFR11P0	Input	Carrier present
SCFR00P0	SCFR01P0	SCFR10P0	SCFR11P0	Input	Secondary carrier
SCA00P0	SCA01P0	SCA10P0	SCA11P0	Output	Secondary control
EPULL000	EPULL010	EPULL100	EPULL110	Output	+12 Volt

TN82 Direct User Interface Controller

4.22 The TN82 is a protocol standard BX.25 compatible controller. The TN82 provides a single, high-speed, synchronous data link channel for the IOP. It can operate one full duplex data link channel at a maximum data transfer rate of 56K bits per second.

4.23 The TN82 is controlled locally by a 16-bit 8086 microprocessor which operates with five 2732A erasable programmable read-only memories (EPROMs) totaling 16K bytes of memory for all operational and diagnostic firmware. Eighteen 4104/61A RAMs provide 8K bytes of static read/write memory as dual access memory. This memory is accessed via the IOMI bus, by the local 9517 direct memory access controller (DMAC) as 8-bit memory, or by the 8086 microprocessor as 16-bit memory (Figure 8).

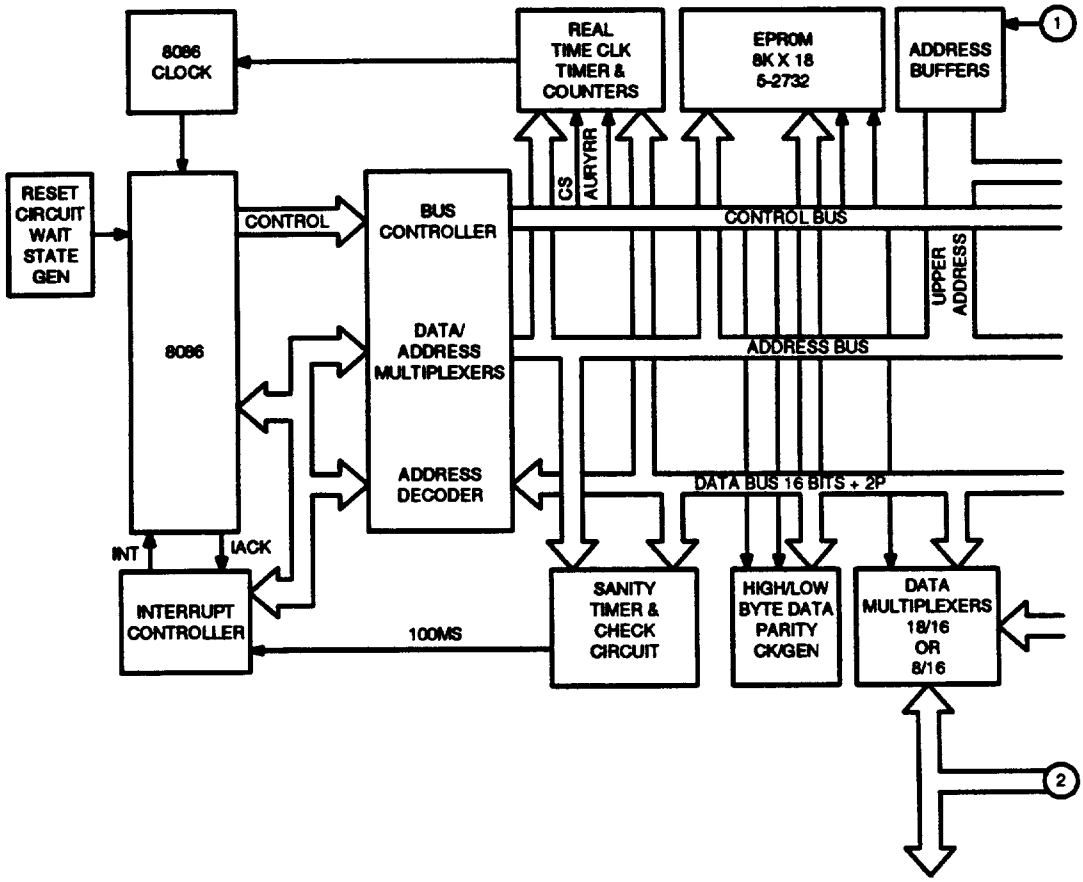

Figure 8. TN82 Block Diagram (Sheet 1 of 2)

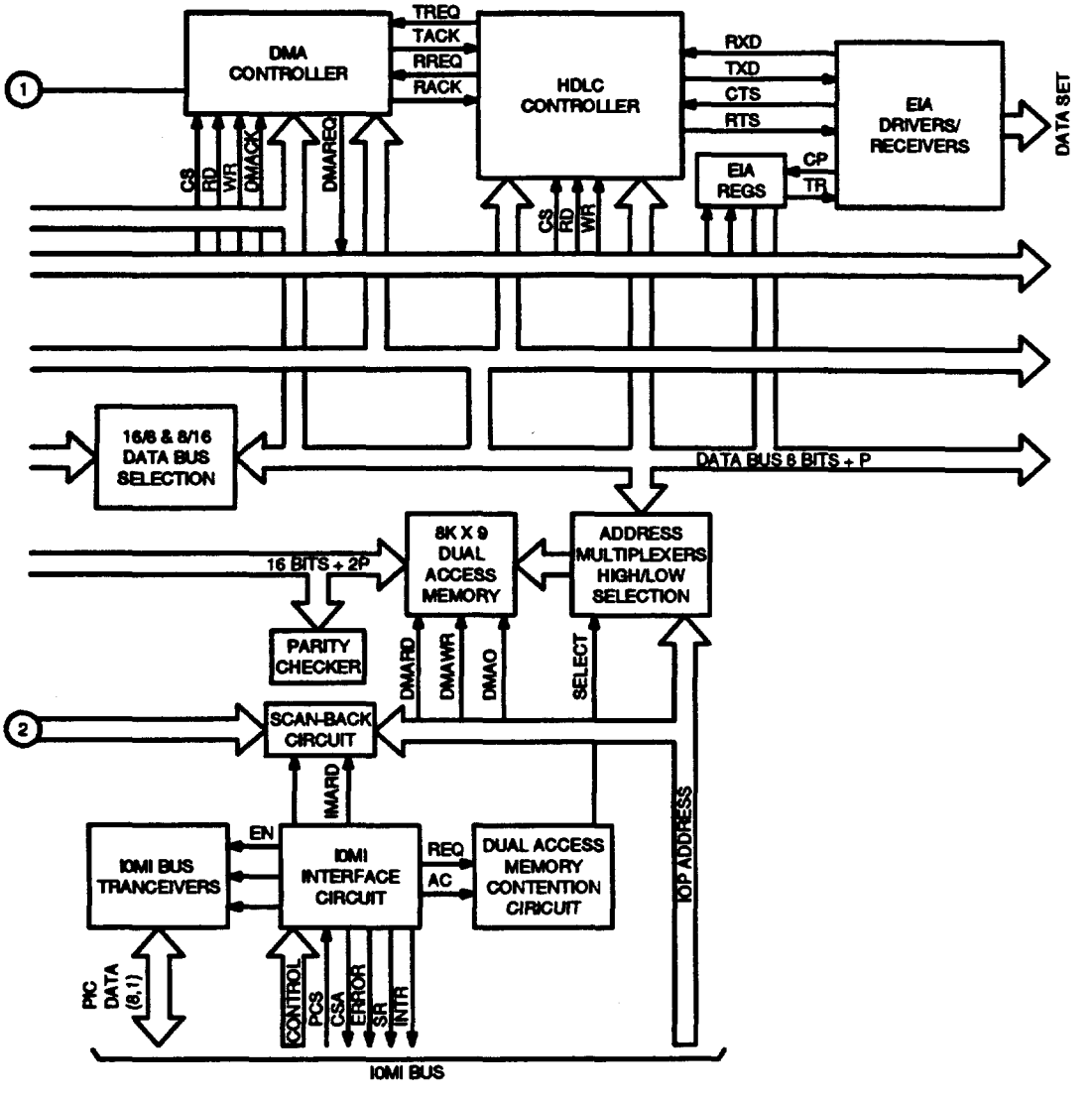

Figure 8. TN82 Block Diagram (Sheet 2 of 2)

4.24 The TN82 direct memory access (DMA) controller provides four independent DMA channels. Two of these channels are used by the 8273 high-level data link control protocol controller, while the other two channels are unused. The high-level data link control protocol controller passes transmitted and received data via DMA operations. Two signaling interfaces are provided on the TN82. The first is a Consultative Committee International Telephone and Telegraph (CCITT) V.35 interface, which allows up to 56K bits per second of data transfer. The second is a standard RS449/423 interface, which allows up to 19.2K bits per second of data transfer. A 1-bit output port on the high-level data link control protocol controller determines which interface is used. Table D provides lead designations and descriptions for the interface between the TN82 and peripheral devices.

4.25 Interfacing between the computer and the TN82 controller is different from that between the processor and other controllers such as the TN74 and TN75. The high rate of data transfer allowed by the TN82 necessitates more direct interfacing between the peripheral controller and the application process requesting the transfer of data. This interface is referred to as the direct user interface (DUI). The concept that makes DUI possible is a common area of application memory directly accessible by the application process and the peripheral controller. This memory is referred to as the DUI table and is used for passing commands and status information between the TN82 and the application process.

4.26 A summary of the sequence of events for successful DUI setup and data transfer follows this paragraph. A successful system initialization is assumed to have already occurred.

4.27 The application process initiates the DUI setup by sending an "open communication" message to the DUI handler. The DUI handler links the peripheral controller subdevice to the application process. (The peripheral controller subdevice is dedicated to the application process until the application process breaks the link.) The application process initializes the DUI table when notified of the established link. The application process then sends a "start" message to the DUI handler, causing the DUI handler to assign DMA jobs. The DUI handler sends restore parameters to the peripheral controller, causing the peripheral controller to poll the DUI table specified in the restore parameters. At this point, the peripheral controller also sets up the BX.25 protocol link. After the DUI handler receives a "connect" report, it assigns any additional DMA jobs and sends an "acknowledge DUI start" message to the application process. When both messages have been received, the application process has full DUI capability. The peripheral controller is active in the DUI mode and carries out all input/output and accompanying instructions in the DUI table.

Table D. TN82 Inputs and Outputs

Lead	Input or Output	Definition
CSR1	Input	Clear to send return (EIA)
CSS0	Input	Clear to send signal (EIA)
DMR1	Input	Data mode return (EIA)
DMS0	Input	Data mode signal (EIA)
RC	Input	Return common (EIA)
RDA	Input	Receive data A (V35)
RDB	Input	Receive data B (V35)
RDR0	Input	Receive data return (EIA)
RDS1	Input	Receive data signal (EIA)
RRR1	Input	Receive ready return (EIA)
RRS0	Input	Receive ready signal (EIA)
RTR1	Input	Receive timing return (EIA)
RTS0	Input	Receive timing signal (EIA)
SCRA	Input	Receive timing A (V35)
SCRB	Input	Receive timing B (V35)
SCTA	Input	Receive timing A (V35)
SCTB	Input	Receive timing B (V35)
STR1	Input	Send timing return (EIA)
STS0	Input	Send timing signal (EIA)
ASDR0	Output	Send data BAL return (EIA)
ASDS0	Output	Send data BAL signal (EIA)
POS1	Output	Positive pull-up
RLS0	Output	Remote loop-back (EIA)
RSS0	Output	Request to send (EIA)
SDA	Output	Send data A (V35)
SDB	Output	Send data B (V35)
SDS1	Output	Send data signal (EIA)
TRS0	Output	Terminal ready (EIA)

TN83/TN983 Maintenance TTY Peripheral Controller

4.28 The maintenance TTY peripheral controller (TN83/TN983) shares a common interface to the UN25, with the other peripheral controllers of an IOP (Figure 1 and Figure 3). Effective with generic 3 the TN983 is optionally available and extends the capabilities of the TN83. The new TN983 peripheral controller improves the interface with the craft handler, provides consistent emergency action interface settings, and controller enhancements. One enhancement is a user prompt display which indicates the readiness of the computer to accept input. The TN983 also makes available a 48 line display and provides a second keystroke requirement. This second keystroke requirement prevents drastic results that could occur from a single accidental keystroke. The TN983 hardware for generic 3 must be supported by other subsystems for generic 3 which include the assignment of new database values to identify the hardware and diagnostics to test the hardware. The TN83/TN983 (Figure 9) interfaces with the following:

- Computer central control via IOP
- Emergency action interface (TN11) CPs
- Maintenance TTY (video terminal)
- Maintenance TTY printer
- Switching control center (SCC)
- TN71 circuit pack in IOP.

The TN83/TN983 is arbitrarily assigned to the first (00) controller location in an IOP used in a duplex computer configuration.

4.29 The primary use of the TN83/TN983 is for manual intervention and control of the computer central control and peripherals. The maintenance TTY interfaces with the TN83/TN983 (Table E) using ASCII (7 bit +1 parity) code and RS232 electrical interface (±12V logic). The maintenance TTY printer also interfaces to the TN83/TN983 using ASCII code and RS232 electrical interface.

4.30 When the TN83/TN983 (computer) connects to a SCC, BX.25 protocol and RS232 electrical interface are employed. The RS232 interface connects to a data set for transmission to the SCC.

4.31 Two emergency action interface ports are provided, with each output dedicated to a central control when used in a duplex configuration. These outputs employ and RS422 (balanced 5 volt) electrical interface. The TN71 interfaces employ TTL.

4.32 A microprocessor (8085/8085A-2) controls the operation of the TN83/TN983. Four 4K by 8-bit erasable programmable memories contain the program for the operation of the TN83/TN983. Parity is not checked when reading the programmable memory. The nine 16K by 1-bit dynamic memory modules (WE28A) contain general purpose, storage setup information, and temporary data. The WE28A memory modules

are dynamic random access devices, which means that the data must be refreshed periodically. On board (TN83/TN983) circuitry contains an address counter and refresh timer. Random access means that any address may be written or read without regard to the previous address. When the central control unit reads the dynamic RAM, an error signal is generated when odd parity is not found. When writing the dynamic RAM, parity is generated but not checked.

4.33 The dual port memory consists of nine 4K by 1-bit (K=1024), static RAM devices. The central control has access to the TN83/TN983 via the dual port memory. For instance, during initialization the central control writes the dynamic RAM via the dual port memory. An internal data bus under control of the central processor unit (CPU) is then used to transfer data to the dynamic memory. Data and instructions to a peripheral device are written in dual port memory. The memory is then read and transmitted to the addressed interface circuit, such as the maintenance teletype.

4.34 When the CPU reads the dual port memory, data parity is checked and an error signal is generated when odd parity is not found. During a write by CPU to the dual port memory, odd parity is generated on the TN83/TN983, the word written (8 data and 1 parity), and parity checked. An error signal is generated when odd parity is not found. When the central control via the peripheral interface controller reads or writes the dual port memory, parity is checked and an error signal generated when odd parity is not found.

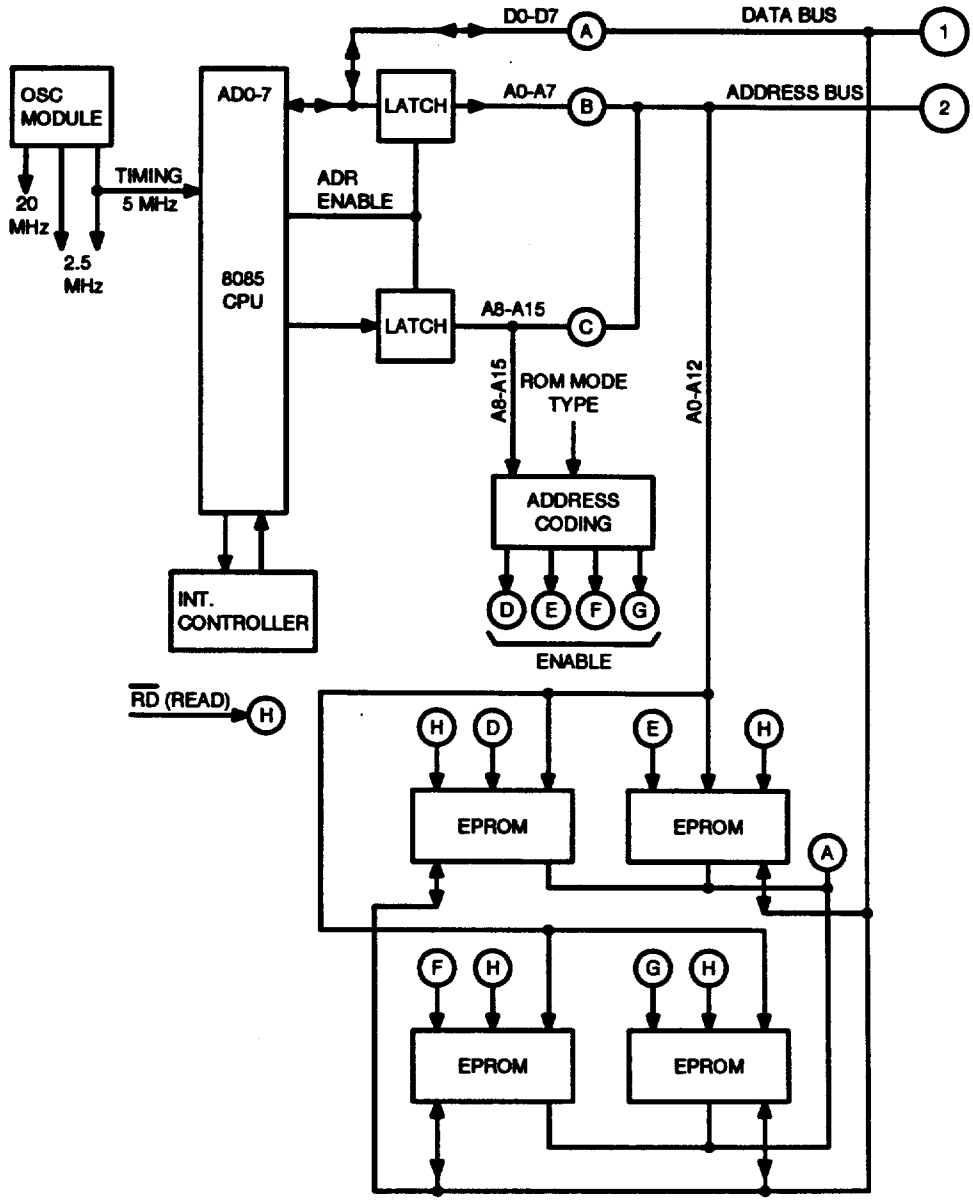

Figure 9. TN83/TN983 Block Diagram (Sheet 1 of 4)

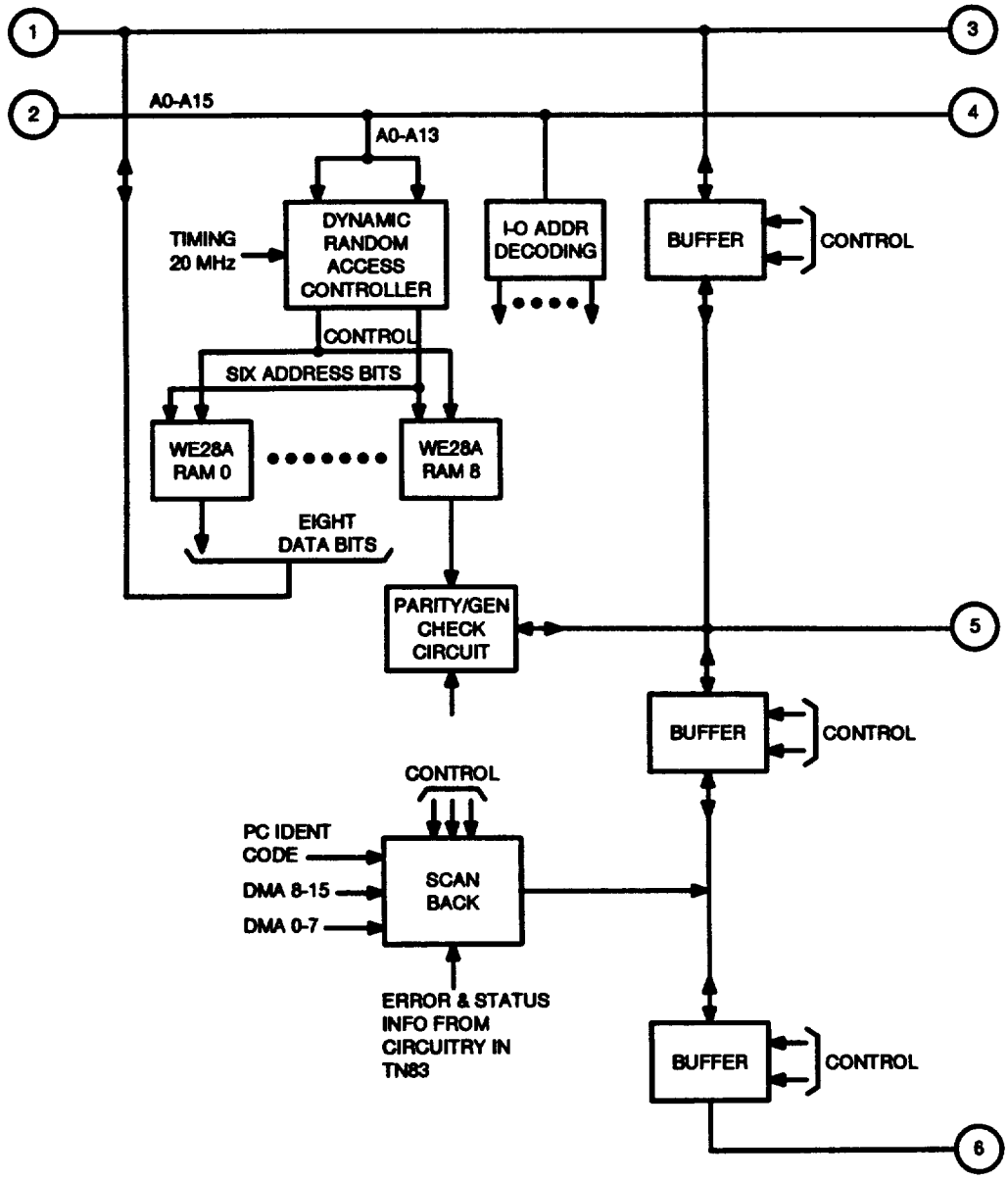

Figure 9. TN83/TN983 Block Diagram (Sheet 2 of 4)

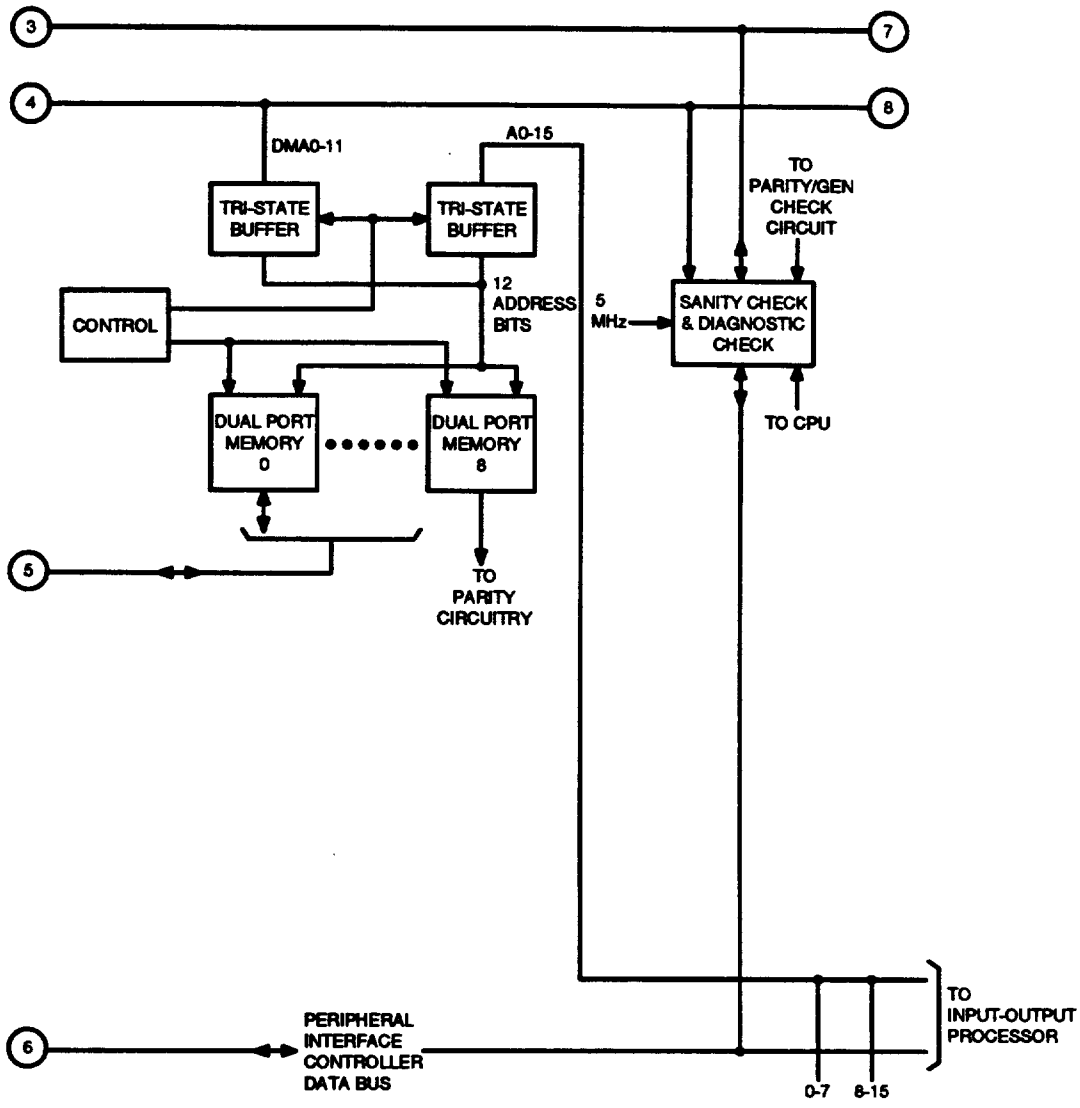

Figure 9. TN83/TN983 Block Diagram (Sheet 3 of 4)

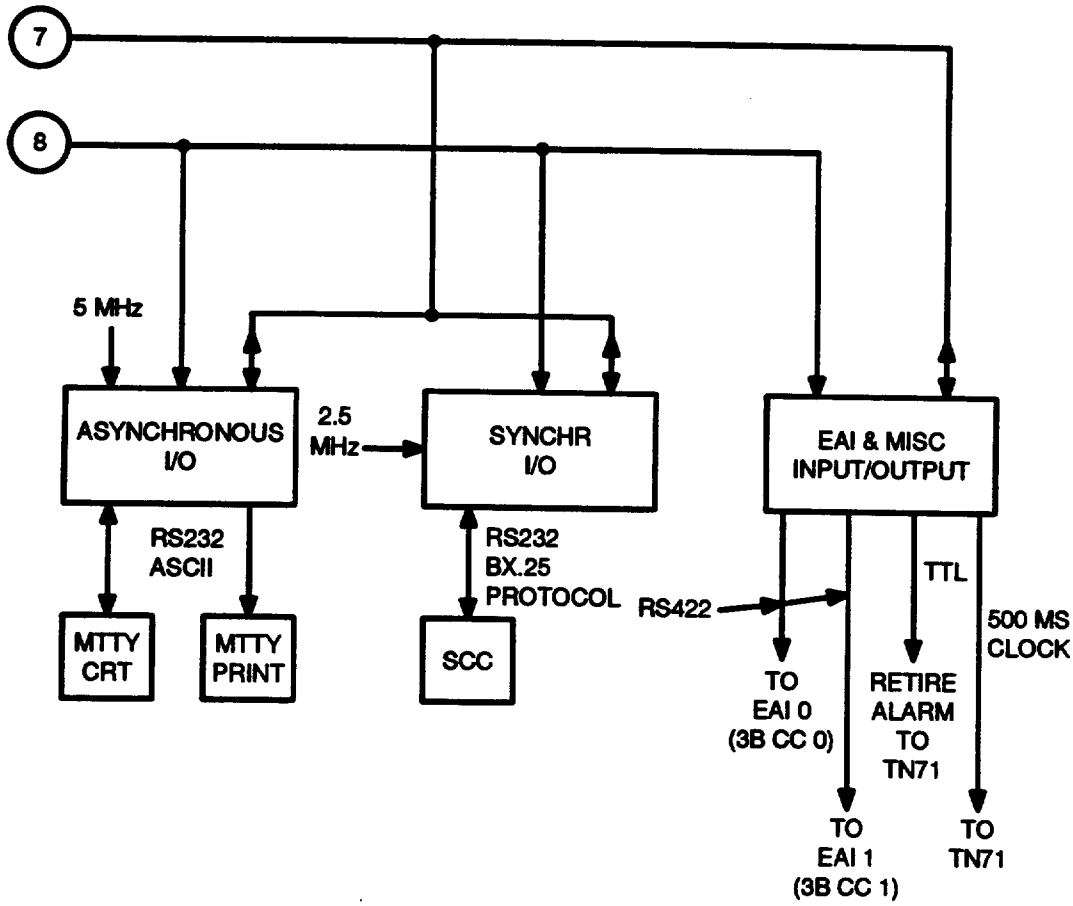

Figure 9. TN83/TN983 Block Diagram (Sheet 4 of 4)

Table E. TN83 Inputs and Outputs

Interface	Lead	Function
Maintenance TTY	CRTTXD0	Transmitted data to maintenance teletypewriter
	CRTDTR0	Data terminal ready to data communication equipment (DCE) (port switch control)
	CRTDTS0	Request to send to DCE
	CRTRXD0	Receive data from DCE
	CRTDSR0	Data set ready from DCE
	CRTCTS0	Clear to send from DCE
	CRTDCD0	Data carrier detect from DCE
Switch control center	SCCTXD0	Transmit data to link
	SCCDTR0	Data terminal ready to MODEM
	SCCRTS0	Request to send to MODEM
	SCCRXD0	Receive data from link
	SCCRXC0	Receive clock from MODEM
	SCCTXC0	Transmit clock from MODEM
	SCCDSR0	Data set ready from MODEM
	SCCCTS0	Clear to send from MODEM
	SCCDCD0	Data carrier detected from MODEM
Emergency action interface (EAI) circuit pack 0 (TN11)	EAI0TXD1	Data transmitted to TN11 circuit pack in central control (CC) 0
	EAI0RXD0	
EAI 0	EAI0RXD1	Data received from TN11 circuit pack in CC 0
	EAI0RXD0	
	EAI0SRQ1	Service request from EAI 0
	EAI0SRQ0	
EAI circuit pack TN11 in CC1	EAI1TXD1	Data transmitted to TN11 circuit pack in CC 1
	EAI1TXD0	
EAI 1	EAI1RXD1	Data received from TN11 circuit pack in CC 1
	EAI1RXD0	
	EAI1SRQ0	Service request from EAI 1
	EAI1SRQ0	

5. Maintenance

5.01 A suspected faulty controller may be tested by the computer. There are no provisions for manual interface on the circuit packs. A test however, may be initiated by inputting a message at the maintenance TTY, and receiving a message relative to the results of the test.

5.02 Each controller circuit pack contains PROM which conditions the circuitry and microprocessor to receive initializing data from the computer. Data and/or address data may be looped back through the scanback circuitry to the computer as a part of the overall test.

5.03 Each controller contains isolation circuitry controlled by the computer which inhibits the error, interrupt, service request, controller selected acknowledge, and data bus outputs to the computer.

5.04 With the exception of the UN33, each controller circuit pack contains a dynamic RAM (16K by 9-bit wide) which is utilized to store the program for that particular controller. Should the dynamic RAM need to be reloaded, the PROM and microprocessor condition the circuit pack and control reloading the dynamic RAM from the computer. Diagnostic programs may also be loaded from the computer.

6. Power

6.01 Each controller circuit pack receives fused power from its host IOP. Table F lists the controllers and required power input.

Table F. Controller Circuit Pack Input Voltage Requirements

Circuit Pack	+5 V	-5 V Memory	+12 V Memory	-12 V E1A	+12 V E1A	-48 V
UN32	X	X	X			
UN134/UN52	X	X	X			
UN33	X					X
TN74	X	X	X	X	X	X
TN75B	X	X	X	X	X	X
TN82	X	X	X	X	X	
TN83	X	X	X	X	X	

Controller Power Alarms

6.02 Fuse alarms and power converter alarms in the IOP provide inputs to the peripheral control frame alarm circuitry. AT&T 254-301-105 contains a detailed coverage of power distribution and alarmed.

UN33 Power

6.03 The UN33 contains a –48 volt to +6 volt floating output converter. A series current limiting resistor in –48 volt input is bypassed by a mechanically operated switch when the circuit pack is properly plugged-in. When the circuit pack is removed, the switch opens and removes the short from the resistor. The switch is linked to a lever on the front of the circuit pack. The 6-volt floating output is monitored for foreign potentials and grounds which might occur on the signal distribute and scan point pairs. A foreign potential of +2 volts to +140 volts, –2 to –140 volts, and a ground will be detected on the UN33 and reported on the error lead to the computer via the UN25 interface.

7. Acronyms and Abbreviations

7.01 The following is a list of acronyms and abbreviations used in this practice.

ASCII	American Standard Code for Information Exchange
CC	Central Control
CCITT	Consultative Committee International Telephone and Telegraph
CP	Central Processor
CPU	Central Processor Unit
DDSBS	Duplex Dual Serial Bus Selector
DCE	Data Communication Equipment
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DSCH	Dual Serial Channel
DUI	Direct User Interface
EIA	Electronic Industries Association
EPROM	Erasable Programmable Read-Only Memories
I/O	Input/Output
IOP	Input/Output Processor

IOMI	Input/Output Microprocessor Interface
MCS	Microcontrol Store
PC	Peripheral Controller
PIC	Peripheral Interface Controller
PROM	Programmable Read Only Memory
RAM	Random Access Memory
SCC	Switching Control Center
SCSI	Small Computer System Interface
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver Transmitter

How Are We Doing?

Document Title: AT&T 3B20D Model 1 Computer General Description

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