AT&T 3B20D Model 1 Computer Storage Module Drive Disk File Controller Description and Theory of Operation

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1. Overview

1.01 This practice provides a physical and functional description and theory of operation of the storage module drive (SMD) disk file controller (DFC) used in the 3B20D Model 1 computer. This practice describes the SMD-DFC only. All references to DFC within this practice pertain to the SMD-DFC.

1.02 This practice is being reissued to include information about the Small Computer System Interface (SCSI) and the effects it has on the 3B20D Model 1 computer and to provide changes that distinguish this DFC from other versions or types that may also be provided on the 3B20D computer. Since this is a general revision, revision arrows used to denote significant changes have been omitted. The Equipment Test lists are not affected.

1.03 This practice contains no admonishments.

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A. Purpose

1.07 The DFC provides mass storage capability for the 3B20D Model 1 computer. The DFC provides microprocessor control, which interprets and executes commands generated in the control unit (CU). Information is then transferred between the CU and moving head disk (MHD) drives. The DFC also provides control input to the disk drives, monitors the operational status of the disk drives, and manages the flow of data between the CU and the disk drives. The SMD-DFC can only be connected to disk drives with a SMD interface.

1.08 Figure 1 shows a typical computer floor plan. Data flow between the disk drive and the DFC is in serial format and occurs at a 10-MHz bit or a 1.6-µs word rate. The DFC is located within the peripheral control frame (Figure 2).

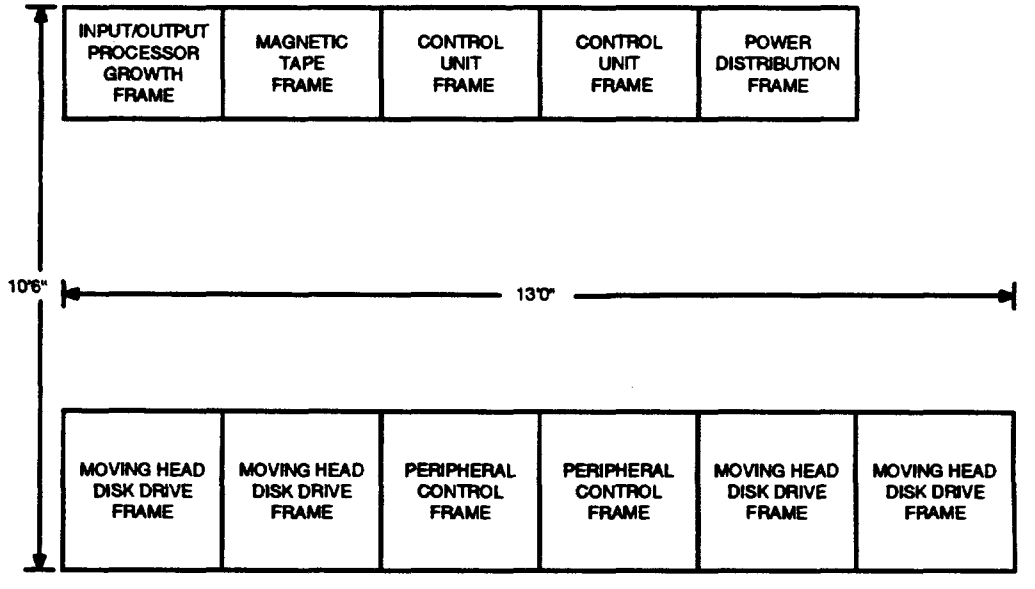


Figure 1. Typical Computer Floor Plan

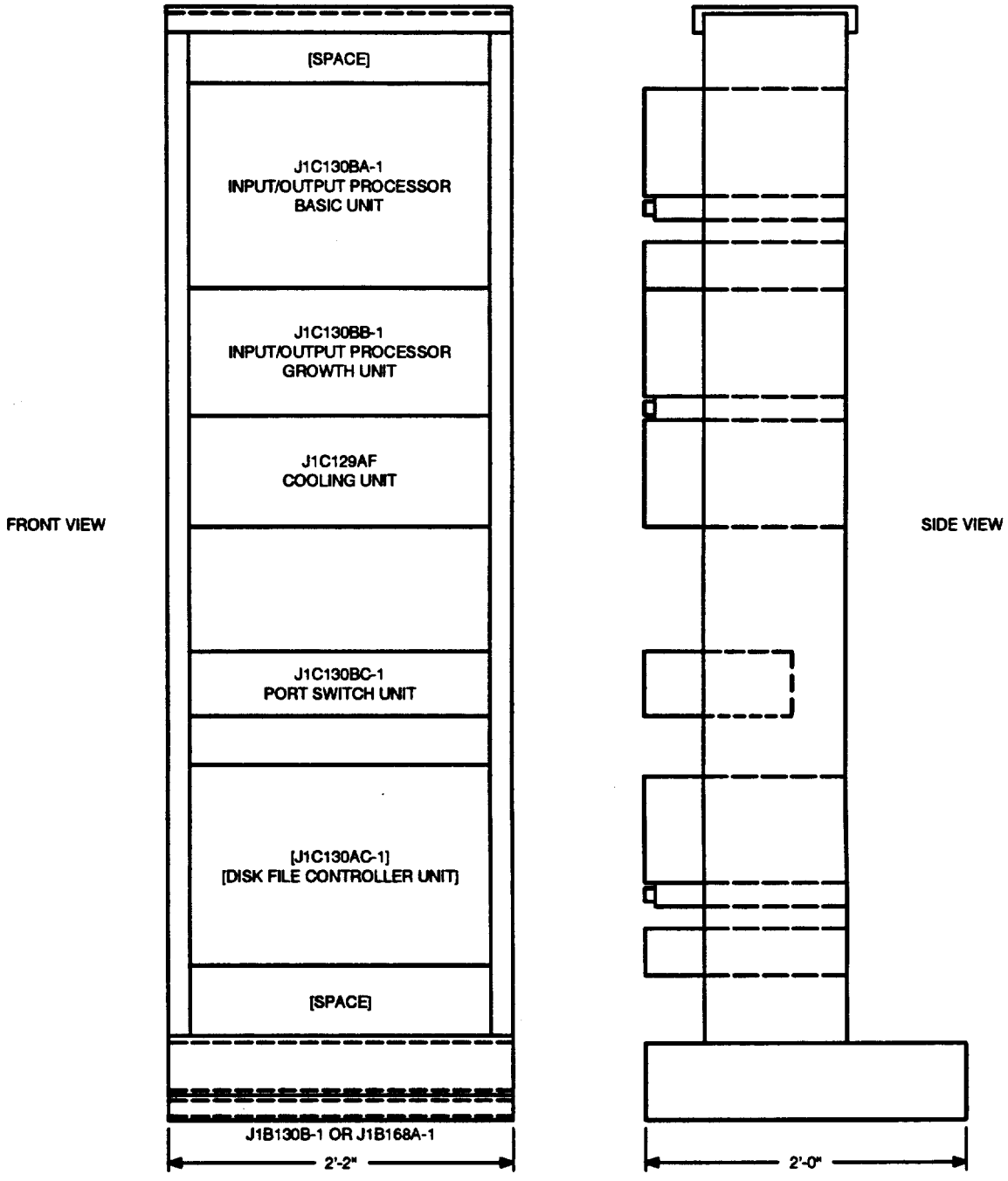


Figure 2. Typical Peripheral Control Frame With Disk File Controller

B. Configuration

1.09 The DFC allows the computer to interface with up to 16 disk drives via a common (daisy chained) control cable (Figure 3).

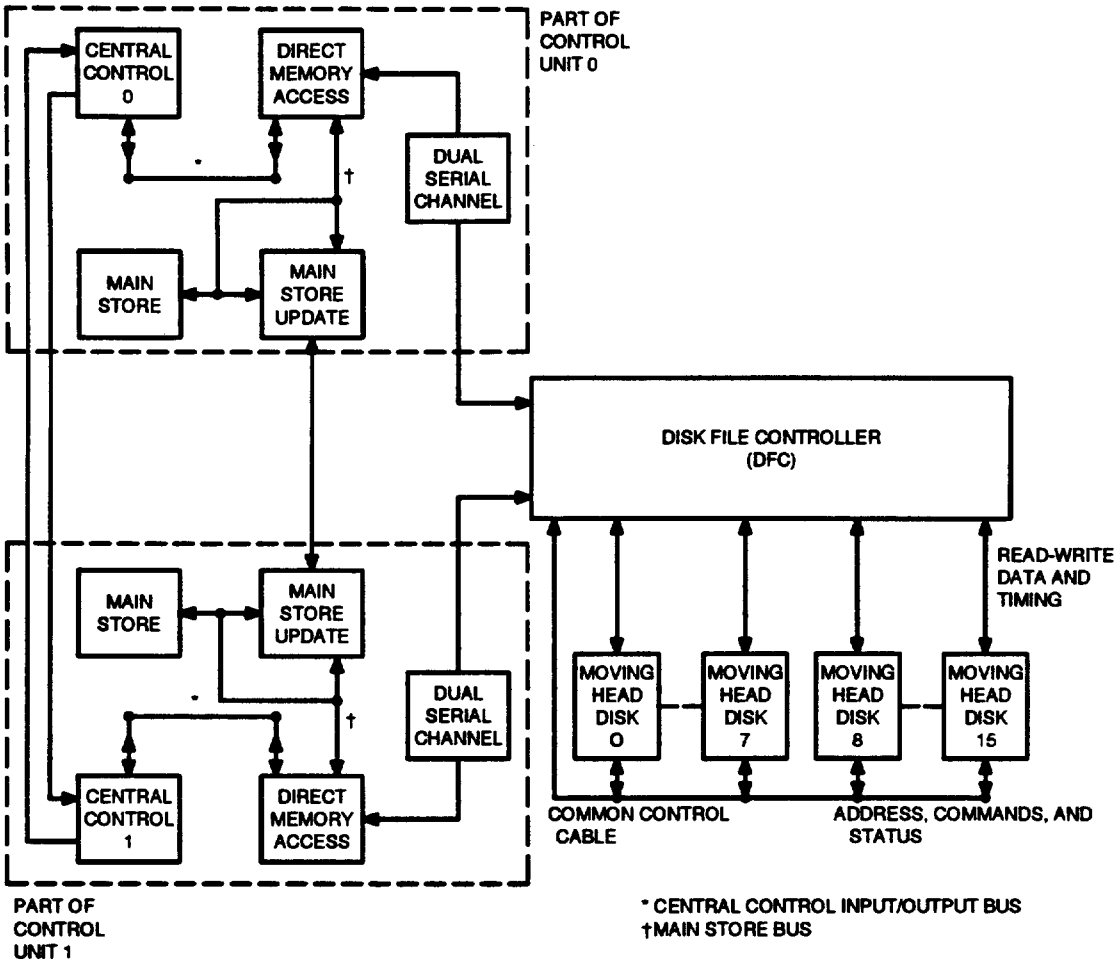


Figure 3. Control Unit—Moving Head Disk Drive Interface

1.10 The DFC interfaces to the computer via a dual serial channel (DSCH) associated with a direct memory access controller (DMAC) in the direct memory access (DMA) input/output unit. The DMAC facilitates transmission of data blocks between the DFC and main store. Each DFC can interface with two CUs (duplex system).

1.11 Each DFC/CU interface contains a cable of five twisted pairs (Figure 4). Two pairs transmit bidirectional data; two pairs transmit dedicated clock pulses; and one pair transmits a service request to the CU via the DSCH. This service request can be an interrupt request, a DMA setup request, or a DMA transfer request.

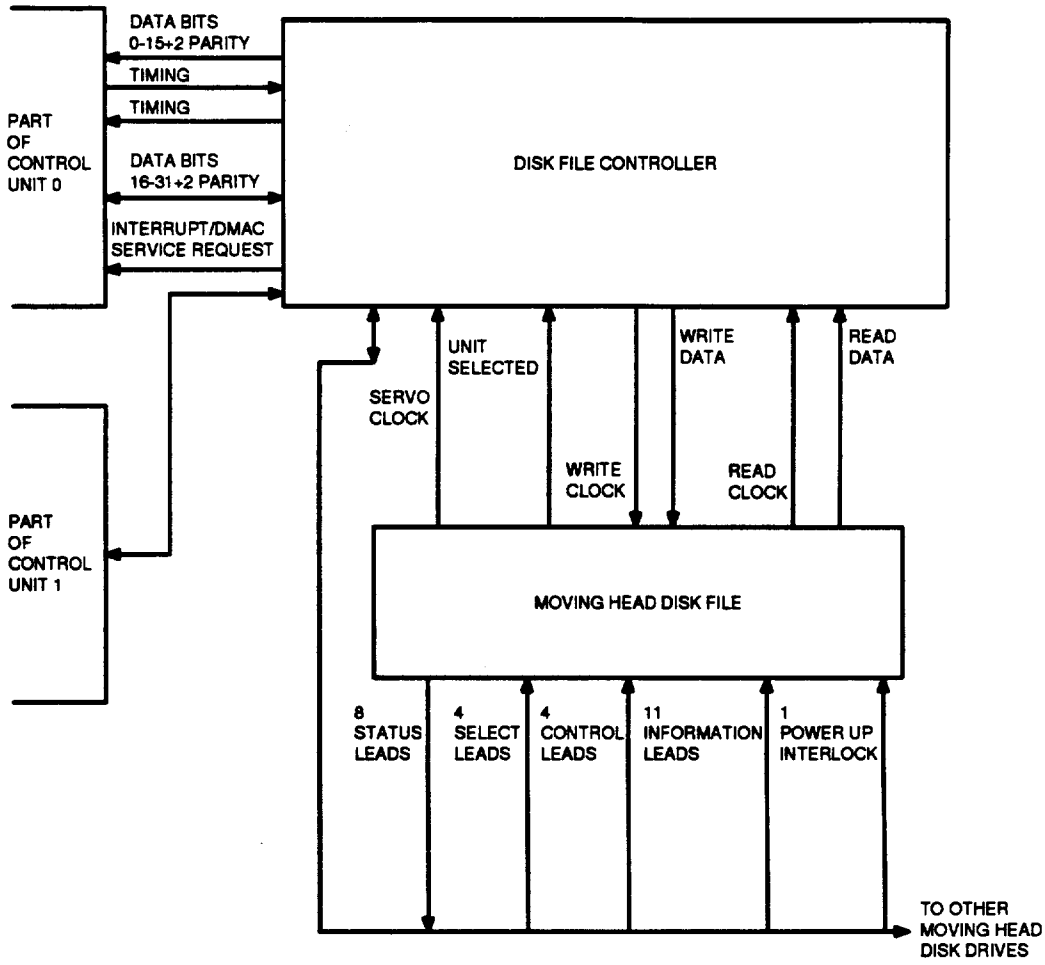


Figure 4. Disk File Controller Unit Control Interfaces

2. Physical Description

2.01 The DFC unit (Figure 5, 6, and 7) consists of the following:

(a) Microcontrol store—TN62 for generic 1 (Figure 5) and TN68 for generic 2 (Figure 6)

(b) Writable control store—TN 18 for generic 3 (Figure 7)

(c) Peripheral interface controller (PIC)—TN61 for generics 1 and 2 (Figure 5 and 6) and TN 20 for generic 3 (Figure 7)

(d) Parallel serial data interface (PSDI)—TN65

(e) Moving head disk data/clock (MHDD/C)—TN64

(f) Moving head disk control—TN63

(g) Bus interface controller (BIC)—TN 70

(h) Duplex dual serial bus selector (DDSBS)—TN69

(i) Power monitor—TN 73

(j) Control and display—ABB1

(k) Power converter 133A

(l) Fuse panel ED-4C181.

Each TN circuit pack is a multilayer board equipped with two 100-pin female connectors. Each connector contains four 25-pin rows. These connectors mate with square pins that protrude through the multilayer board backplane.

2.02 An ED-4C181 type fuse panel is mounted beneath the plug-in circuit packs (Figure 5, 6, and 7). Fuse positions are provided for +5 volt and –48 volt power. Each equipped position contains fuse holders for a main and pilot fuse.

2.03 Each DFC contains a 133A DC-to-DC power converter (plug-in). Two mating connectors on the DFC mounting plate provide an interface for –48 volt power input and +5 volt power output. The power converter contains a mechanical latch and power switch that can be operated only when the power converter is properly plugged in.

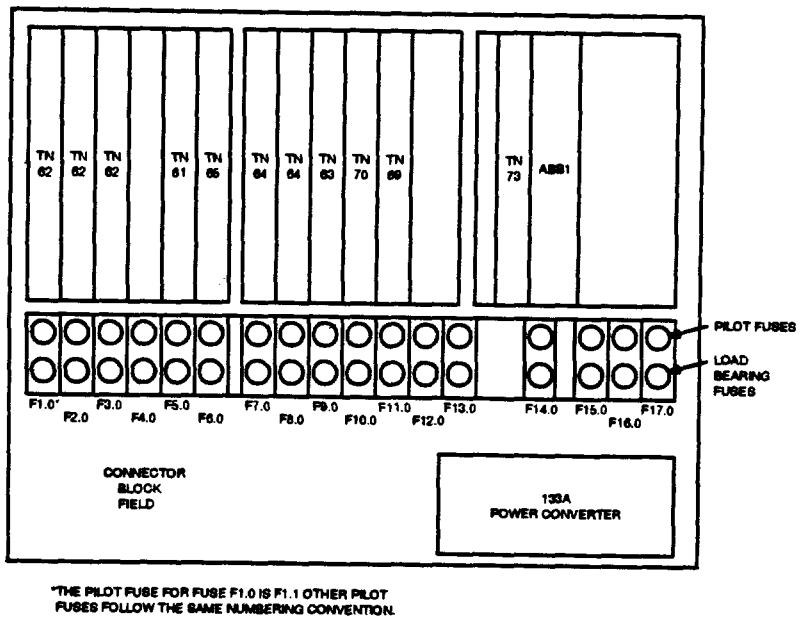


Figure 5. Typical Disk File Controller Unit Layout (Generic 1)

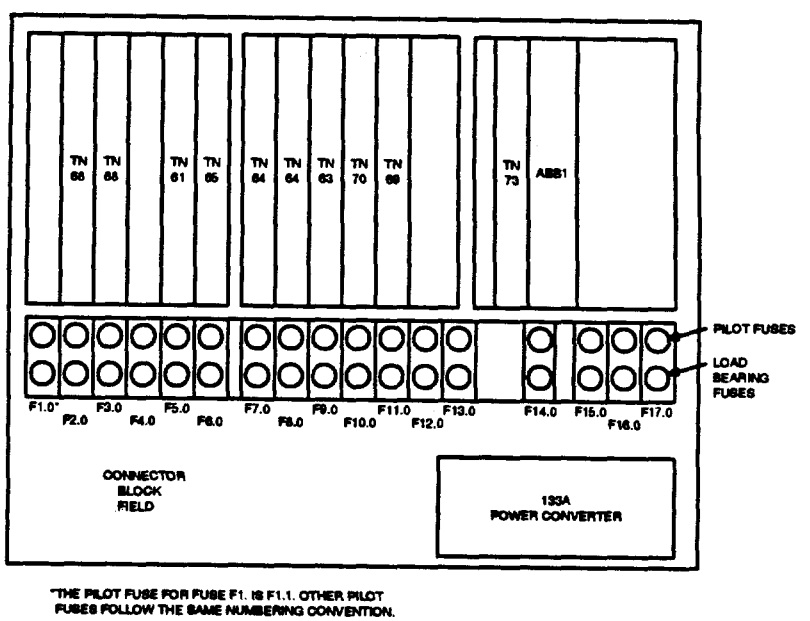


Figure 6. Typical Disk File Controller Layout (Generic 2)

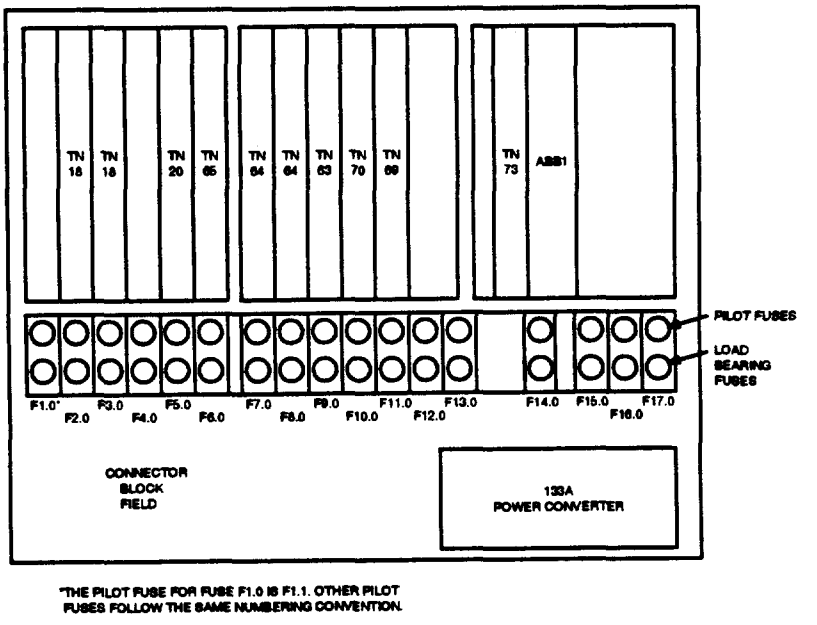


Figure 7. Typical Disk File Controller Layout (Generic 3)

3. Interfaces

3.01 The DFC provides the interface between the disk drives and the CU of the computer. The CU issues commands and data to the DFC where they are interpreted and executed under microprocessor control. The CU commands, via the DFC, cause an addressed disk drive to read from, or write to, a disk or main store. A DFC interfaces with two CUs. Normal operation dictates that only one CU is ever active at a time. A CU is recognized on a first-come, first-served basis. Data written on a disk or read is in a serial format at 10-MHz rate.

4. Functional Description

A. General

4.01 The DFC is a self-contained assembly consisting of TN type circuit packs (Table A) which perform signal and control format changes, timing, read/write functions, job priority control, and error detection.

Table A. Circuit Packs Used in Disk File Controller Unit

Circuit Pack	Quantity Used	Nomenclature
TN 18	2	Writable Control Store 1 (Generic 3 Only)
TN 20	1	Peripheral Interface Controller (Generic 3 Only)
TN61	1	Peripheral Interface Controller (Generics 1 and 2 Only)
TN62	3	Microcontrol Store 1 (Generic 1 Only)
TN63	1	Moving Head Disk Control
TN64	Up to 2	Moving Head Disk Data/Clock
TN65	1	Parallel Serial Data Interface
TN68	2	Microcontrol Store 1 (Generic 2 Only)
TN69	1	Duplex Dual Serial Bus Selector
TN 70	1	Bus Interface Controller
TN 73	1	Disk File Controller Power Monitor
ABB1	1	Power Control and Display

4.02 A DSCH is connected to the DDSBS, which allows either CU to communicate with the DFC. Data and commands for the DFC are transmitted by the DSCH to the DDSBS over a 5-twisted pair cable that is duplicated for each CU. The data transmitted (32 + 4 parity bit words) is in the form of two serial 16 + 2 parity bit words. The low-order bits (0 through 15 + 2 parity) and a 4-digit start code are transmitted over a data LO lead; the high-order bits 16 through 31 + 2 parity and a start code are transmitted over the data HI lead. The start code is used by the DFC to set up the mode of operation or to signal a command is present. After information is received by the DFC, a response code is transmitted to the DSCH to let the CU know how the data or command was received by the DFC.

B. Disk File Controller

4.03 The DFC contains its own PIC and associated microcontrol store (generics 1 and 2) or writable control store (for generic 3).

4.04 The PIC circuit pack (TN61 for generics 1 and 2) consists of a controller and up to 65K words of microcontrol store. Additionally, the PIC contains a 16-bit register and arithmetic logic unit (ALU), a 16-bit microprogram sequencer, a condition test multiplexer, and 4K bytes of random access memory (RAM).

4.05 The microcontrol store circuit pack (TN62 for generic 1) contains 4K by 40-bit program store and the PIC clock circuit. The microcontrol store circuit pack contains parity check circuits for the microdata word and microaddress decoding circuits for seven additional 4K-word microstore circuit packs.

4.06 To improve the performance of the DFC, new firmware is needed. A new microcontrol store circuit pack (TN68 for generic 2) is implemented with 8K by 40-bit program store. To take advantage of the added memory, a new PIC circuit pack (TN 20 for generic 3) with expanded RAM is implemented. Also, a writable control store circuit pack (TN 18 for generic 3) with 8K by 40-bit program store will replace the TN68 circuit packs. The TN 18 circuit packs provide the capability of updating the firmware by reprogramming the erasable programmable read-only memory (PROM).

C. Peripheral Interface Controller

4.07 The peripheral interface controller (PIC) contains a 4K by 18-bit (16 data and 2 parity) RAM used for data storage. Associated with the RAM is a 12-bit RAM address sequencer, which provides a 4-level stack onto which interim addresses can be gated and retrieved. An incrementer is provided for automatic incrementing capability.

D. Bus Interface Controller

4.08 A BIC funnels information from the DDSBS to the PIC, and functions as a buffer between the 32-bit DDSBS and the 16-bit word of PIC. Contained in the BIC are a 16-word by 32-bit data first-in, first-out (FIFO), a 32-bit command register, 32 bits of status flags, and a 16-bit sanity and interval timer. Each is segmented into two 16-bit fields for access by the PIC. The BIC buffers data and commands to the PIC, buffers data and status information from the PIC, and performs the necessary handshaking protocols to communicate with the DDSBS.

4.09 The BIC FIFO may be operated in a single 32-bit word mode or in a 16-word block mode. The FIFO may be accessed by either the PIC or the DDSBS, but not both at any one time. The 32-bit command register records commands from the CU to the PIC. The PIC may read this register and, for maintenance functions, write data in the register.

4.10 The sanity and interval timer inputs are derived from a 16-bit counter (sanity) on the BIC. Also, the PIC is provided read/write access to this counter for timing.

4.11 The flag circuits (32 bits) within the BIC request interrupt and DMA functions from the CU, signal the PIC of the presence of a CU command or data transfer request, and record the detection of error conditions. These flags are segmented into status flags (16 bits) and error flags (16 bits).

4.12 The status flags are:

- Command
- Command in progress
- Data
- Transfer mode
- Data FIFO word count
- Interrupt
- DMA transfer
- End of data expected
- End of data received
- DMA setup
- PIC data bus parity check enable
- Interface enable.

4.13 The error flags are:

- Command register overflow
- Data register overflow
- Unused
- Data bus parity
- Sanity failure
- PIC soft error summary
- PIC fatal error summary
- 3B computer error summary
- End of data
- Setup overwrite
- Information parity failure.

E. Moving Head Disk Control

4.14 A MHD control circuit pack (TN63) provides an interface between the PIC and the control cable of the MHD drives. This control cable allows the PIC to select the disk drive unit, head position, read/write mode, and to monitor the disk drive status.

4.15 The MHD control has five registers of varying lengths. The first four registers, explained as follows, set up the disk drive for read and write operations. The fifth register is a status register.

(1) ***Device Enable Register:*** This register produces the cable enable signal. The register must be active for the disk drive to receive information on the control cable.

(2) ***Unit Select Register:*** This register stores the number of the disk drive that has been selected (disk drive 0 through 15).

(3) ***Tag Register:*** This register produces strobes for the disk drives cylinder select, head select, control select (read/write functions), and unit select strobe.

(4) ***Control Register:*** The function of these bits depends on the TAG register. When TAG = cylinder select, control register = cylinder number. When TAG = head select, control register = head number. When TAG = control select, control register = read/write, fault clear, etc.

(5) ***Status Register:*** This register presents MHD status information to the PIC. The status register is written into by the disk drives and read by the PIC.

F. Parallel Serial Data Interface

4.16 The parallel serial data interface (PSDI) communicates with the PIC over three buses: 16 + 2 parity bit data bus (parallel), 5-bit source address bus, and a 5-bit destination address bus. These buses allow the PIC to send commands to the PSDI, retrieve status and error, and send/receive data.

4.17 The PSDI allows the PIC to transmit data to or receive data from a disk drive via the MHDD/C. The PSDI takes parallel information from the PIC and converts it to a serial format that the MHDD/C uses during a write operation. During a read operation, the PSDI takes serial information from the MHDD/C and converts it to a parallel format for the PIC.

4.18 The PSDI (TN65) consists of a FIFO, shift register, command/status register, bit word counter, and error detection/location logic. When writing onto the disk, a parallel-to-serial conversion takes place in the PSDI between the data FIFO and the shift register. The command/status register controls the communication between the PSDI and the MHDD/C. Bits 0, 1, and 2 of the command/status register are loaded and read by the PIC, while bits 3 through 15 are generated internally to the PSDI and read by the PIC.

G. Moving Head Disk Data/Clock

4.19 The MHDD/C is an interface between the PSDI and up to eight disk drives. The MHDD/C converts transistor-transistor logic (TTL) signals from the PSDI to a differential voltage signal that the disk drive can use to write data on the disk. During a disk read, the MHDD/C converts differential voltage signals from the disk drive to TTL signals which the PSDI requires.

5. Theory of Operation

A. General

5.01 Dual serial data streams accompanied by dedicated timing pulses are transmitted between the DMAC, DSCH, and DDSBS of the DFC. This transmission occurs over a 5-twisted pair cable, which is duplicated for each CU. This interface is bidirectional with each DSCH capable of conveying 16 data and 2 parity bits (2 bytes) accompanied by a start code. Odd parity is observed for each byte. The start code is used to signal a command is present and to set up the mode of operation (that is, disk write operation or disk read operation).

5.02 All actions within the DFC occur under the control of the PIC circuit pack, which is a microprocessor implemented with bipolar bit slice parts. The instructions, which the PIC executes, are stored in PROMs on three microcontrol store circuit packs (TN62s) for generic 1 or two microcontrol store circuit packs (TN68s) for generic 2. The instructions that the PIC executes for generic 3 will be stored in erasable PROMs on two writable control store circuit packs (TN 18s).

5.03 The PIC interfaces to the computer via the BIC (TN 70) and the DDSBS (TN69). (See Figure 8 for generic 1, Figure 9 for generic 2, and Figure 10 for generic 3.) Actually, the PIC has direct access only to the BIC circuit pack, and information transfers between the BIC and DDSBS occur under the control of the computer (Table B). The first four bits of each serial data stream (high data bits and low data bits) contain a code which, when decoded, determines the DFC mode of operation (Figure 11). The first bit is always a 1 with a 1-out-of-3 code following the leading 1. Table C lists the commands transmitted by the CU and the responses generated by the DDSBS circuit pack.

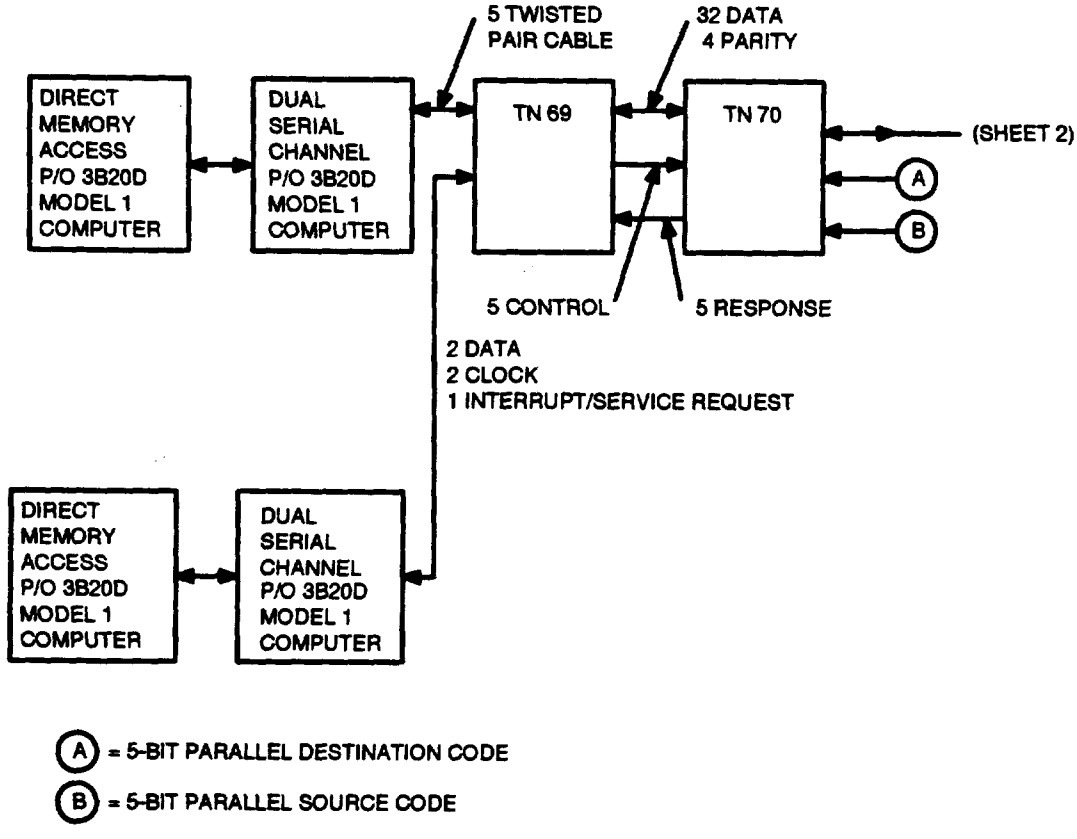


Figure 8. Disk File Controller Unit Block Diagram (Generic 1) (Sheet 1 of 2)

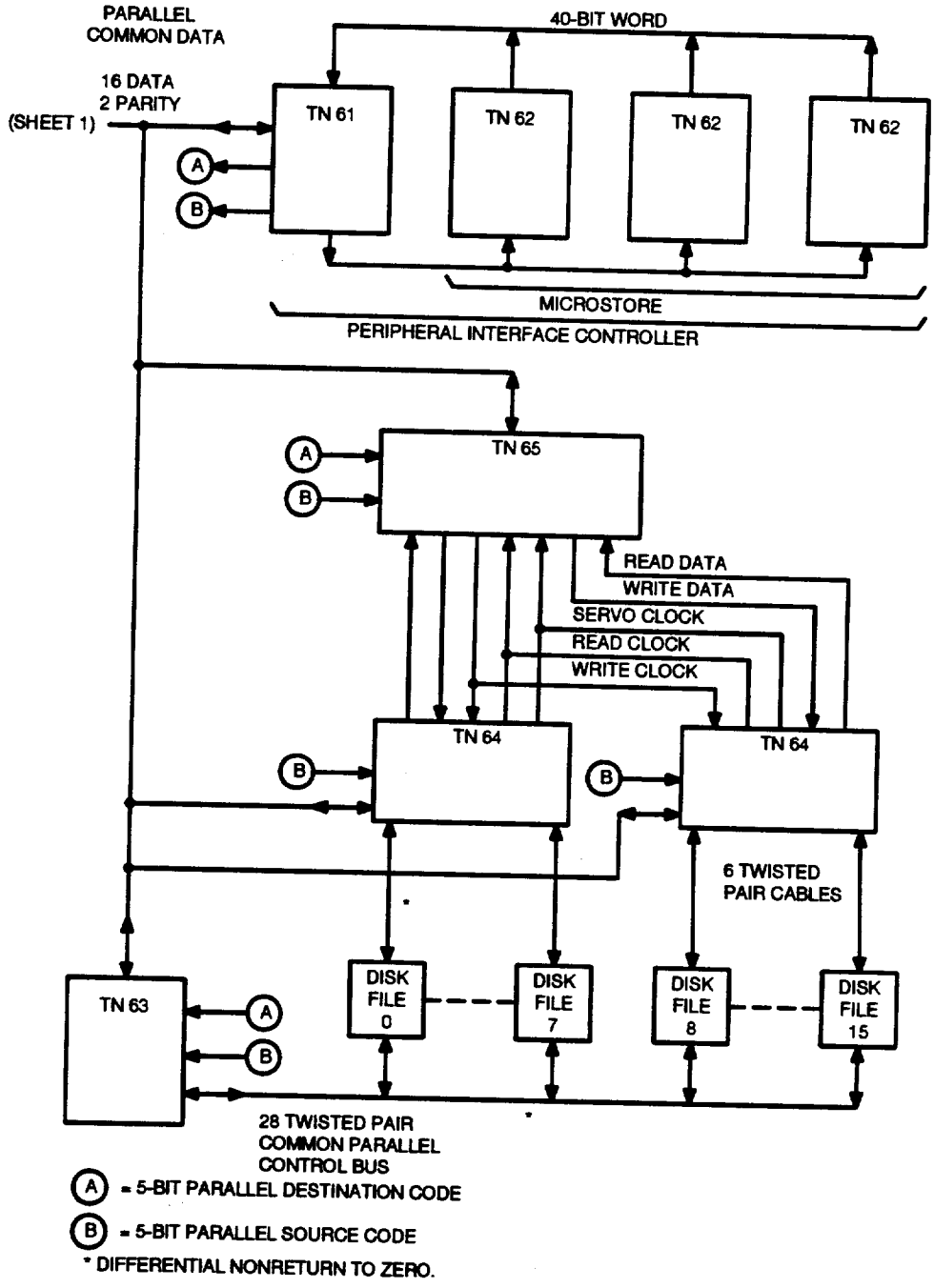


Figure 8. Disk File Controller Unit Block Diagram (Generic 1) (Sheet 2 of 2)

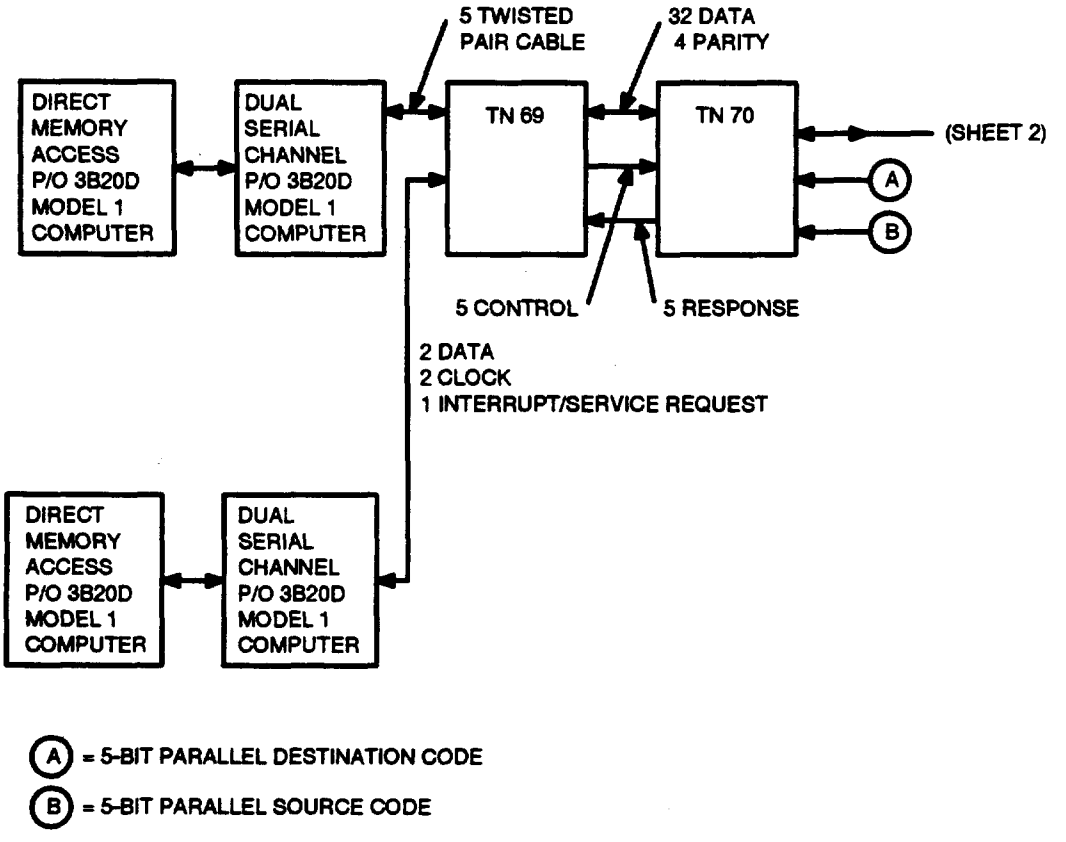


Figure 9. Disk File Controller Unit Block Diagram (Generic 2) (Sheet 1 of 2)

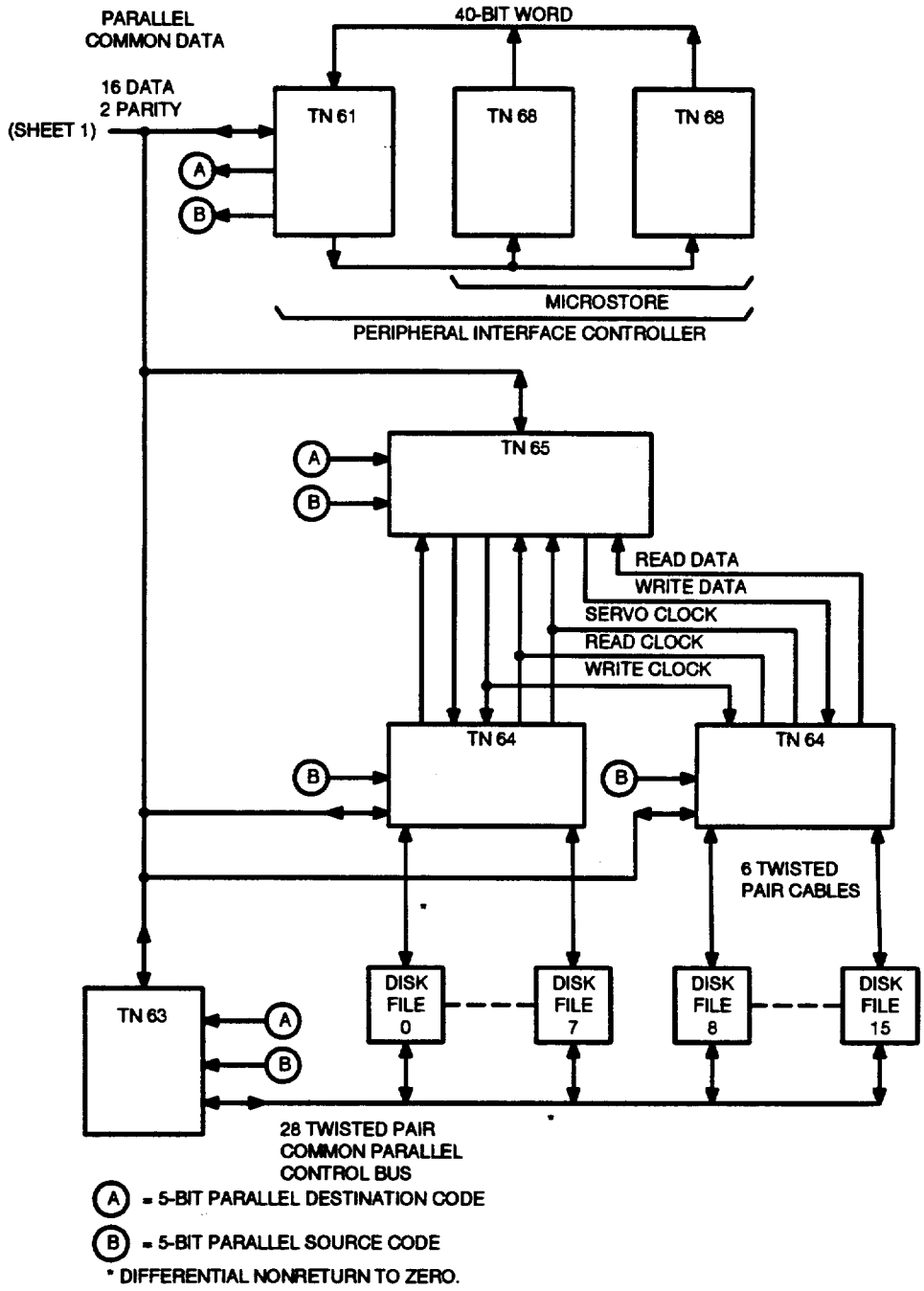


Figure 9. Disk File Controller Unit Block Diagram (Generic 2) (Sheet 2 of 2)

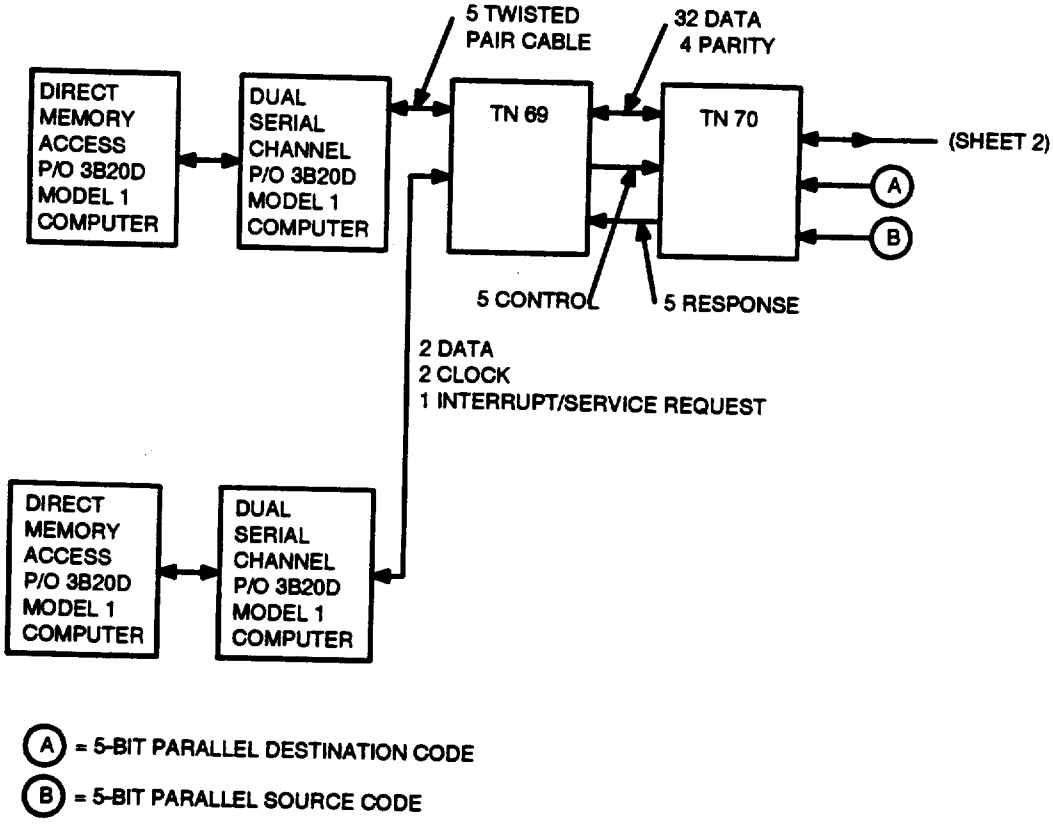


Figure 10. Disk File Controller Unit Block Diagram (Generic 3) (Sheet 1 of 2)

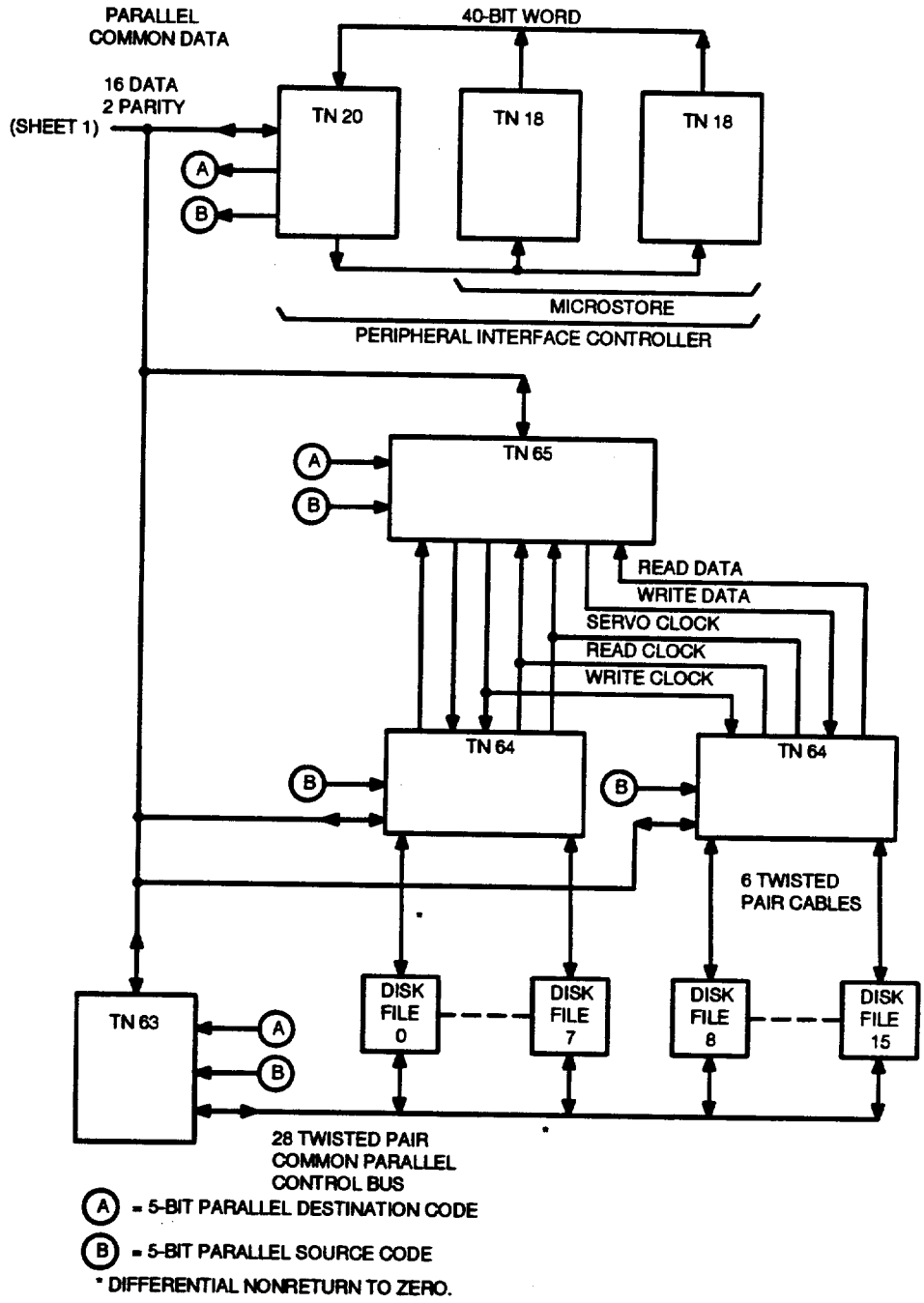


Figure 10. Disk File Controller Unit Block Diagram (Generic 3) (Sheet 2 of 2)

Table B. DDSBS and BIC Control Interface

Response	Meaning
SYNC	Issued when the BIC has responded to control signal. SYNC removed when control signal removed.
ER	Issued when an abnormal condition is detected in the BIC. Circuit pack TN69 samples ER lead after generation of SYNC signal.
INTP	Issued when the DFC wishes to interrupt the CU.
XFER	Issued when the DFC informs the direct memory access controller that it is ready to send or receive another word or block during an autonomous DMA transfer.
SETUP	Issued when a DFC wishes to initiate a DMA setup. The DMA will acknowledge the request by activating the data request lead.

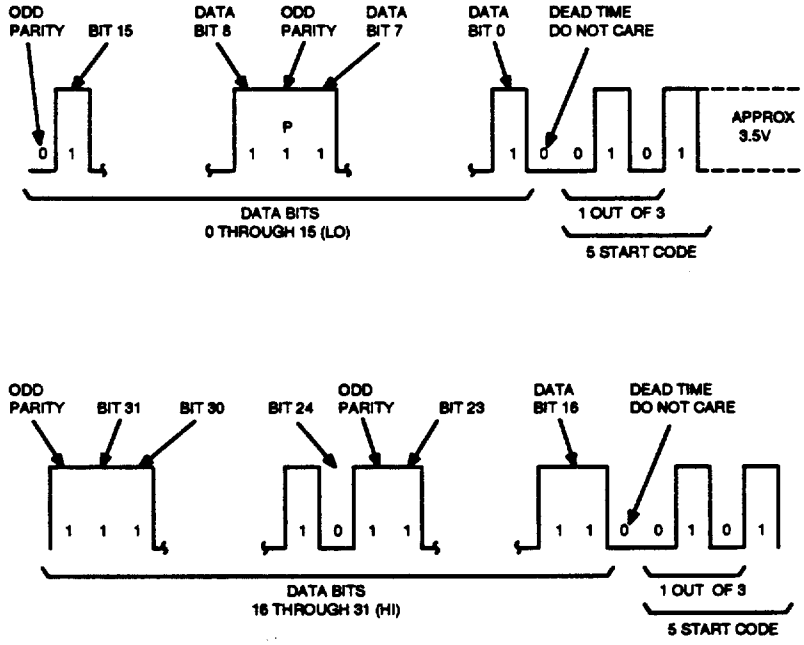


Figure 11. Disk File Controller—Direct Memory Access Message Format

Table C. Coded Commands and Responses

Command To TN69 Circuit Pack	HI Preamble Code Bits 16 Thru 31	LO Preamble Code Bits 0 Thru 15
Write Data (Word Mode)	0011 = 3	0011 = 3
Send Device Command	0011 = 3	0101 = 5
Write Data (Block Mode)	0011 = 3	1001 = 9
Read Data (Word Mode)	0101 = 5	0011 = 3
Sense Status	0101 = 5	0101 = 5
Read Data (Block Mode)	0101 = 5	1001 = 9
End of Transfer	1001 = 9	0011 = 3
Response To 3B20D Model 1 Computer		
All Seems Well	0011 = 3	0011 = 3
Device Reported Error	0011 = 3	0101 = 5
Illegal 3B20D Model 1 Computer Command	0101 = 5	0011 = 3
Illegal Start Code	0101 = 5	0101 = 5

5.04 The PIC informs the computer that it needs service via three request mechanisms initiated by the writing bits in the status register. These three request mechanisms are DMA setup request, interrupt request, and transfer request.

5.05 A DMA setup request informs the DMAC that the DFC wants to transfer control information to the DMAC. This information tells the DMAC where, in main memory, data transfers are to commence when the DFC sends a transfer request. A DMA transfer request informs the DMAC that the DFC wants to transfer a block of sixteen 32-bit words to/from main store. When the DMAC services this request, it commands the DSCH, which is interfaced to the DMAC in the computer, to transfer the contents of the BIC FIFO to the DSCH utilizing the serial data link between the DDSBS and DSCH. An interrupt request informs the computer that the DFC wants to communicate with the software disk driver via programmed (synchronous) input/output channels.

5.06 The PIC communicates to disk drives via the MHD control (TN63), MHDD/C, TN64, and PSDI, TN65. The MHD drive specifies that each disk drive should have two interfaces, one for command information and one for data.

5.07 Command information is transmitted to the disk drives over the "A" cable, which is a common bus originating at the DFC. The cable is routed to all disk drives connected to that DFC. The moving head disk control circuit pack contains several registers, to which the PIC has read/write access. The outputs of these registers, after

being level-shifted by differential line drivers, drive the "A" cable. This command interface allows the PIC to perform the following functions:

(1) Select (address) a disk drive for use

(2) Move heads to a desired cylinder

(3) Select a disk drive read/write head

(4) Command a disk drive to begin or stop reading/writing data

(5) Obtain disk drive status.

Because the "A" cable is a shared bus, the PIC can communicate with only one disk drive at a time, ie, the disk drive which is currently selected by the PIC.

5.08 The second disk drive interface consists of a serial clock signal, data signals, and a select acknowledge signal. These signals are transmitted between the disk drive and the DFC via a dedicated "B" cable, which is terminated in the DFC on the MHDD/C circuit pack. Each MHDD/C can support a maximum of eight disk drives. Therefore, a DFC must be equipped with two MHDD/C circuit packs, if the DFC supports more than eight disk drives. With two MHDD/C circuit packs, a DFC can support a maximum of 16 disk drives. The select acknowledge signal becomes active when the PIC selects a disk drive interfaced to the MHDD/C, via the MHD control circuit pack.

5.09 The MHDD/C circuit pack provides a level shifter and multiplexer for the serial clock and data signals. The multiplexed serial clock and data signals are transmitted to and from the PSDI circuit pack. These multiplexed signals are servo clock, read clock, read data (inputs to PSDI), write data, and write clock (outputs from PSDI).

5.10 The select acknowledge signal enables the MHDD/C circuit to select which clock and data signals from the disk drives are transmitted to the PSDI circuit. Additionally, the PIC circuit has read access to all the select acknowledge signals. This provides the PIC with the capability to verify that the designated disk drive has been selected.

5.11 The PSDI performs data conversion, generates a 32-bit error correction code (ECC) during disk writes, and provides ECC information during disk reads for the PIC circuit pack. Data conversions and ECC functions occur in the PSDI circuit pack under control of a hardware sequencer started and stopped by the PIC. The PSDI utilizes the read clock signal to format words from the serial read data stream during read operations. During write operations, the PSDI uses servo clock to generate the serial write data stream and the write clock signal, which are outputs to the disk drive.

B. Disk Read/Write

5.12 Each disk read or write operation, which the system wants the DFC to perform, is described to the DFC in the form of a job request containing the following details:

- Which disk drive
- Type of operation (read or write)
- Starting main store virtual address
- Starting disk block address
- Number of data blocks to transfer (block = 512 bytes)
- Job identification code.

To access the proper area of disk, the PIC decodes the binary-coded disk block address into cylinder, head, and sector numbers.

Disk Read

5.13 The PIC, via the MHD control, selects the desired disk drive. After verifying that the proper disk drive was selected, by reading the select acknowledge signals on the MHDD/C, the PIC causes the disk drive to move its read/write heads to the desired cylinder by issuing a seek command. When the heads have stopped moving, the PIC (via MHD control) selects the read/write head it wants to use. Before the beginning of the sector where data will be read from the disk, the PIC writes DMAC job setup information in the BIC FIFO and generates a setup request to the computer. When the beginning of the desired sector is under the read/write heads, the PIC (via the MHD control) commands the disk drive to read, initialize, and start the sequencers on the PSDI in a read mode. The PSDI examines the incoming serial data stream. After detecting the presence of SYNC characters, the PSDI begins assembling data words in the FIFO memory.

5.14 The PIC monitors the status register on the PSDI. When the PIC detects that the FIFO memory is half full (at least 16 words), it transfers 16 words from PSDI to a RAM buffer on the PIC. This process continues until 516 bytes (512 data + 4 address) have been transferred from PSDI to the buffer on the PIC. At this point, one sector of information has been read from the disk, and the PIC is waiting for the beginning of the next sector.

5.15 When the PIC detects the beginning of the next sector (drive status from MHD control), it commands the disk drive to stop reading (avoid reading over read/write splice at sector mark). If more data is to be read from the disk (that is, more than 512 bytes were requested in the original command), the PIC again commands the disk drive to start reading again within 10 microseconds. Before the PIC can begin transmitting the data in its RAM buffer to the computer, it must receive an interrupt from the PSDI. This informs the PIC that any error correction information for the sector which has just been read is now available.

5.16 When the PIC receives the interrupt from PSDI, it reads status and error correction information from registers on the PSDI. Based on this information, three possible conditions could arise at this point:

(a) The error correction information says that no errors were detected during the read of the sector.

(b) An error was made, and the information read from PSDI details which bytes in the received data need to be corrected.

(c) An error was made, and the information read from PSDI says that the error cannot be corrected.

The PIC corrects the data in its buffer if condition (b) occurs and then, as in condition (a), marks a control word in its RAM buffer that says this particular data block may be transferred back to the computer. If condition (c) occurs, the PIC terminates further processing of data from the disk (unrecoverable error) and reports failing job status to the computer. Additionally, if either condition (a) or (b) occurs, the PIC will verify that the address information contained in its RAM is what is expected.

5.17 At this point, the PIC has data that can be transferred to the computer, and data from the disk is continuing to be input to PSDI. The PIC divides its time equally between transferring data from its RAM buffer to BIC for transmission to the computer, and from the PSDI FIFO to the RAM buffer on the PIC. In transmitting data to the computer, only the 512 data bytes of the buffer are sent, and the 4 address bytes, which were read from the disk, are stripped off. This process continues until all the data that was requested in the job description has been transferred to the computer. At this time, PIC formulates a job completion report in its RAM buffer.

5.18 After transferring the completion report to the BIC FIFO, the DFC begins searching its job queue, located in its RAM buffer, for other disk jobs which it can perform.

Disk Write

5.19 The DFC actions during a write/disk operation are very similar to those during a read with the main differences being:

(1) Data is transferred from the computer to the PIC RAM buffer.

(2) Data is transferred from PIC RAM buffer to PSDI FIFO.

(3) An error correction algorithm is not performed by PIC because the disk is being written (that is, PSDI does not generate interrupts to the PIC after each sector is written on disk).

(4) Both PSDI and the disk drive are put in a write mode.

(5) The PIC will not allow the write operation to continue to the next succeeding sector on the disk unless all the data for that sector is present in PIC RAM buffer.

(6) The PSDI outputs serial data and clock to MHDD/C for transmission to the selected disk drive.

(7) The PSDI computes a 32-bit ECC for each sector and transmits it to the disk drive after the data has been sent. This allows the DFC to correct up to a maximum of 11 consecutive bits in a sector.

6. DC Power

A. General

6.01 The DFC receives –48 volt fused power from a computer power distribution frame (PDF). The –48 volt power is terminated on push-on type terminals on the rear of the DFC. A resistance-capacitance input power filter across the –48 volt input reduces the effect of voltage transients and noise. A manually operated power control and display (ABB1) plug-in circuit pack controls the application and removal of –48 volt power to a 133A DC-to-DC +5 volt power converter. See Figures 12, 13, and 14 for generics 1, 2, and 3, respectively.

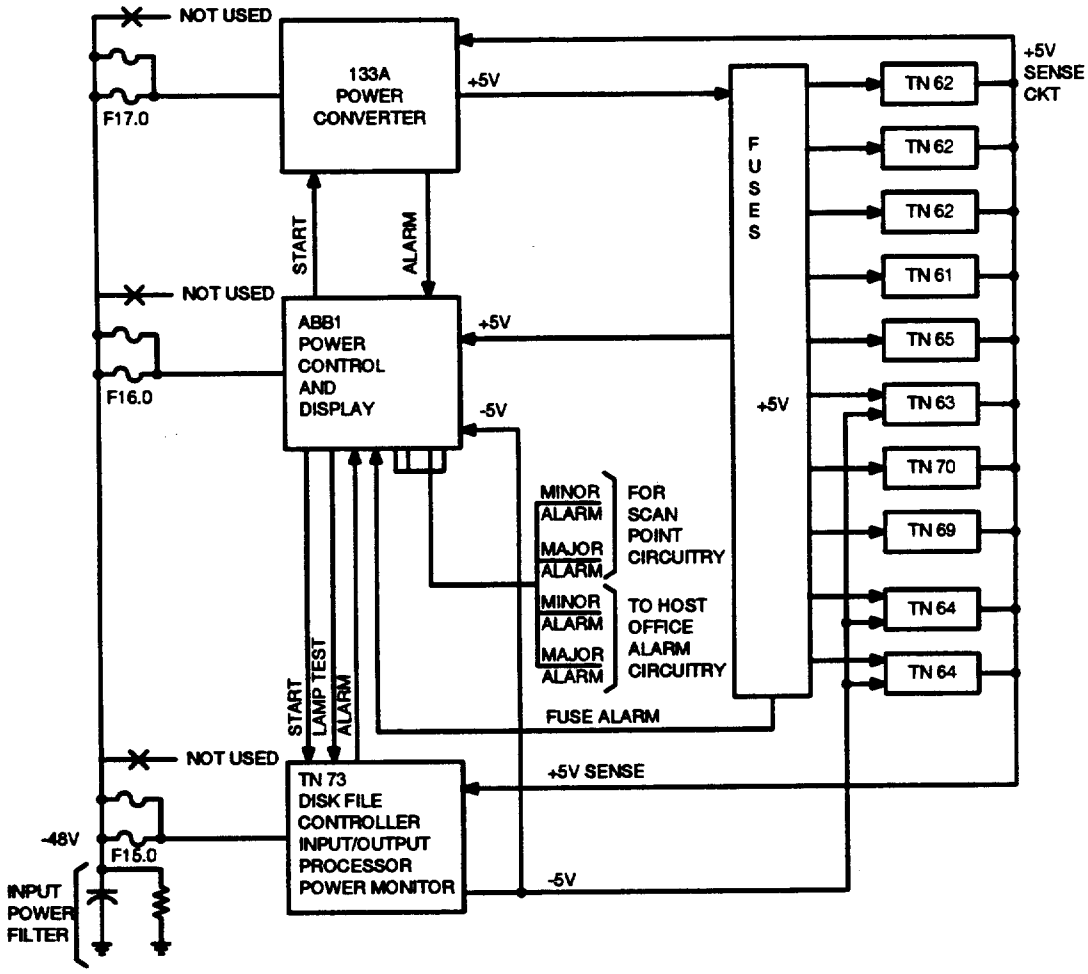


Figure 12. Disk File Controller Unit Power and Alarm Circuit (Generic 1)

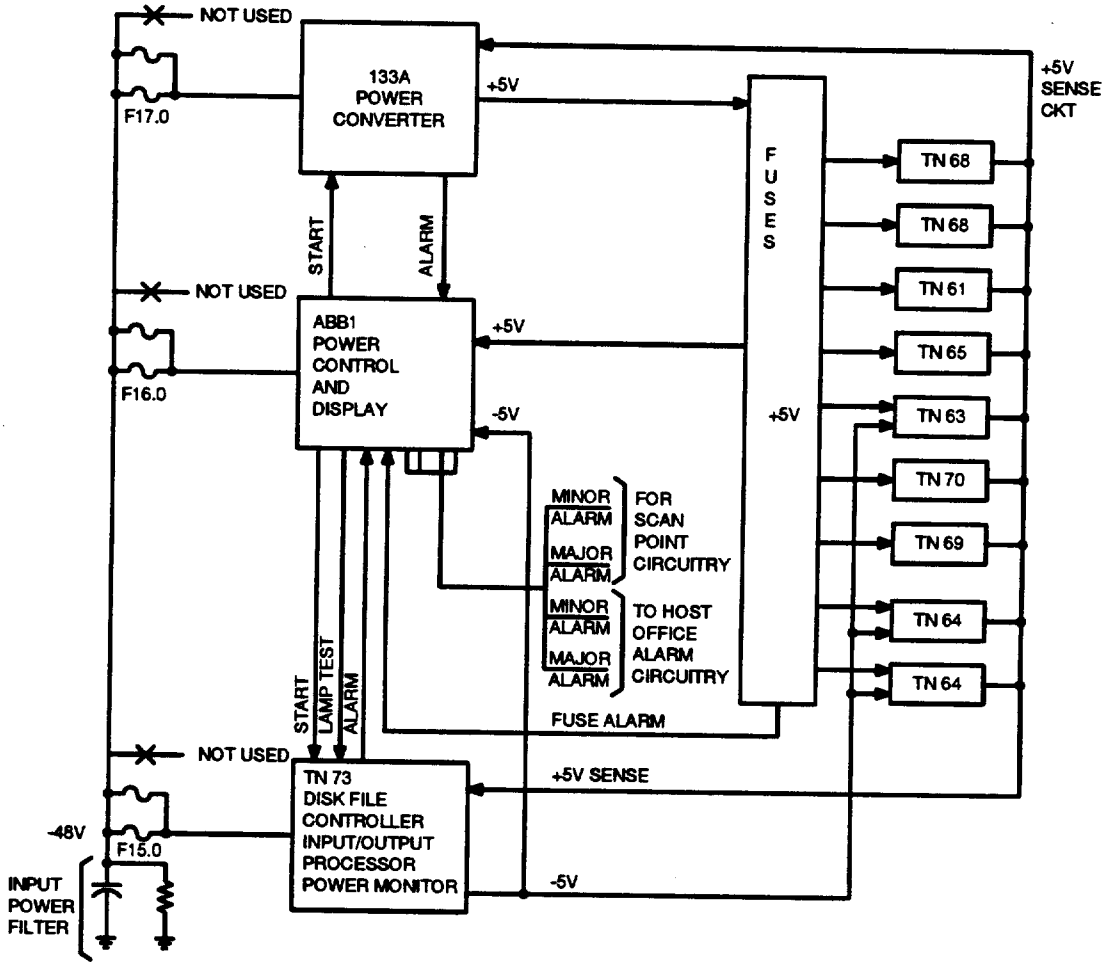


Figure 13. Disk File Controller Unit Power and Alarm Circuit (Generic 2)

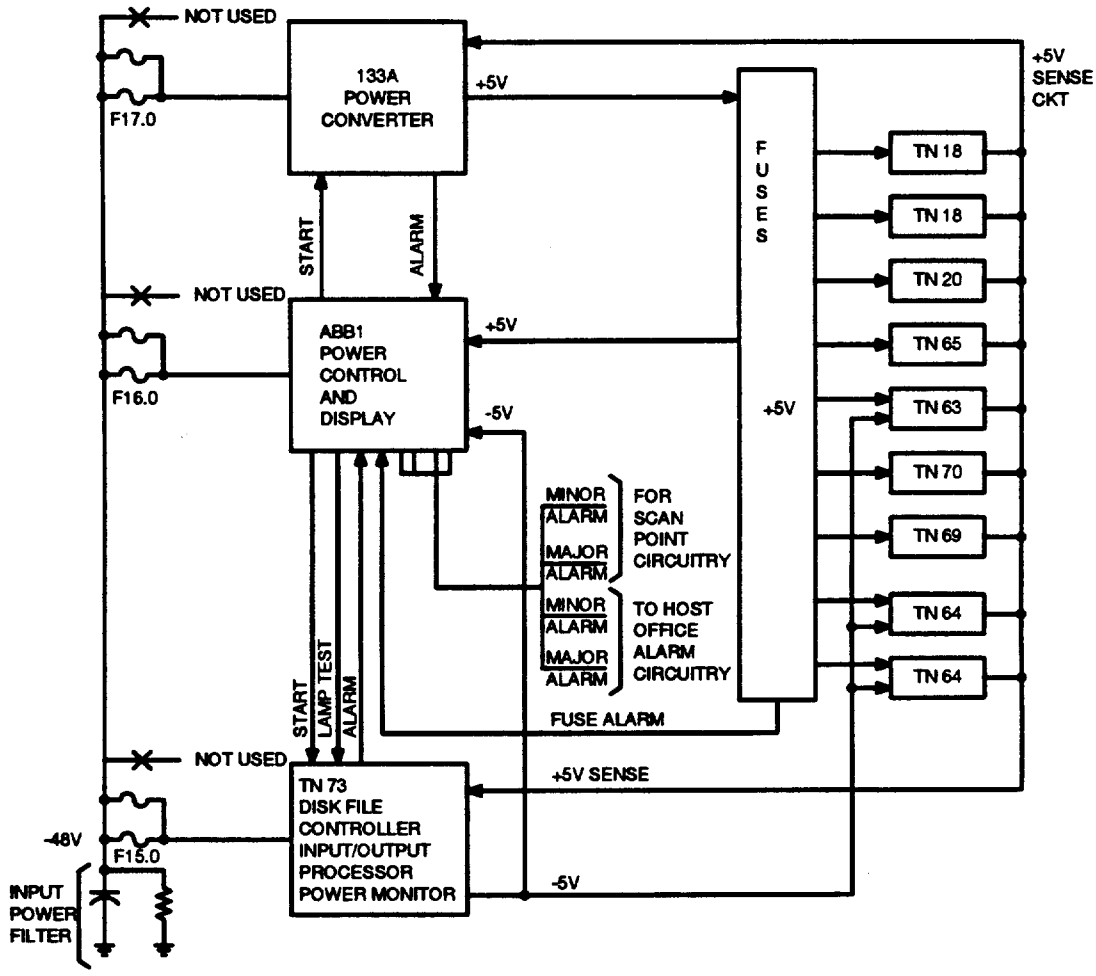
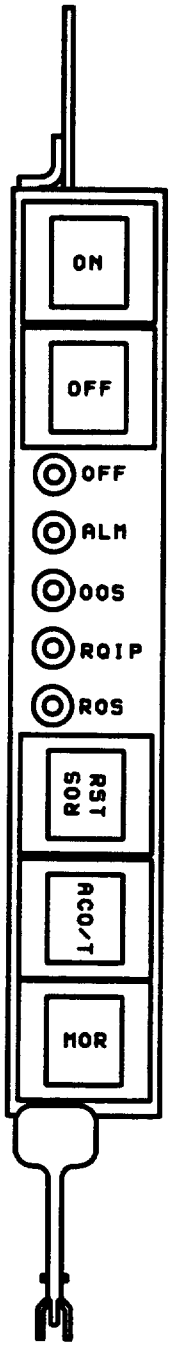


Figure 14. Disk File Controller Unit Power and Alarm Circuit (Generic 3)

B. Power Control

6.02 An ABB1 power control and display circuit pack controls the application and removal of –48 volt power to a 133A power converter (–48 volts to +5 volts) and the TN 73 DFC power monitor circuit pack. The power monitor circuit pack receives –48 volts and produces –5 volts unfused power for the MHD control and MHDD/C circuit packs via a low current converter.

6.03 The ABB1 (Figure 15) contains switches to apply and remove power (ON/OFF), request out of service/request to restore (ROS/RST), lamp test/retire major alarm (ACO/T), and manual override (MOR). The light-emitting diodes (LEDs) on the ABB1 indicate power off (OFF), alarm condition (ALM), out of service (OOS), request in process (RQIP), and request out of service (ROS).



LEGEND:

ACO/T	- ALARM CUT OFF/TEST
ALM	- ALARM
MOR	- MANUAL OVERRIDE
OOS	- OUT OF SERVICE
ROS	- REQUEST OUT OF SERVICE
ROS/RST	- REQUEST OUT OF SERVICE/ RESTORE TO SERVICE
RQIP	- REQUEST IN PROGRESS

Figure 15. ABB1 Front Panel

7. Power Alarms

A. Power Monitor Circuit Pack

7.01 In addition to supplying –5 volt power to the MHD control and MHDD/C, the power monitor circuit pack contains circuitry for monitoring the following:

(a) +5 volt fuse failure

(b) +5 volt output out of tolerance from 133A power converter

(c) –5 volt output out-of-tolerance condition from converter on TN 73.

7.02 The LED lamps on the front panel of the power monitor circuit pack provide the following:

(a) CR16 +5 volt circuit pack monitor input not present

(b) CR19 –5 volt converter output out of tolerance

(c) CR17 +5 volt from converter out of tolerance.

There are unused LED indicators on the front panel of the power monitor circuit pack; however, all LEDs are tested when the lamp test switch on the ABB1 power control and display circuit pack is operated. The lamp test also causes all the LEDs on the ABB1 to light.

B. Visual Fuse Alarms

7.03 Each load-carrying fuse on the DFC has a low current pilot fuse wired in parallel. Each pilot fuse contains an indicator which protrudes through the fuse cap when the fuse has "blown." Pilot fuses F15.1, F16.1, and F17.1 (–48 volt) alarm outputs are not used as their alarm functions are provided by ABB1.

C. 133A Power Converter Alarm

7.04 The 133A power converter provides a relay closure to the power control switch for the following conditions:

- Excessive output current
- Output voltage too high
- Output voltage too low
- Low –48 volt input voltage.

A LED on the face of the power converter lights for any of the above alarm conditions.

8. Glossary of Terms

8.01 Listed below is a brief description of the most commonly used terms in this practice:

Byte—Eight data and one odd parity bit.

Central Control—Control practice of computer. It consists of control circuitry, arithmetic unit, rotate mask unit, general and special register, maintenance channel, store address translator circuit, and optional cache memory unit.

Control Unit—That part of the computer which is switched in and out of service as a unit. The CU includes a central control (CC), main store (MAS), DMA unit, input/output (I/O) channels (CHs), and control power unit (CPU).

Disk File Controller—Interfaces to a DSCH and to disk drives. The DFC includes a peripheral interface controller and a MHD interface.

Dual Serial Channel—Provides a 32-bit DC signal interface to the DFC utilizing two bidirectional serial data paths.

Duplex Computer—Consists of duplicated CUs interconnected via each maintenance channel and all peripheral hardware required for system operation.

Duplex Dual Serial Bus Selector—Provides an interface for two DSCH to a DFC.

On-Line—A CU is on-line when it is in active control of the system configuration and execution.

Pilot Fuse—A low current indicating type fuse wired in parallel with a higher current load bearing fuse.

9. Acronyms and Abbreviations

9.01 The following is a list of acronyms and abbreviations used in this practice.

ACO/T	Alarm Cutoff/Test
ALM	Alarm
ALU	Arithmetic Logic Unit
BIC	Bus Interface Controller
CC	Central Control
CCU	Central Control Unit

CH	Channel
CU	Central Unit
DDSBS	Duplex Dual Serial Bus Selector
DFC	Disk File Controller
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DSCH	Dual Serial Channel
ECC	Error Correction Code
FIFO	First In First Out
I/O	Input/Output
LED	Light Emitting Diode
MAS	Main Store
MHD	Moving Head Disk
MHDD/C	Moving Head Disk Data Clock
MOR	Manual Override
OOS	Out of Service
PD	Power Distribution
PDF	Power Distribution Frame
PIC	Peripheral Interface Controller
PSDI	Parallel Serial Data Interface
RAM	Random Access Memory
PROM	Programmable Read Only Memory
ROS	Request Out Of Service
RQIP	Request In Progress
RSI	RS232 Interface
RST	Request Restore
SCSI	Small Computer System Interface
SMD	Storage Module Drive
TTL	Transistor-Transistor Logic

How Are We Doing?

Document Title: AT&T 3B20D Model 1 Computer Storage Module Drive Disk File Controller Description and Theory of Operation

Document No.: AT&T 254-301-215 Issue Number: 4 Publication Date: February 1992

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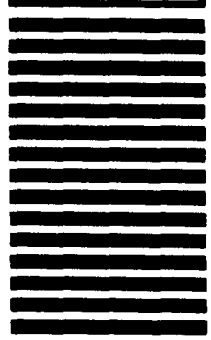

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