TEST EQUIPMENT
DESCRIPTION
3B20D MODEL 1 PROCESSOR

CONTENTS PAGE

CONTENTS PAGE

Figures

Tables

1. GENERAL

1.01 ▶This section describes the test equipment/functions necessary to maintain the 3B 3B20 duplex (3B20D), Model 1 processor. The 3B20D Model 1 processor hereinafter referred to as 3B20D1.◀ It is intended to familiarize the reader with the test equipment available for monitoring and testing the 3B20D1. The type of testing performed generally consists of system status verification and operations involving software diagnostics. Diagnostics are input via a terminal, or automatically invoked by software-controlled verification maintenance procedures.

1.02 This section is reissued to include changes brought about by duplex multi-environment real time (DMERT) operating system generic program PG-4C004 (Generic 2). Revision arrows are used to emphasize the more significant changes. The specific reasons for this reissue are as follows:

(a) To change the title

(b) To make changes where appropriate to indicate there are two models of the 3B processor

(c) To make correction to Fig. 1 (3B20D1 Processor Maintenance Craft Interface)

(d) To add descriptions of field test set (FTS) and field test unit (FTU)

(e) To delete Tables A (Abbreviations and Acronyms) and B (Test Equipment of 3B Processor)

(f) To delete Fig. 4 (Input/Output Terminals — Typical Arrangement)

(g) To delete listing of references.

1.03 The test equipment required to support the operation and maintenance functions of the 3B20D1 consists not only of equipment installed within the 3B20D1, but also supplemental equipment brought into the office as required. The test equipment installed within the 3B20D1 consists generally of visual/audible indicators, and messages displayed via maintenance terminals. In the 3B20D1, test equipment may be placed into one of two categories:

- Test equipment that is internal to the 3B20D1.
- Test equipment that is external to the 3B20D1.

1.04 Test equipment/functions that are internal to the 3B20D1 includes the following:

- Software routines (diagnostics, status, error checking, etc)
- Input/output (TTY/video) terminal
- Power switch (ABB1)
- Emergency action interface (EAI).

1.05 Test equipment that is external to the 3B20D1 (may be located in the central office or shared among several 3B20D1s) includes the following:

- Micro level test set (MLTS)
- Oscilloscope (Tektronix 7000 Series)*
- ♦Field test unit (FTU).♦

*Equipment specified or its equivalent may be used.

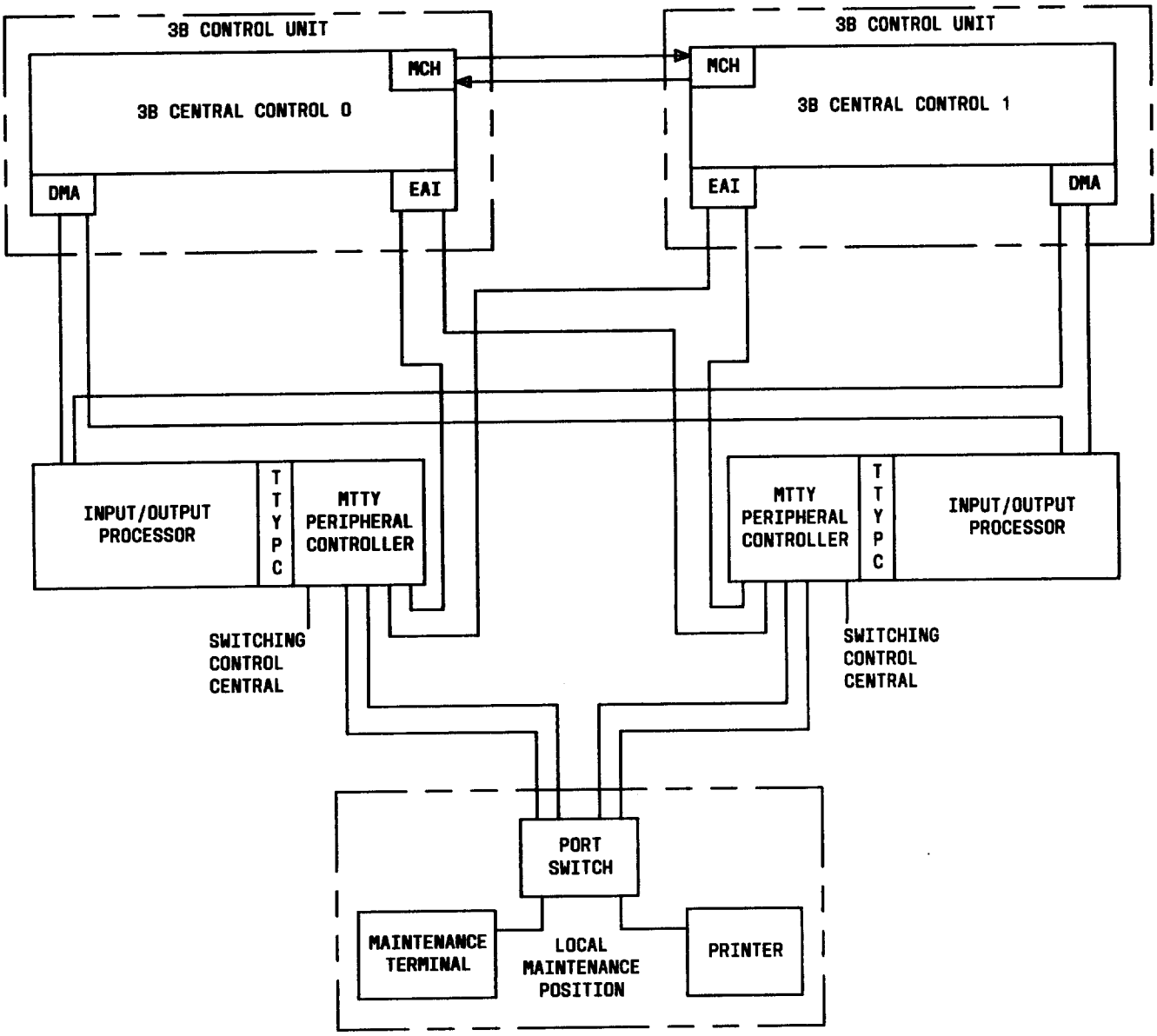
1.06 No test procedures are contained in this section. Refer to Sections 254-301-811 and 254-301-812 for routine and trouble clearing procedures, or refer to the documentation provided with the test equipment.

2. FUNCTIONAL DESCRIPTION

INTRODUCTION

2.01 Testing of the 3B20D1 may be initiated manually, or automatically via software routines. Manual testing must be performed using published test procedures. Testing results in verifying that equipment is operating properly, or is faulty. The local maintenance position (Fig. 1) provides the craft access to the 3B20D1 for control, monitoring, and testing the 3B20D1 and its application. A receive-only printer (ROP), is available to provide hard copy of system status or test results. Access can also be made from remote locations such as the switching control center (SCC). The maintenance access via the terminal interface is a prime tool for manually controlling, configuring, and recovering the system. The central focus of access is via the maintenance teletypewriter (terminal) peripheral controller (MTTYPC). The MTTYPC interfaces the maintenance terminal and ROP via the port switch unit. The MTTYPC also serves as an interface for the SCC and EAI.

2.02 Software routines are utilized to perform hardware status monitoring, to detect and correct software errors, and to record program status. The 3B20D1 central control (CC) is provided with a large set of self-checking logic to detect errors quickly. The error detection strategy uses parity checking, results matching, and duplication of logic. Most registers (but not all) have four parity bits (one for each byte of a data word). Parity is generated whenever data is moved through the arithmetic logic unit (ALU) and is checked whenever data is used. Detection of a parity error results in a control unit (CU) stop-and-switch action. Where parity checking is not used, duplication of logic circuitry is used (two ALUs for example) to avoid errors.



EAI - EMERGENCY ACTION INTERFACE
DMA - DIRECT MEMORY ACCESS
MCH - MAINTENANCE CHANNEL
MTTY - MAINTENANCE TELETYPEWRITER
SCC - SWITCHING CONTROL CENTER
TTYPC - TTY PERIPHERAL CONTROLLER

Fig. 1—3B20D1 Processor Maintenance Craft Interface

2.03 Hardware and system status information is provided by monitoring status registers and displays. The contents of the status registers may be retrieved and interpreted for the status of the hardware or system. For example, the hardware status register (HSR) contains hardware and control status information retrieved from the destination bus under microprogram control. The system status register (SSR) contains processor status information (configuration, maintenance, and recovery) and information sensed from scan points of certain manual switches. The status information gathered may indicate faulty equipment or system status. When faulty equipment is indicated, diagnostics are used to isolate the faulty unit to a replaceable plug-in unit.

TEST EQUIPMENT

A. Micro Level Test Set (MLTS)

2.04 The MLTS (Fig. 2) communicates with the 3B20D1 via the MLTS interface (UN16) located in the CC. The MLTS interface permits external access to the microinstruction structure, busses, and registers of 3B20D1. The MLTS also provides diagnostic access to SCC or another test facility. Communications between the 3B20D1 CC, the MLTS, and the craft person takes place via a serial channel and data set (Fig. 3) from the input/output terminal. The MLTS may be considered to be a low-level debugging tool and is useful for hardware, firmware, and software debugging, for initializations (such as from a deadstart), and for initial installation of the 3B20D1 Processor.

2.05 The MLTS functions are summarized below:

- Provides access to internal registers and buses.
- Provides control of the 3B20D1 clock. This permits the user to start, stop, or step through the execution of the addressable microinstructions.

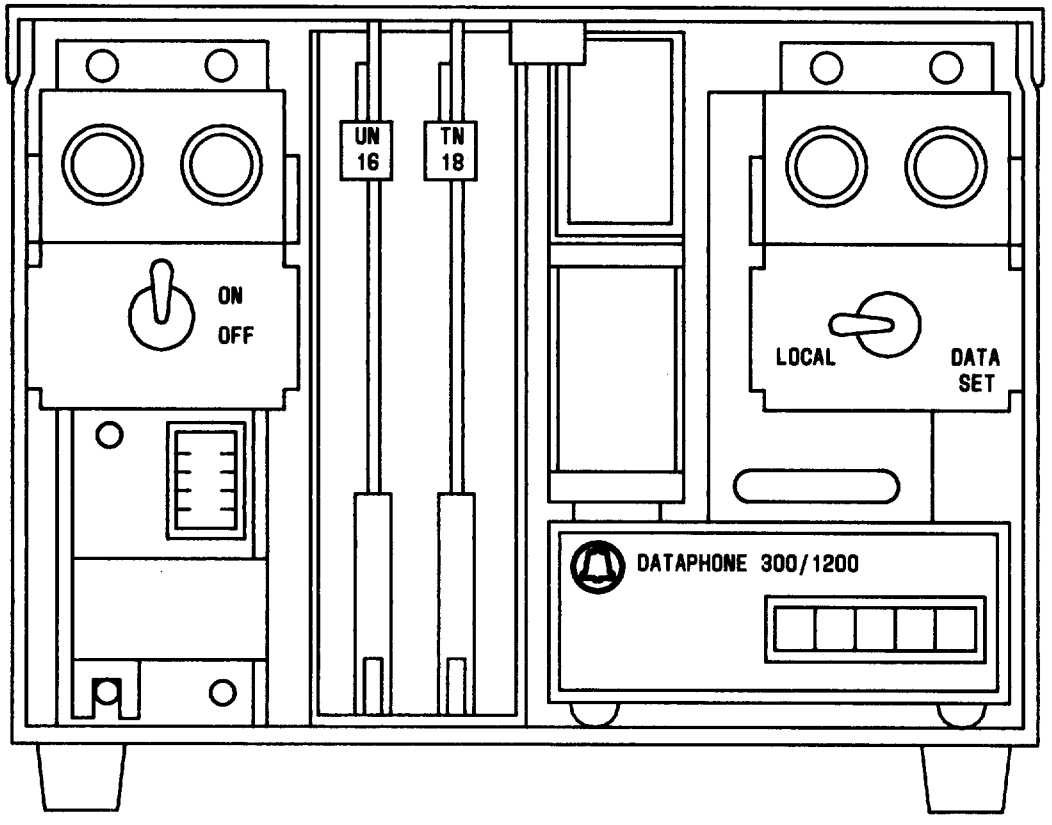


Fig. 2—Micro Level Test Set (MLTS)

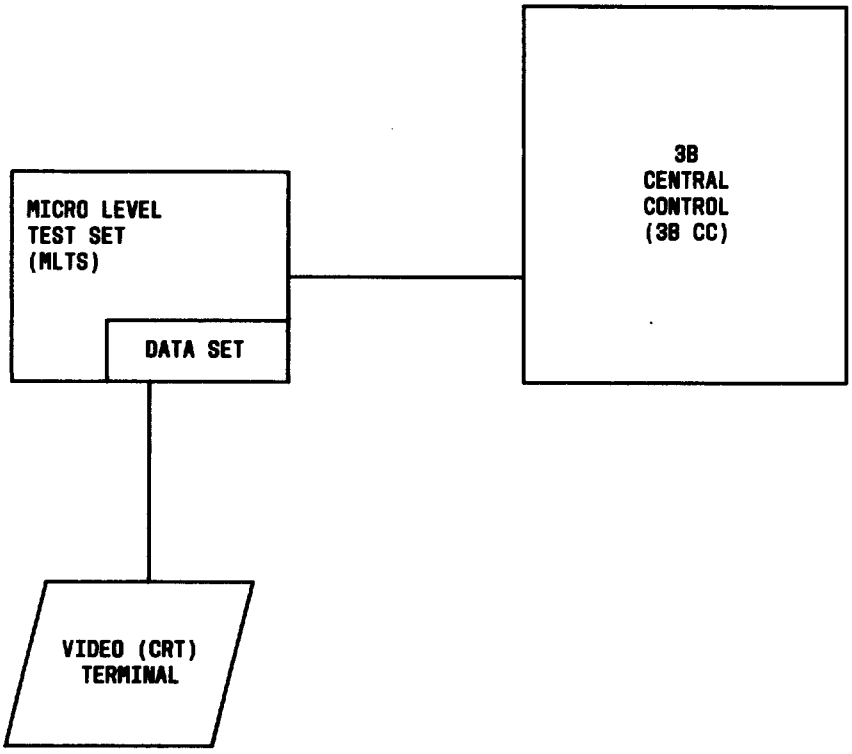


Fig. 3—Micro Level Test Set (MLTS) Application

- Provides control of the microsequencer. The user may instruct the processor to execute the next microinstruction.

- Provides basic commands so that basic functions may be executed as directed by the input commands.

Some of the typical MLTS commands are; STOP (stops 3B20D1 clock), RUN (starts clock), STEP n (runs clock long enough to execute n commands), GOTO address, D item (display item on terminal), and L item value (loads address or memory location with value). Using the MLTS commands, the user may load and edit memory locations, display register contents or bus signals, and control the execution of microinstruction, ie, control the 3B20D1.

◆B. Field Test Set (FTS)

2.06 The FTS is a software debugging tool that can monitor processes executing in the 3B20D2 at a field site without interrupting service. A FTS interfaces the 3B20D2 via a dual utility circuit (DUC). The DUC (UN61) monitors data flow between the CU and main memory. A DUC may be either permanently installed or installed only when its analysis features are required. When DUC is installed on a temporary basis, the equipment configuration database must be updated to reflect equipped or non-equipped status.◆

C. Input/Output (TTY/Video) Terminal

2.07 The maintenance terminal is the primary craft interface with the 3B20D1. The terminal provides the means for communicating with the 3B20D1 via input/output messages. The maintenance terminal is used for manually requesting tests, diagnostics, and removal or restoration of equipment from or to service. The maintenance terminal also receives response messages from the 3B20D1.

The terminal remains operational (via the MTTYPC) even though outages may occur in other parts of the system. Each MTTYPC contains a microprocessor programmed to oversee its ports in the event of CU outages or input/output processor (IOP) failures. This permits craft interface capability when the sys-

tem is not operational. A receive-only printer (ROP) is provided for obtaining hardcopy printouts of messages and status reports. For specific details concerning the terminal input/output message formats and details refer to the appropriate input/output message manuals and to the Trouble Locating Manual (TLM).

D. Power Switch (ABB1)

2.08 The ABB1 Power Switch (Fig. 4) controls the application and removal of power from an associated unit. The functions that may be accomplished via the ABB1 switch are:

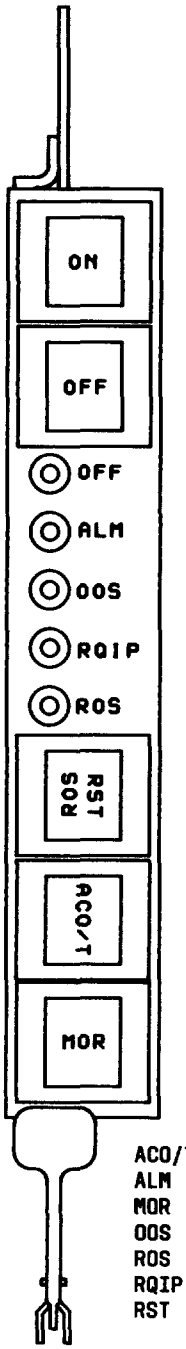
- Power-up or power-down an associated unit
- Initiate a request to remove or restore a unit to service
- Test indicator light-emitting diodes (LEDs) on the ABB1 switch, and retire (cut off) a major alarm initiated from the associated unit.

The functions of the switches and indicators of the ABB1 switch are summarized in Table A. Two scan points (Request out of Service or X and Power Alarm or Y), two alarm points (MJ and MN), and two signal distribute points (OOS and RQIP) are provided. The scan and alarm point states are summarized in Table B. The signal distribute point states are summarized in Table C.

2.09 Input voltages to the ABB1 switch are -48 volts from the office supply, and +5 volts from a dc-to-dc converter.

E. Emergency Action Interface (EAI)

2.10 The EAI (Fig.1) provides access to the 3B20D1 via the system status register (SSR). The EAI, which is microprocessor controlled, can set or clear control bits of the SSR, and can read status bits of the SSR. The EAI may be used to force CU configurations, to select and initiate various levels of recovery, to initialize hardware, to disable check circuits, and to provide certain CU status information. Commands sent from the MTTYPC to the EAI cause bits to be set or cleared in the SSR which result in certain EAI functions being performed. The SSR bits are examined and, by being either set or cleared, cause certain responses to be displayed on the maintenance terminal.



ACO/T LAMP TEST/RETIRE MAJOR ALARM
ALM ALARM
MOR MANUAL OVERRIDE
OOS OUT OF SERVICE
ROS REQUEST OUT OF SERVICE
RQIP REQUEST IN PROGRESS
RST REQUEST RESTORE

Fig. 4—Power Control Switch (ABB1) Front Panel

TABLE A

POWER CONTROL SWITCH (ABB1)
SWITCH/INDICATOR FUNCTIONS

SWITCH/INDICATOR	FUNCTION
ON (green)	Initiates power-up sequence when ACO/T is not in ACO (retire alarm) state.
OFF (red)	Initiates power-down sequence when the associated unit is out of service. An electrical interlock prohibits a power-down unless an out-of-service request has been granted.
ROS/RST (yellow)	Request the associated unit to be taken out of service and illuminates the ROS LED. If the request is granted, RQIP lights, otherwise RQIP flashes for a short period of time. When in the RST (request restore) position, the unit is requested to be restored to service.
ACO/T (white)	Depressing the ACO/T (alarm cut-off/test) switch silences the office major alarm and lights (test) all LEDs.
MOR (red)	Initiates an emergency power-down sequence when the MOR (manual override) and the OFF switches are depressed simultaneously. The interlock between the OFF switch and the unit out-of-service distribute point overridden to permit the power-down request.
OFF (red)	The red OFF LED is lit when the converter is in the power-off state and is extinguished when the converter is in the power-up state.
ALM (red)	The red ALM LED is lit when a power-related fault is present.
OOS (yellow)	The yellow OOS LED is lit when the associated unit is OOS. The OOS LED is activated via the OOS signal-distribute point.
RQIP (green)	The green RQIP (request-in progress) LED is lit to indicate that a request has been rceived to take the associatd unit out of service or to restore the unit to service. The RQIP LED flahses if the request is denied. The RQIP is activated via the RQIP signal-distribute point.
ROS (green)	The green ROS LED is lit when the ROS/RST switch is in the ROS position and is extinguished when the switch is in the RST position.

TABLE B

SCAN AND ALARM POINT STATES

CONDITON	X (REQUEST OUT OF SERVICE)	Y (POWER ALARM)	MJ (MAJOR)	MN (MINOR)
Normal in service	0	0	0	0
Request out of service (ROS)	1	0	0	0
Manual power off	1	1	0	0
Automatic power off or input -48V not present	1	1	1	0
Coverter power on with major fault	0	1	1	0
Converter power on with minor fault	0	1	0	1

TABLE C

SIGNAL DISTRIBUTE POINT STATES

CONDITON	RQIP	OOS
Normal in service	0	0
Remove from service or restore to service requested with dispositon pending	1	0
Request out of service (ROS) denied	FLASH	0
Diagnostic failure after a restore-to-service request (OOS lights)	FLASH	1
System grants out-of-service request (software requested)	0	1

2.11 Upon receipt of the appropriate command, the EAI assumes control of the maintenance and processor and enters the emergency action mode (this mode may be entered automatically if the 3B20D1 fails). In this mode, a special display is shown on the maintenance terminal and craft response (via the maintenance terminal) is dependent upon the data displayed. The display shows the state of the EAI functions and certain 3B20D1 states, such as RUN, ACTIVE, and FORCED. Indicators (LEDs) on the EAI indicate certain states or modes of the processor. The indicator functions are described in Table D. The EAI functions are described briefly in the following paragraphs.

(a) ***Force Primary Boot Device:*** The processor boots on its primary boot device.

(b) ***Force Secondary Boot Device:*** The processor boots on its secondary boot device.

(c) ***Force Processor On-Line:*** The selected processor is forced on-line. If successfully forced on-line, the ACTIVE or RUN indicators for the processor will be displayed on the terminal.

(d) ***Disable Timer:*** The sanity timer for the associated processor is disabled. Interrupts due to timer failures cannot occur.

(e) ***Maintenance Reset Function (MRF):*** The EAI circuit issues an MRF to the processor and causes an initialization of the hardware, software (DMERT Operating System), and any real-time process executing under the operating system. A system bootstrap may occur if the boot option bit is active in the SSR during the initialization.

(f) ***Input Parameter Buffer (IPB):*** Sixty-four parameter bits are sent to the EAI to indicate initialization levels, inhibit functions, and configuration functions for DMERT or the application.

(g) ***Inhibit Hardware Checks:*** Switching to the off-line processor is inhibited for errors detected for such things as parity, clock checks, My Store Error A, main store time-out, data manipulation unit error, or store address controller error.

(h) ***Output Processor Recovery Message (PRM):*** The EAI sends 64 bits of information relating to processor recovery actions during an initialization sequence. This includes the current initialization level and the success or failure of the initialization.

(i) ***Enable Backup Root File System Boot:*** The standard software boot is executed from the ROOT file system section of the boot device.

(j) ***Enable Minimum Configuration (nonapplication) Boot):*** The processor boots with the software configuration that is only needed to support the core of the processor. This includes software for the disk file, TTY communications, and processor microcode.

(k) ***Output Status:*** The emergency action status is generated from the EAI circuit to the MTTYPC. The MTTYPC updates its internal status tables which in turn updates the EAI display information on the video terminal display.

(l) ***Clear Emergency Action Functional:*** The active emergency action commands being generated by the EAI are cleared.

(m) ***Initialize TTY Channel:*** The TTY portion of the operating system, including hardware and software, is completely initialized.

F. Oscilloscope

2.12 The oscilloscope used to test the 3B20D1 circuitry should have the following capabilities:

- Dual trace
- Vertical deflection—DC to 50 MHz bandwith
- Vertical deflection—Rise time 7 nanoseconds
- Vertical deflection—Volts/division range from 5 mV/division to 5V/division
- Vertical deflection—Accuracy 3 percent
- Horizontal deflection-Time base 0.05 microsecond/division to 0.5 second/division
- Horizontal deflection—X10 MAG to extend sweep rate to 5 nonoseconds/division
- Horizontal deflection—Delay sweep
- Horizontal deflection—Trigger modes

TABLE D

EMERGENCY ACTION INTERFACE UNIT
INDICATORS AND FUNCTIONS

INDICATOR	FUNCTION
RUN	Indicates that the CU is executing main store instructions
ACTIVE	Indicates that CU is on-line (active)
EMERGENCY ACTION ENABLE	Indicates that this CU is in the emergency action mode, enabling control of other EAI functions
FORCED ON-LINE	Indicates that this CU has been forced on-line (regardless of attempts by software to switch) and the other CU is forced off-line.
FORCED OFF-LINE	Indicates that this CU has been forced into the off-line mode, and the other CU is concurrently on-line
STATUS	A 1-digit hexadecimal display which indicates the low 4 bits of the system status register (SSR) as written to the EAI.

- Horizontal deflection—Accuracy 3 percent
- Calibrated output to check scope
- Accessories—Probes (X1 and X10).

The oscilloscope requires a power source of 115 volts ac, 60 Hz for operation.

▶G. Field Test Unit

2.13 The FTU (Fig. 5) or disk drive exerciser is a portable unit housed in a brushed aluminum attache case with protective cover and carrying handle and weighs 25 pounds. The main feature of the FTU is its 8085 microprocessor based controller. The FTU contains several stored diagnostic programs which are resident in the units firmware, and through its alphanumeric key pad, program mode switch and LED display, programs can be created.

2.14 The primary purpose of the FTU is to functionally exercise and test the 300 megabyte disk drive which has a storage module drive (SMD) interface. The FTU supports maintenance of the disk memories in the off-line stand-alone mode. Some of the features and tasks which the FTU is capable of performing are as follows:

- Verification of troubles reported through system diagnostics
- Monitoring of disk drive fault indicators
- Verifies that repairs are correctly performed
- Executes stored disk drive verification routines
- Programmability to allow custom test routines

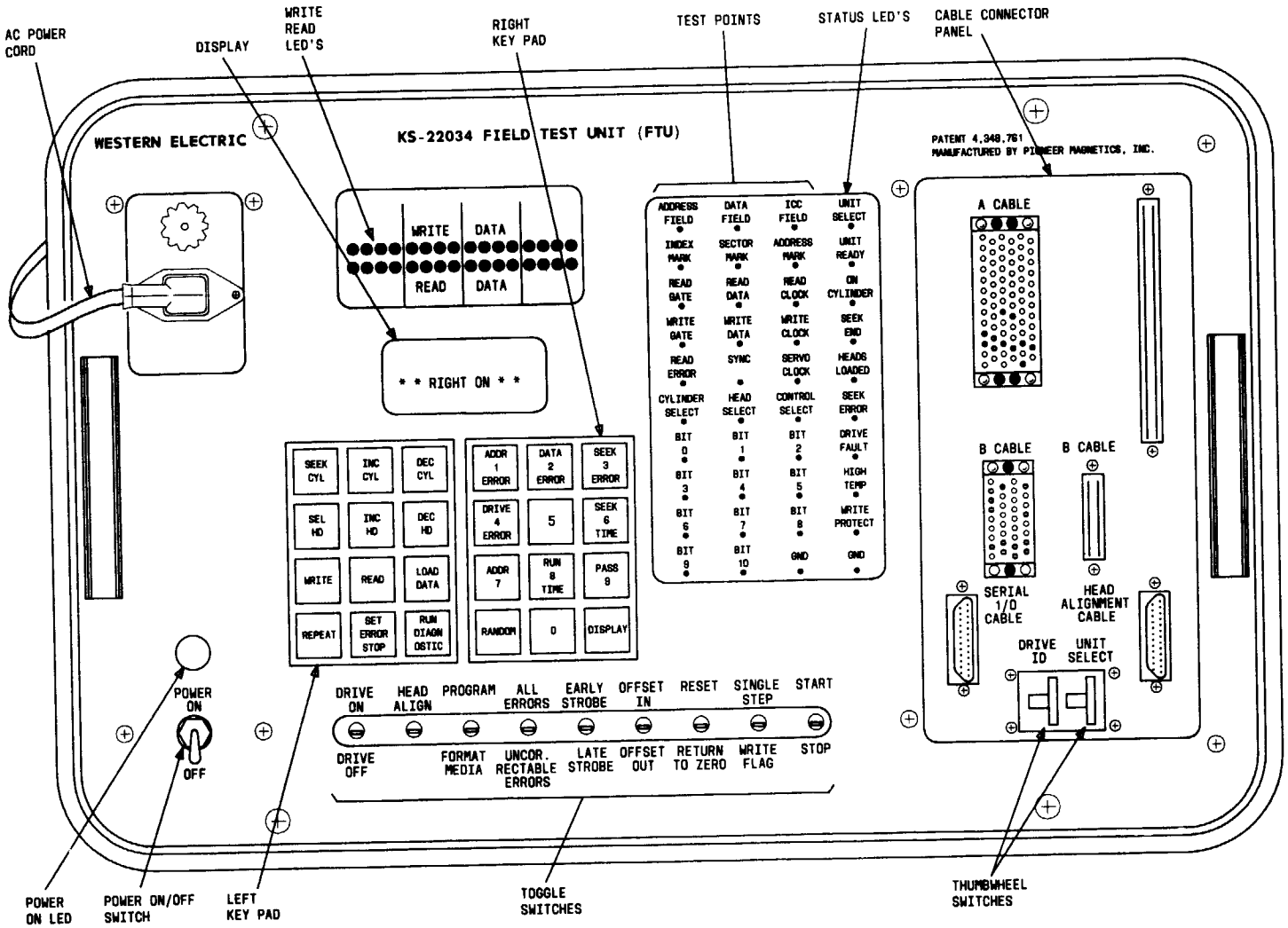


Fig. 5—Field Test Unit

- Head alignement of disk drives within micro-inches
- Verification of disk pack integrity
- Self-test diagnostics
- Performs simulated dynamic testing on an off-line basis.

3. POWER

A. Test Equipment Internal to the 3B Processor

3.01 The internal test equipment is normally supplied with power from the frame on which the equipment is mounted. Power is applied to (or removed from) circuit packs in the 3B20D1 via the ABB1 power switch. Five indicator lights (or LEDs) on the front of the ABB1 switch indicate the state of the processor unit being controlled. The lights are labeled (from top to bottom) OFF, ALM (alarm), OOS (out of service), RQIP (request in process), and ROS (request out of service. Five pushbutton switches provide power control. The switches are located on the front of the ABB1 switch and are labeled (from top to bottom) ON, OFF, ROS/RST (request out of service/request restore service), ACO/T (retire alarm or alarm cutoff/test lamps), and MOR (manual override). Procedures are provided in Task Oriented Practice, Section 254-301-811 for the proper application/removal of power.

3.02 The frame that provides the power also supplies the filtering and fusing as required for proper operation of the equipment.

3.03 Alarms are provided by the frame supplying the power to the test equipment.

B. Test Equipment External to the 3B20D1

3.04 The external test equipment is provided operating power from one of the following sources:

- Self-contained battery
- Circuit under test
- 115 volts ac 60 Hz power
- Local office battery (-48 volts).

4. MAINTENANCE

4.01 The test equipment internal to the 3B20D1 may be checked on a periodic basis by software routines. These routines may also be initiated manually via the maintenance terminal. Refer to the input/output message manuals for details concerning the proper format and details of the messages. When a malfunction is suspected, software routines verify proper operation or detect faulty equipment.

4.02 The external test equipment should be checked as recommended by the manufactures or when a malfunction is suspected. Some test equipment is equipped with internal calibration or diagnostic features. Proper operation may be checked by performing calibration or diagnostic procedures provided with the test equipment.

5. GLOSSARY

5.01 A glossary of terms is provided to aid in the understanding of technical words or terms used in this section.

Diagnostics—Specially coded programs which direct the hardware within a circuit to perform in a required manner and checks that the performance is correct.

Fault—A condition which causes a device, a component, or an element to fail to perform in a required manner.

Initialization—An action taken to provide the system with a known good and operating configuration.

Microcontrol (MC)—The MC portion of the CC controls the sequencing of the MIS and decoding of the microinstructions, providing control signals to the CC circuitry.

Microinstruction—A fixed, read-only instruction which is used to form microinstruction sequences that are permanently stored in a read-only memory. The microinstruction sequences are used to implement the 3A CC instruction set and basic control functions.

Parity—A binary digit appended to an array of bits to make the sum of all the bits always odd (odd parity) or always even (even parity).

Routine—A series of computer instructions which performs a specific task.

6. ABBREVIATIONS

6.01 The following is a list of abbreviations used in this section and the words they represent.

ABBREVIATION	TERM
ACO	Alarm Cut Off
ALM	Alarm
ALU	Arithmetic Logic Unit
CC	Central Control
CU	Control Unit
DMA	Direct Memory Access
EAI	Emergency Action Interface
FTS	Field Test Set
FTU	Field Test Unit
HSR	Hardware Status Register
IOP	Input/Output Processor
IPB	Input Parameter Buffer
LED	Light Emitting Diode
MAS	Main Store
MC	Microcontrol
MCH	Maintenance Channel
MJ	Major
MLTS	Micro Level Test Set
MN	Minor
MOR	Manual Override
MRF	Maintenance Reset Function
MTTYPC	Maintenance Teletypewriter Peripheral Controller
OOS	Out of Service
PC	Peripheral Controller
PRM	Process Recovery Message
ROP	Receive-Only Printer
ROS	Request Out of Service
RQIP	Request in Progress
RST	Restore to Service
SCC	Switching Control Center
SMD	Storage Module Drive
SSR	System Status Register
TLM	Trouble Locating Manual