AT&T 3B20D Computer
General Description

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1. Overview

1.01 This practice provides a system-level description of the AT&T 3B20D Model 2 and Model 3 computers. The physical and functional descriptions are preceded by an overview of the system and its important features. A separate description of the fault- detection and maintenance capabilities is also included. Figure 1 shows one of the typical configurations for the 3B20D Model 2 computer. Figure 2 shows a minimum system configuration for the 3B20D Model 3 computer.

1.02 This practice is reissued to update information about the Small Computer System Interface (SCSI). The specific reasons for reissue are listed below:

(a) Add a new section - Small Computer System Interface Disk File Controller (SCSI-DFC)

(b) Add a new figure illustrating a typical new system configuration equipped with SCSI disk drives - Figure 6

(c) Add sentences and paragraphs where appropriate to clarify equipment differences between the 3B20D Model 2 and Model 3 computers

(d) Add new section in Part 3 entitled SCSI Disk Cabinet

(e) Add a new Figure in Part 3 for the SCSI disk cabinet - Figure 16

(f) Modify Figure 25 formerly Figure 23

(g) Modify Figure 26 formerly Figure 24

(h) Modify and change title of Figure 27 (formerly Figure 25) to SMD/SCSI DFC Co-Existence Diagram

(i) Modify Figure 28 formerly Figure 26

(j) Modify Figure 29 formerly Figure 27.

1.03 This practice contains no admonishments.

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1.07 Technical assistance for 3B20D Model 2 and Model 3 computers can be obtained by calling the Regional Technical Assistance Center at **1-800- 225-RTAC**. This telephone number is staffed 24 hours per day. During regular business hours, your call will be answered in your region. During evening and early morning hours, your call will be answered at Rolling Meadows, Illinois.

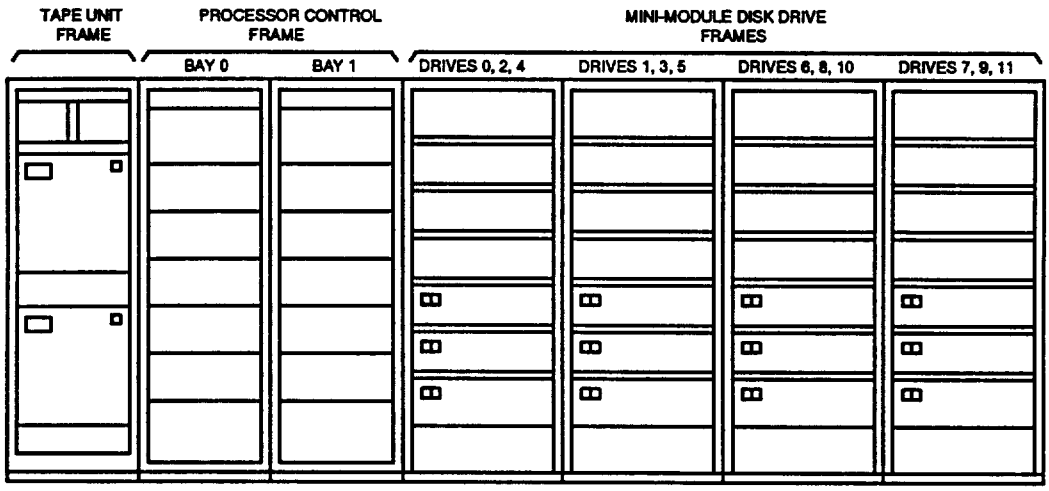

Figure 1. 3B20D Model 2 Computer (Example of a Typical Configuration)

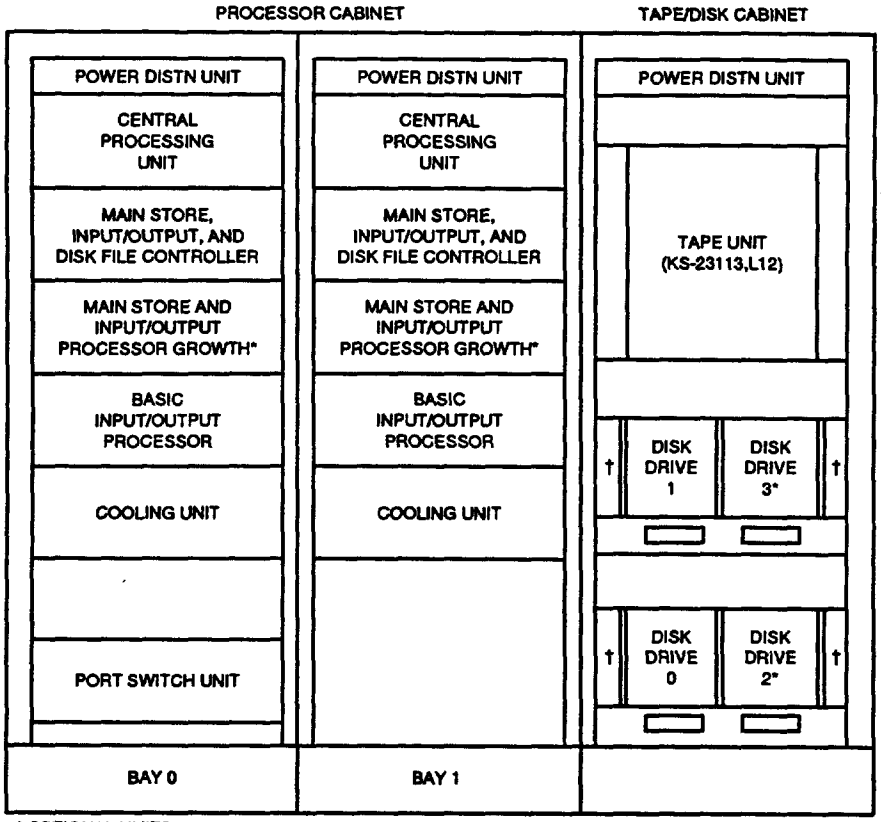

Figure 2. 3B20D Model 3 Computer (Minimum System Cabinet Configuration)

2. System Overview and Features

A. Physical Space

2.01 The 3B20D Model 2 computer's equipment is housed on frames, while the 3B20D Model 3 computer is contained in cabinets. Both the Model 2 and Model 3 computers require only a single double bay of equipment space. The Model 2 computer is contained on a double bay frame shown in Figure 3. All frames for the Model 2 computer are 7 feet tall, 2 feet 2 inches wide and 2 feet deep. The Model 3 computers are contained in double-bay cabinets. All cabinets are 6 feet 4 inches tall, 26 inches wide, and 30 inches deep. The cabinets are bolted together side by side (see Figure 2).

The minimum system shown in Figure 2 is shipped as a unit. Each cabinet is equipped with doors front and back, casters and insulating, nylon-tipped, adjustable leveling feet.

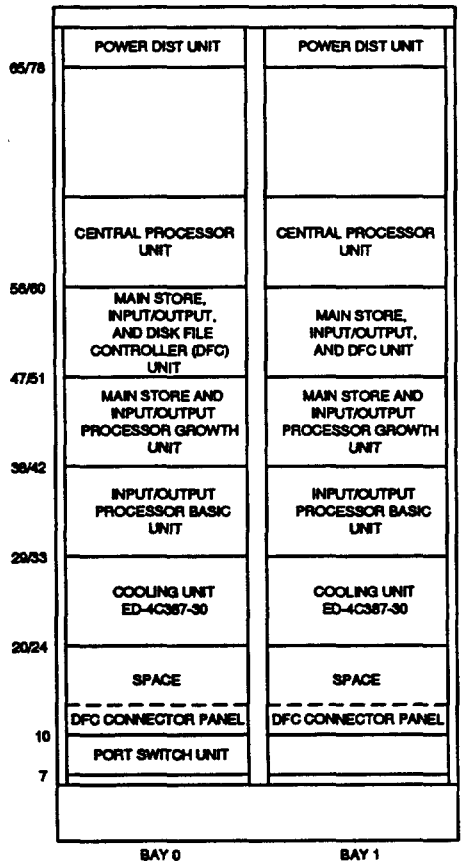

Figure 3. Processor Control Frame 3B20D Model 2 Computer

B. Duplex Reliability

2.02 The processor control frames/cabinet consists of two independent processors as shown in Figure 4. Extensive checking hardware, built into each computer, coordinates with software to detect a fault in the on-line computer as it occurs. If the on-line computer fails, the backup immediately takes over. The active computer keeps the main store (MAS) of the backup computer and associated disk storage up to date should a computer switch become necessary. Also, the input/output (I/O) system is configured so that peripheral devices can communicate over both computers I/O buses.

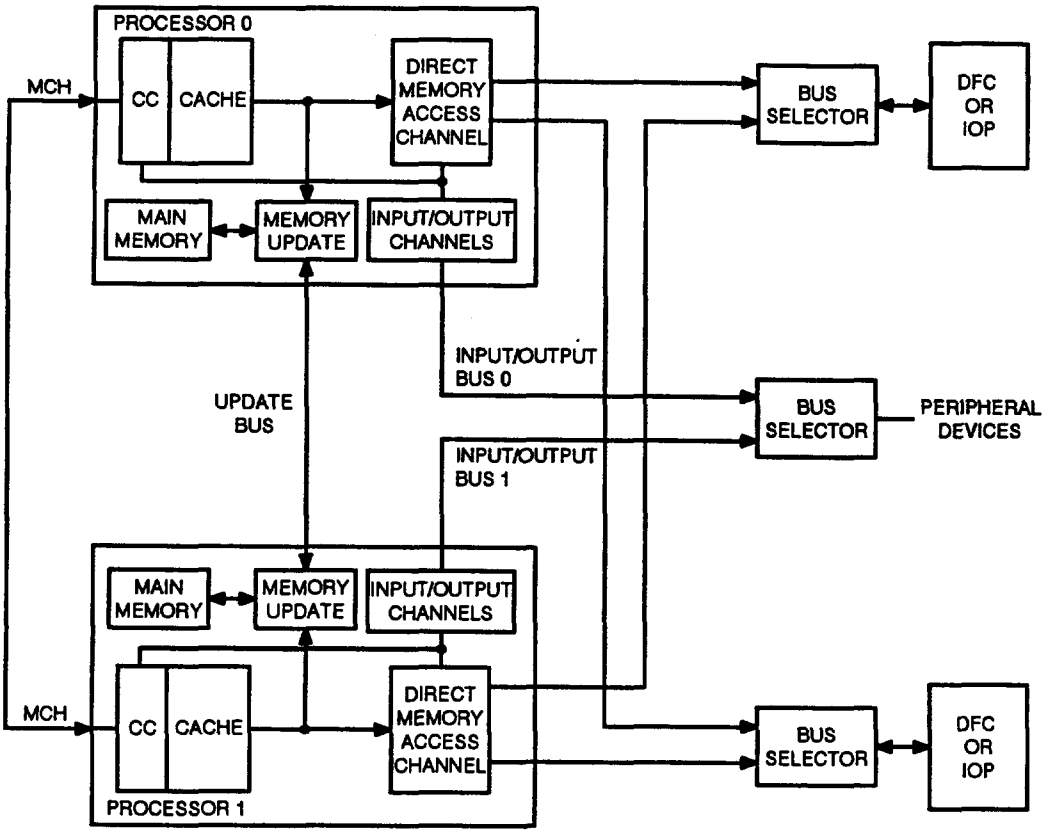

Figure 4. Duplex Operation

C. Extended Main Memory

2.03 The 32-bit word capability, use of microcode firmware, and bus arrangement make the computer a high-speed, efficient machine. The execution of each 32-bit instruction word fetched from main store is accomplished through a sequence of microinstructions (firmware). This reduces the number of program instructions to be developed and stored and allows a higher level programming language to further reduce programming effort.

2.04 Each computer uses a 40-bit, dynamic, volatile, random-access, semiconductor memory. The maximum memory capacity depends on the circuit pack option. The maximum capacity using the TN28 circuit packs is 16 Mbytes. Effective with *UNIX** RTR Operating System Release 1, the extended main memory (EMM) feature (using the TN56 circuit packs) increases the maximum capacity to 32 Mbytes. The memory (known as main store) is full-word (32 bits), half-word (16 bits), or byte (8 bits) addressable. Each stored 40-bit word includes eight Hamming bits in addition to the 32 data bits. The eight Hamming bits were generated from the data word and four parity bits by the main store. The main store access time is 850 ns. To increase real-time capabilities, an optional high- speed (250-ns) cache memory with 2K-word capacity can be used to store the most frequently read information.

D. Input/Output System Flexibility

2.05 Because the computer is intended to serve a wide range of applications, the I/O facilities were designed to be modular, flexible, and easy to modify. Two types of I/O channels can be connected. Programmed channels may be used with low-speed devices, such as teletypewriters and printers, that send and receive data one word or character at a time. Direct memory access (DMA) channels transfer large blocks of data to or from high-speed magnetic disk drives and similar devices that cannot be stopped at each character. The DMA channels are also used to control a large number of slower speed devices, such as teletypewriters, through special devices called I/O processors (IOPs).

2.06 The IOP is the most flexible of the peripheral devices. It acts as a remote "hub," connecting as many as 16 microprocessor-based peripheral controllers to the central processor unit (CPU). Each peripheral controller is programmed to handle up to four subdevices. This kind of distributed processing is part of what makes the computer so efficient and flexible. The peripheral controllers relieve the CPU of many tasks, and can be altered easily without affecting ongoing operations.

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* *UNIX* is a registered trademark of *UNIX* System Laboratories, INC.

E. Hardware Circuitry

2.07 The computer is built using a broad range of complex and high-performance integrated circuits. These integrated circuit devices are packaged and interconnected. They are contained in a dense, high-performance packaging system. This includes a substantial increase in the number of devices allowed per circuit pack and the number of contacts per pack.

F. Power System

2.08 The power system is electrically and physically superior to conventional designs. Instead of fuse arrangements that affect circuit impedance, a current programming method is used to protect backplane wiring against overcurrent damage.

3. Physical Description

3.01 Figure 1 shows a typical configuration of the AT&T 3B20D Model 2 computer. The double-bay processor control frame, four minimodule disk frames, and one high-speed tape unit frame are shown. The computer can be configured for up to eight moving head disk (MHD) frames or four minimodule disk frames. Up to four high-speed tape or tape/disk frames may be provided.

3.02 Figure 2 shows the minimum system configuration for the 3B20D Model 3 computer. Each cabinet has a floor cabling duct at the rear. Filtered air is circulated through the cabinets and is exhausted through the top. The minimum 3B20D Model 3 computer configuration consists of one double-bay processor cabinet containing the duplexed processors 0 and 1, one single-bay tape/disk cabinet containing one tape drive and two disk drives. Figure 2 shows four 340-Mbyte SMD type disk drives. Figure 5 shows a typical 3B20D Model 3 computer growth configuration. The peripheral interface cabinet is required for growth. This cabinet provides space for the addition of two basic IOP units and two growth IOP units. Basic units must be added before growth units.

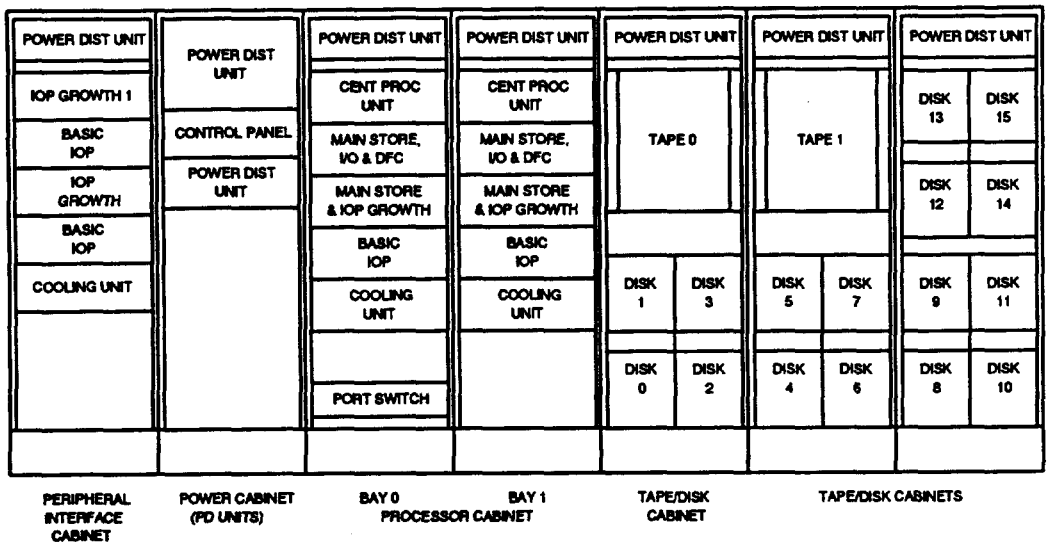


Figure 5. 3B20D Model 3 Computer Typical Growth Configuration

A. Very Large Main Memory (R6)

3.03 This feature supplies the 3B20D Model 2 and Model 3 computers with more virtual memory and fuller capabilities in using memory after retrofit to very large main memory (VLMM) (R6) has been made. It is also geared toward satisfying the current and future memory needs of customers.

3.04 Though some of the circuit packs in VLMM (R6) are downward compatible to EMM, both VLMM (R6) and EMM cannot exist at the same time.

3.05 The VLMM (R6) feature provides the user with 64 megabytes of virtual addressing memory and up to 32 megabytes (up to 64 megabytes as a growth option) of physical memory with DMA. Cache is provided on all memory to further enhance the memory use capabilities by reducing apparent access time of main store (MAS). Other capabilities and benefits of VLMM (R6) are:

- The larger virtual memory address space removes problems with process size. Since there is more physical memory, the number of processes placed in core is not a problem.
- Also, the VLMM (R6) features a 4K Cache.

Hardware Changes

3.06 The VLMM (R6) feature requires the following hardware changes:

- Backplane changes on the physical address bus to support the larger physical address (26 bits).
- The Store Address Controller (UN43 for R1) changes (to UN611 for R6) to support 64 megabytes addressing. Specific items expected to change are the Store Address Register (SAR) and Program Address (PA) layouts and their use.
- The Store Address Translator (UN45 for R1) which supports 64 Address Translator Buffer (ATB) entries for 16 megabytes of memory, will be changed (to UN612) in order to support ATB entries of 256 entries for 64 megabytes of memory and wider physical addresses for VLMM (R6).
- Writable microstore (UN248B) changes to increase memory for future product enhancements.
- The Main Store Update board (UN133 for R1) changes (to UN614 for R6) to support the wider address bus.
- The Direct Memory Access Controller (UN46 for R1 and UN614 for R6) changes an internal register and access privilege interpretation to support the Page Table Entry (PTE), relocation address field expansion and addresses 64 megabytes physical memory.
- The cache (UN10 and UN11 for R1) will be changed (to UN616 and UN617 for R6) to cover all physical memory and double its size.
- A new 4 megabyte memory array.
- The main store controller (UN59) changes to support 64 megabyte physical addressing and the new 4 megabyte memory array (UN618 for R6).
- The utility circuit (UN61 or UN21 for R1) changes (to UN615 for R6) to provide address matching and program transfer tracing based on a 26-bit address.
- The Microlevel Test Set (MLTS) control unit software (TN16) changes to properly access cache maintenance addresses.
- The CU microcode changes to support the new cache and memory spectrum.

3.07 One impact of the hardware is the extent to which the changed circuit packs will be downward compatible. Most of the packs will function in R1 with EMM but they will require software changes to R1 to be compatible. Though the function remains the same for all releases, the pack code does not remain the same.

Software Changes

3.08 The software consequences of VLMM (R6) are reflected on any product that addresses translation, or uses the modified software structures.

Which includes the following:

- Operating System - Which is mostly felt in the memory manager/kernel code and libraries, as well as certain structure layouts and system variable limits (for example, segment table entry, page table entry, segment base register and segment table size).

The memory audits are significantly impacted with the addition of VLMM (R6). Extension of the audits will also have to consider the timing implications of auditing larger or more memory resources.

Expected products requiring changes for VLMM (R6) within the operating system are kboot, 3bpmgr, libc and memory manager/kernel.

- Fault Recovery - This subsystem requires changes to expand the memory clearing currently done during bootstrap.
- Software Generation System - The need for a 26-bit address forces expansion of the immediate address fields for address modes 4 through 9.
- Field Update - This must change its relocation scheme to allow for the new relocation types.
- System Generation Programs - These products need changes for table expansion and page table use to support the feature.

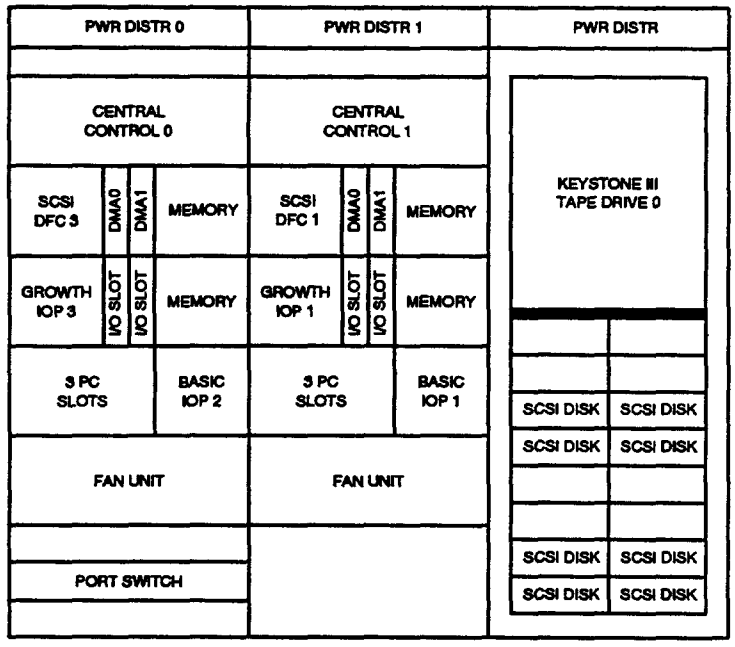
B. Small Computer System Interface (SCSI) Disk File Controller

3.09 The small computer system interface disk file controller (SCSI-DFC) (available beginning with Release 6) provides an alternate interface for the disk file system. The SCSI-DFC utilizes new circuit boards and the latest disk technology to provide increased disk storage capacity in a smaller, lower power disk unit. Disk drives are packaged in a disk unit package (DUP) which also contains a fan, power supply, and power switch.

3.10 The SCSI-DFC is available as a new start option in 3B20D Model 3 computers. Growth and conversion options are available in both Model 2 and Model 3 computers.

3.11 When SCSI is provided as a new start option, it will have a typical configuration as shown in Figure 6.

3.12 A new cabinet, the SCSI disk cabinet, is required. This cabinet is used to house the new SCSI disk drives and replaces the Tape/Disk Cabinet in new start systems.



Legend:

DFC - Disk File Controller
DMA - Direct Memory Access
IOP - Input/Output Processor
I/O - Input/Output
PWR DISTR - Power Distributor
SCSI - Small Computer System Interface

Figure 6. 3B20D Model 3 Computer — Typical New System Configuration Equipped with SCSI Disk Drives

C. Processor Control Frame/Cabinet

3.13 The processor control frame is a double-bay frame for the 3B20D Model 2 computer or a double bay cabinet for the 3B20D Model 3 computer. Each bay (0 and 1) houses an independent computer (one active and one standby).

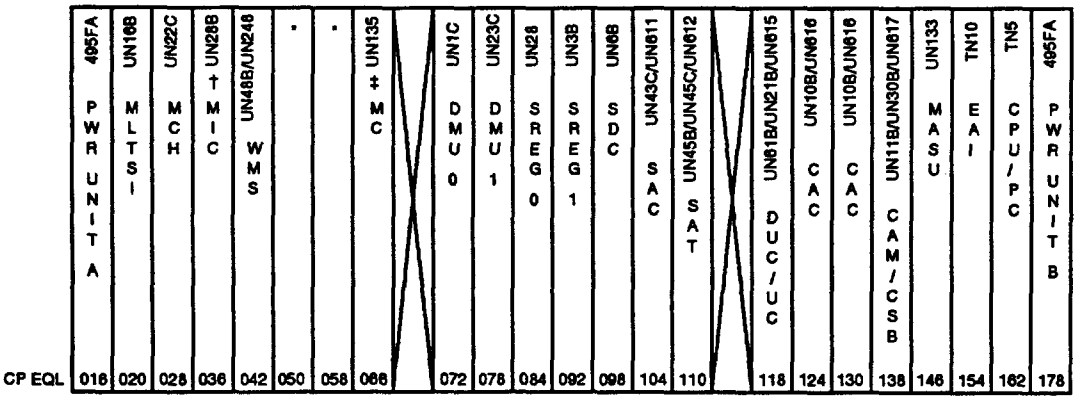
3.14 As shown in Figures 2 and 3, each computer in the processor control frame and the processor cabinet contains the following physical/functional units:

(a) **Central Processor Unit:** The central processor unit (CPU) (Figure 7) is comprised of two 495FA power converters and the following circuit packs:

- Microlevel test set interface—UN16B
- Maintenance channel—UN22C
- Programmable microstore—MC4C077A1B (UN28B for R1) and MC3T003A1 (UN28B for R6).

- Writable microstore—UN48B for R1 and UN248 for R6
- Microstore controller—MC4C076A1 (UN135)
- Data manipulation unit 0—(UN1C for R1 and UN608 for R6).
- Data manipulation unit 1— (UN23C for R1 and UN609 for R6)
- Special register 0—UN2B
- Special register 1—UN3B for R1 and UN3C for R6
- Store data control—UN6B
- Store address control—UN43C or UN43D (UN611 for R6) (used with EMM feature and VLMM
- Store address translator—UN45B or UN45C (UN612 for R6) Effective with UNIX RTR Operating System Release 1 for the 3B20D Model 2 and Model 3 computer.
- Utility circuit—UN21B/UN61B (UN615 for R6)
- Two cache memory controllers—UN10B, UN10C or UN616 (which is used with EMM and VLMM [R6])
- Cache memory—UN11B, UN11C or UN617 (which is used with EMM and VLMM [R6])
- Main store update—UN133, UN133B (used with extended main memory feature) or UN133C (used with very large main memory).
- Emergency action interface—TN10
- CPU power control—TN5B.

The CPU power control provides a manual power switch, visual display of power alarms, and 5 V CPU power-up initialization supply. Figure 8 shows the faceplate of the TN5 circuit pack. The faceplates of the TN3, TN5, and TN6 circuit packs are identical.

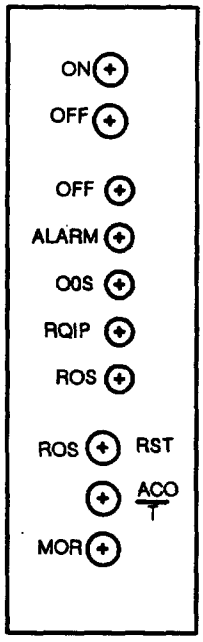


LEGEND:

CAC - CACHE CONTROL
CAM - CACHE MEMORY
CPU PC - CENTRAL PROCESSOR UNIT POWER CONTROL
CSB - CACHE STORE BOARD
DUC - DUAL ACCESS UTILITY CIRCUIT
DMU - DATA MANIPULATION UNIT
EAI - EMERGENCY ACTION INTERFACE
FPU - FLOATING POINT UNIT
MASU - MAIN STORE UPDATE
MC - MICROCONTROLLER
MCH - MAINTENANCE CHANNEL
MIC - MICROSTORE (PROGRAMMABLE)
MLTSI - MICROLEVEL TEST SET INTERFACE
PMS - PROGRAMMABLE MICROSTORE
PWR - POWER
SAC - STORE ADDRESS CONTROL
SAT - STORE ADDRESS TRANSLATOR
SDC - STORE DATA CONTROL
SREG - SPECIAL REGISTERS
UC - UTILITY CIRCUIT
WMS - WRITABLE MICROSTORE

* CAN BE:
UN48B (WMS) FOR R1 AND G2
UN28B (PMS) FOR R1 AND G2
† CAN BE:
MC3T003A1 (UN28B)
MC4C077A1B (UN28B)
‡ MC4C076A1 (UN135)

Figure 7. Central Processor Unit



LEGEND:
ACO - ALARM CUTOFF
MOR - MANUAL OVERRIDE
OOS - OUT OF SERVICE
ROS - REQUEST OUT OF SERVICE
RQIP - REQUEST IN PROGRESS
RST - REQUEST RESTORE TO SERVICE
T - TEST

Figure 8. Power Control Panel (TN3/TN5/TN6)

(b) **Main Store, Input/Output, and Disk File Controller Unit:** The MAS, I/O, and disk file controller (DFC) unit (MAS/IO/DFC) (Figures 9 and 10) contains two 495FA power units and the following circuit packs:

(1) Main store (MAS)

- MAS controller—UN59, UN59B or UN59C (used with EMM and VLMM features) also UN618 for R6
- MAS arrays (eight)—TN28, TN56 or TN2012 for R6.

(2) Input/output

- Dual serial channels (two)—UN9B
- Direct memory access controllers (two)— UN46.

(3) Disk file controller: there are two types of DFCs now available; the storage module drive (SMD) and the SCSI.

SMD - DFC (Figure 9)

The MAS/IO/DFC unit of Figure 9 is available in both 3B20D Model 2 and Model 3 computers.

The SMD-DFC consists of the following:

- Microcontrol store—TN68 (MC4C061A1B and MC4C061B1B) (TN19 if using 340MB disk drive) Effective with *UNIX* RTR Operating System Release 1 for the 3B20D Model 2 and Model 3 Computers
- Disk file controller interface—UN54 (UN55 if using 340MB disk drive) Effective with *UNIX* RTR Operating System Release 1 for the 3B20D Model 2 and Model 3 Computers
- Bus interface controller—TN70B
- Dual duplex serial bus selector—TN69B
- Peripheral device interface—UN64
- Power supply (495FA)
- Power switch (TN3B).

SCSI - DFC (Figure 10)

The MAS/IO/DFC unit of Figure 10 is available only in 3B20D Model 3 computers. The SCSI-DFC consists of the following:

- Power supply (410AB)
- Power switch circuit pack (TN6B)
- Duplex dual serial bus selector (TN69B)
- Host Adapter (UN294)
- Host Adapter (TN2116).

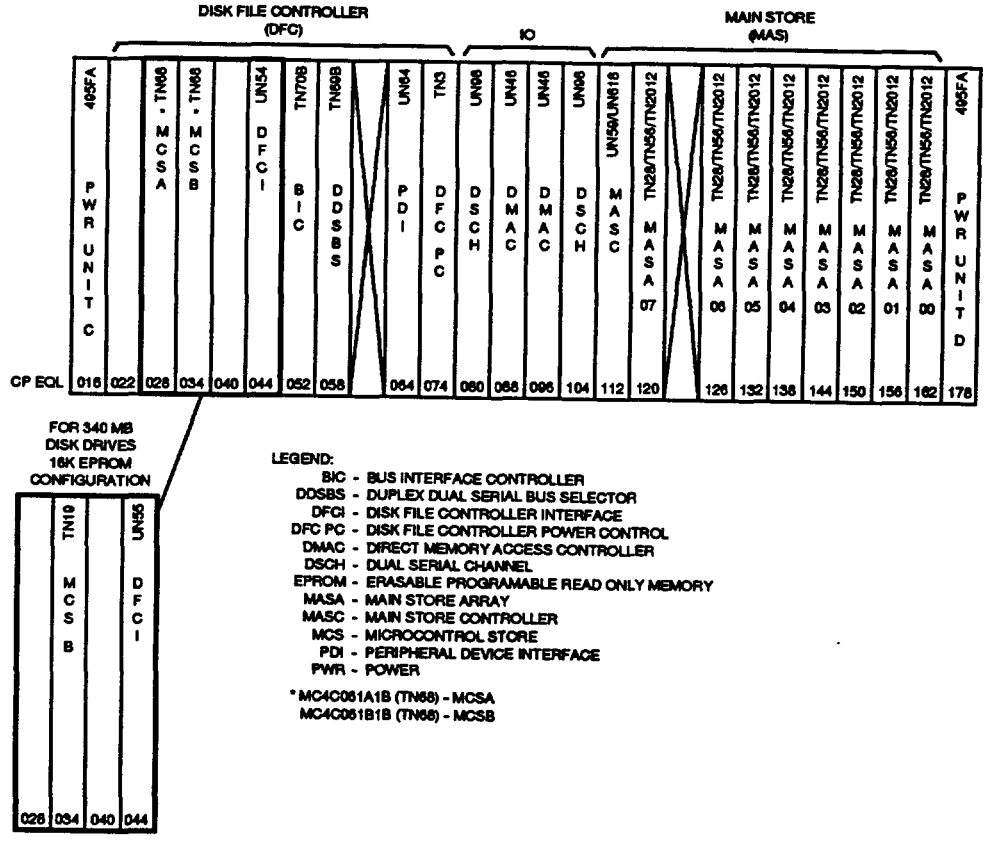
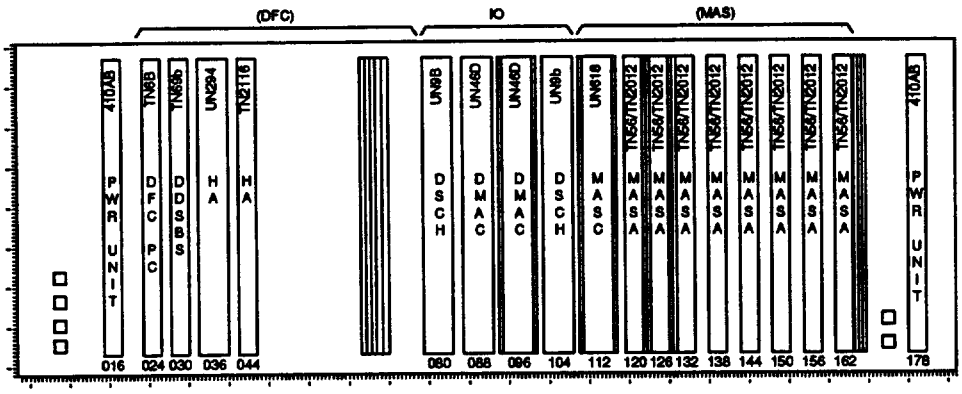


Figure 9. Main Store, Input/Output, and SMD Disk File Controller Unit



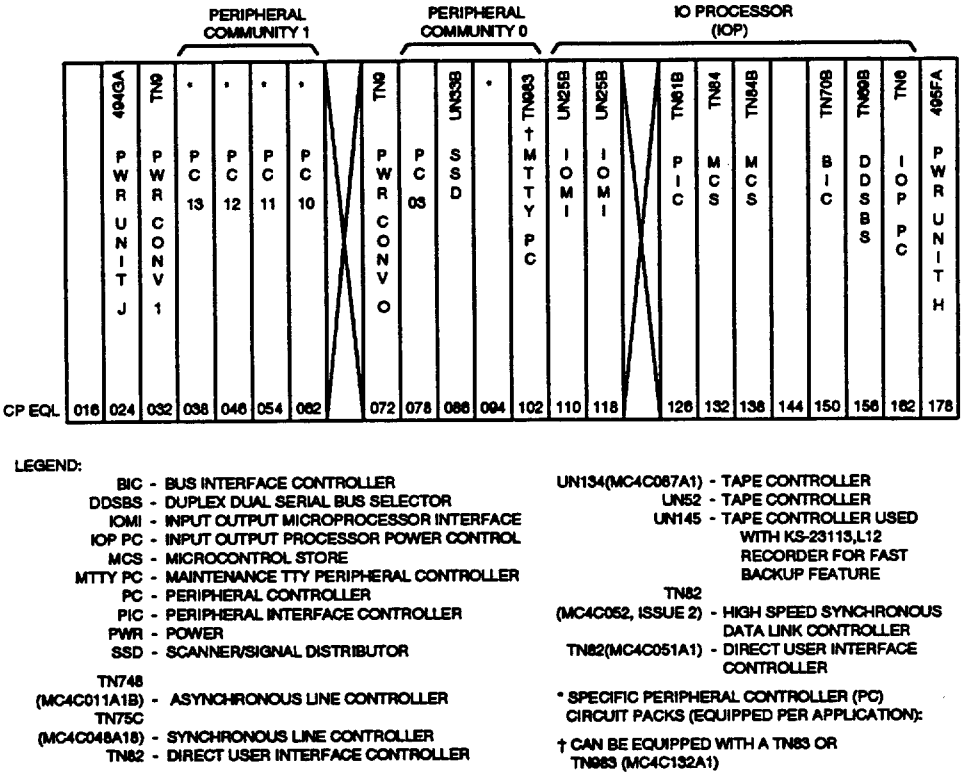
LEGEND:

DDSBS - DUPLEX DUAL SERIAL BUS SELECTOR
DFC PC - DISK FILE CONTROLLER POWER CONTROL
DMAC - DIRECT MEMORY ACCESS CONTROLLER
DSCH - DUAL SERIAL CHANNEL
HA - HOST ADAPTER
MASA - MAIN STORE ARRAY
MASC - MAIN STORE CONTROLLER
PWR - POWER

Figure 10. Main Store, I/O, and SCSI Disk File Controller Unit

(c) **Input/Output Processor Basic Unit:** The IOP basic unit (Figure 11) is made up of the following circuit packs:

- Selectable I/O microprocessor interface— UN25
- Peripheral interface controller—TN61
- 8K Microstore—MC4C049A1B (TN84)
- Bus interface controller—TN70
- Duplex dual serial bus selector—TN69
- IOP power control—TN6
- Peripheral communities 0 and 1.



LEGEND:

BIC - BUS INTERFACE CONTROLLER
DDSBS - DUPLEX DUAL SERIAL BUS SELECTOR
IOMI - INPUT OUTPUT MICROPROCESSOR INTERFACE
IOP PC - INPUT OUTPUT PROCESSOR POWER CONTROL
MCS - MICROCONTROL STORE
MTTY PC - MAINTENANCE TTY PERIPHERAL CONTROLLER
PC - PERIPHERAL CONTROLLER
PIC - PERIPHERAL INTERFACE CONTROLLER
PWR - POWER
SSD - SCANNER/SIGNAL DISTRIBUTOR
TN748 (MC4C011A1B) - ASYNCHRONOUS LINE CONTROLLER
TN75C (MC4C048A1B) - SYNCHRONOUS LINE CONTROLLER
TN82 - DIRECT USER INTERFACE CONTROLLER

UN134(MC4C067A1) - TAPE CONTROLLER
UN52 - TAPE CONTROLLER
UN145 - TAPE CONTROLLER USED WITH KS-23115,L12 RECORDER FOR FAST BACKUP FEATURE
TN82 (MC4C052, ISSUE 2) - HIGH SPEED SYNCHRONOUS DATA LINK CONTROLLER
TN82(MC4C051A1) - DIRECT USER INTERFACE CONTROLLER

* SPECIFIC PERIPHERAL CONTROLLER (PC) CIRCUIT PACKS (EQUIPPED PER APPLICATION):

† CAN BE EQUIPPED WITH A TN83 OR TN983 (MC4C132A1)

Figure 11. Input/Output Processor Basic Unit

The IOP also provides additional space for a growth UN25 and a growth TN84 circuit pack. The UN25 circuit pack is used to interface with four peripheral communities. Each peripheral community is equipped with TN9 circuit packs, which provide independent +12 and –5 V for peripheral controller memories and ±12 V for communication interfaces. Each peripheral community consists of up to four peripheral controller circuit packs. The specific peripheral controller circuit packs are equipped according to the application. The 495FA power unit H on the right side of the unit provides +5 V logic power for the IOP control portion and community 0. The 494GA power unit J provides +5 V logic power for community 1.

(d) **MAS and IOP Growth Unit:** The growth unit (Figure 12) can be located between the MAS, I/O, and DFC unit and the IOP basic unit.

- The growth unit has positions for eight additional TN28 or TN56 (TN2012 for R6) MAS array circuit packs.
- Positions are provided for adding four additional I/O channels and two additional peripheral communities (2 and 3). The 495FA power unit E on the left side of the growth unit supplies +5 V logic power for both peripheral

communities. Power unit F on the right side supplies +5 V logic power for the MAS and I/O growth packs.

(e) **ED-4C387 Cooling Unit:** The cooling unit is comprised of four plug-in fans. The fans provide filtered air with a common plenum between the modules. The fans are equipped on two trays, two fans per tray. The two trays plug into the common plenum. When a fan fails, the common plenum design allows the remaining three fans to partially replace the cooling provided by the failed fan. The cooling unit includes its own power switch and alarm features.

(f) **Port Switch Unit:** The port switch unit is located at the bottom of bay 0 of the processor frame. The port switch unit can have a maximum of four port switch subunit circuit packs (TF4) and five scanner/signal distributor (SSD) interface circuit packs (TF2).

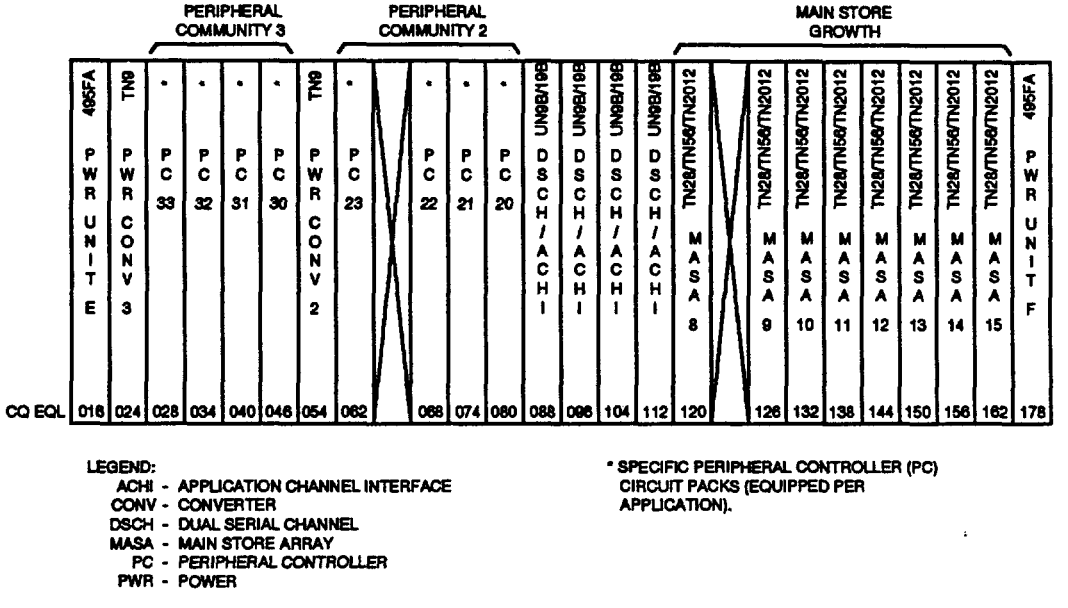


Figure 12. Main Store and Input/Output Processor Growth Unit

(g) **Power Distribution Unit:** The power distribution unit is comprised of fuse blocks, receptacles, and terminal blocks. This unit uses 70- and 74-type fuses. The 74-type fuse is a fast-blow fuse, and the 70-type fuse is a slow-blow fuse, which provides a visual indication of a blown fuse.

D. 300-Mbyte Moving Head Disk Drive Frame

3.15 The 300-Mbyte disk drive is one of the disk drives used with the 3B20D Model 2 computer. Each 300-Mbyte moving head disk drive frame (Figure 13) contains a KS-22707, L1 or L2 (L6 available with different color appearance) 300-Mbyte disk drive, a 2000 VA inverter, and a disk power control panel. The disk drive requires 208 V 60-Hz single-phase power, which is supplied by the inverter. The inverter contains two cooling fans, a fuse, and two plug-in circuit packs. One circuit pack contains the microprocessor and control circuitry while the other contains the silicon-controlled rectifiers used for generating the output ac power. The disk power control panel contains an ED-4C194 plug-in control unit for the inverter.

3.16 The 300-Mbyte disk drives use KS-22048 removable disk packs that can be installed or removed via a pack access lid at the top front of each unit. The panels and covers of each unit are also removable, which allows access to the upper and lower interior of the unit for maintenance purposes.

E. 160-Mbyte Minimodule Disk Drive Frame

3.17 Each minimodule disk drive frame (Figure 14, used with the 3B20D Model 2 computer) can contain up to three KS-22693 160-Mbyte disk drives and three 1200 VA inverters. The nonremovable minimodule disk platter assemblies are housed in a sealed module with a closed-loop air system. Each disk drive requires 120 V 60-Hz single-phase power, which is supplied by the 1200 VA inverter. The inverter contains one TN2 circuit pack, five 495H1 circuit packs, and one 394A synthesizer. The TN2 circuit pack contains the power cycling switch and alarm circuitry. The 495FA packs are –48 V to ±175 V DC-to-DC converters. The 394A synthesizer converts the ±175 V DC to 120 V AC.

F. Tape Disk Frame (340-Mbyte Fixed Storage Disk)

3.18 The 340-Mbyte fixed storage disk drives are housed in the tape/disk frame, (Figure 15, and the tape/disk cabinet, Figure 2). If the upper portion of the tape/disk frame or tape/disk cabinet contains a magnetic tape unit, a maximum of four KS-22875, disk drives may be housed in the lower portion as shown in Figure 15(a) and Figure 2. If the frame is used to house only disk drives, a maximum of eight drives may be equipped as shown in Figure 15(b) for the 3B20D Model 2 computer. This arrangement of eight drives on a frame is also an available configuration for the 3B20D Model 3 computer. Each 340-Mbyte fixed storage disk drive has its own KS-22997 power supply and ED-4C480 power switch. The storage medium for the 340-Mbyte disk drive is a rigid platter arrangement, not removable from the drive assembly.

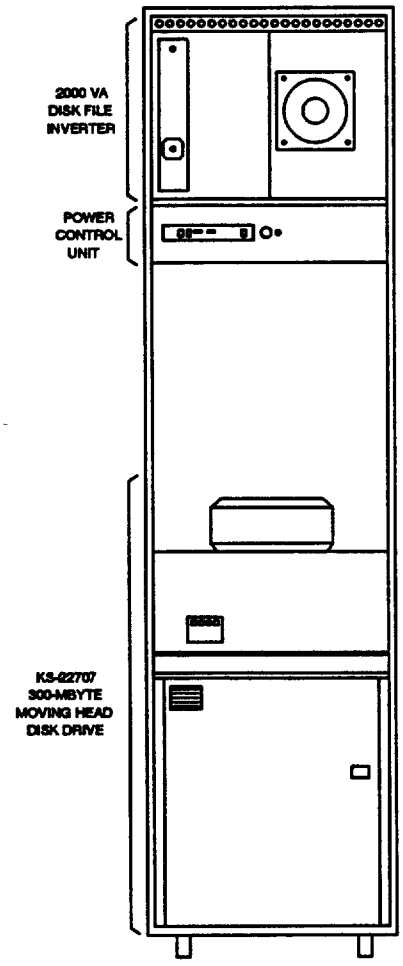


Figure 13. 300-Mbyte Moving Head Disk Driver Frame

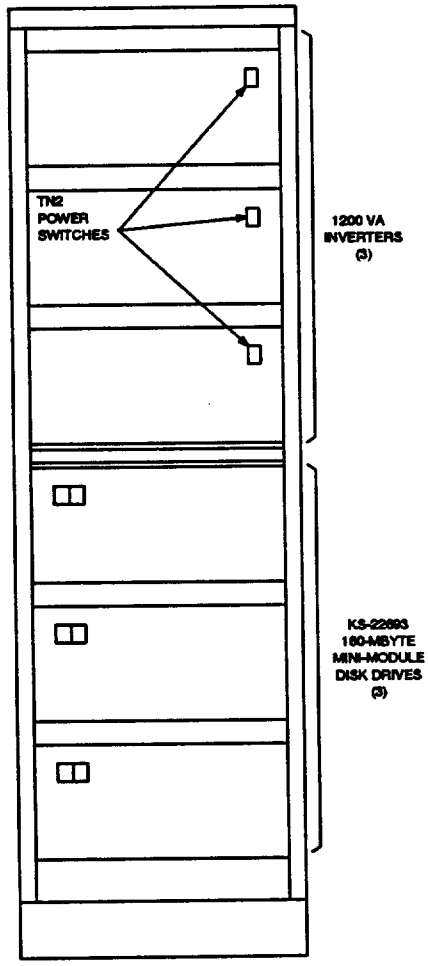


Figure 14. 160-Mbyte Mini-Module Disk Frame

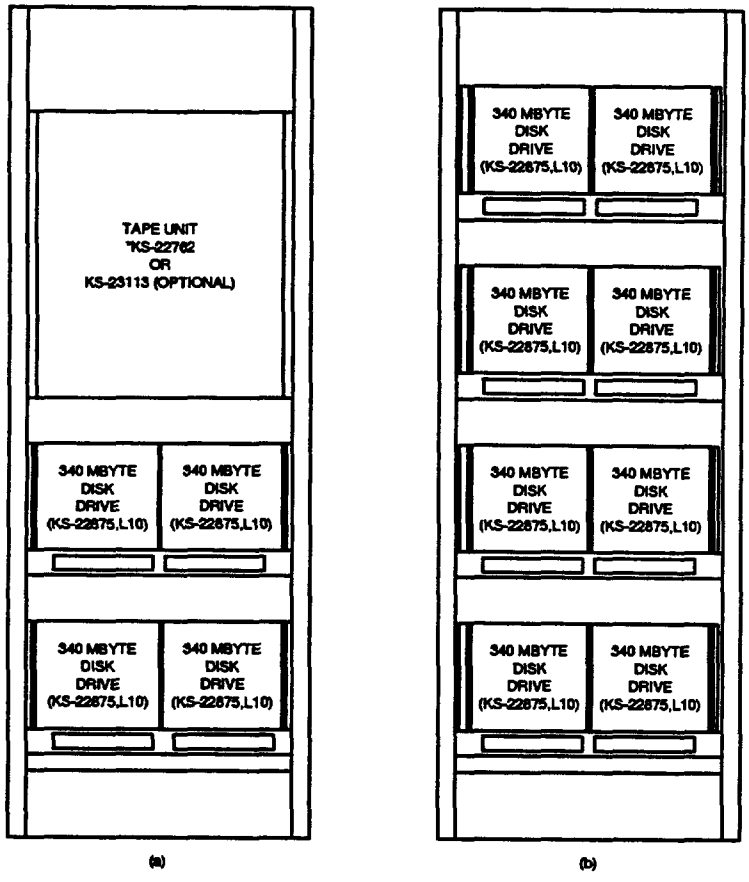
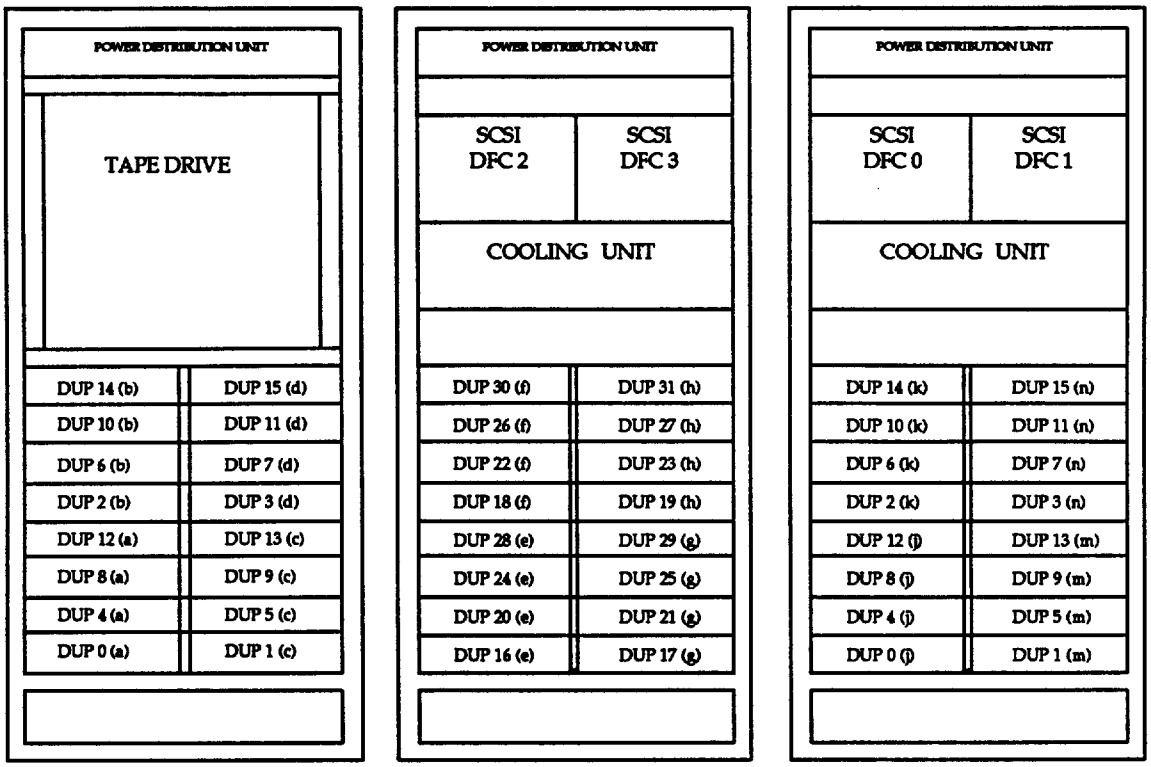


Figure 15. 340-Mbyte Fixed Storage Disk Drive Frame Mounting Arrangements

3.19 Effective with the *UNIX* RTR Operating System Release 1, the KS-23113 tape drive is available to replace the KS-22762 tape drive of the 3B20D Model 2 computer. This tape drive is part of the fast backup feature that is used to reload the disk and system in a minimum amount of time.

G. SCSI Disk Cabinet

3.20 The SCSI disk cabinet is used to house the SCSI DUP. The cabinet can be configured three ways. The first configuration is for new start systems and consists of a tape drive and up to 16 DUPs (Figure 16a). The second configuration, used when the SCSI hardware is grown onto an existing 3B20D computer, is equipped with two SCSI DFCs, a cooling unit, and up to 16 DUPs (Figure 16b). The third configuration (Figure 16c) is used when an existing 3B20D computer SMD-DFC is converted to a SCSI-DFC.



NEW SHIP
Figure 16a

GROWTH
Figure 16b

CONVERSION
Figure 16c

LEGEND:
(a) = SCSI DUPs on DFC 0 - Bus 0
(b) = SCSI DUPs on DFC 0 - Bus 2
(c) = SCSI DUPs on DFC 1 - Bus 1
(d) = SCSI DUPs on DFC 1 - Bus 3
(e) = SCSI DUPs on DFC 2 - Bus 4
(f) = SCSI DUPs on DFC 2 - Bus 6
(g) = SCSI DUPs on DFC 3 - Bus 5
(h) = SCSI DUPs on DFC 3 - Bus 7
(j) = SCSI DUPs on DFC 0 - Bus 0
(k) = SCSI DUPs on DFC 0 - Bus 2
(m) = SCSI DUPs on DFC 1 - Bus 1
(n) = SCSI DUPs on DFC 1 - Bus 3

Figure 16. SCSI Disk Cabinet

3.21 Two DUPs are mounted on each shelf. Tabs at the rear of the shelf engage slots at the rear of the DUP as it is slid into position. A stiffening bracket, also with tabs, is installed across the front. This bracket engages slots on the front of the DUP and is installed with screws to secure the DUP to the shelf.

3.22 A power distribution unit at the top of the cabinet contains fuses for the -48 V DC power feeders that supply each DUP and, when equipped, the DFCs and cooling unit. A tape drive, when mounted in this cabinet, receives 120 V AC from a local ac power panel.

H. Tape Unit Frame

3.23 The tape unit frame of the 3B20D Model 2 computer (Figure 17) contains space for two KS-22762, L1 or L3 tape transport units or two KS-23113, L12 tape transport units, effective with *UNIX* RTR Operating System Release 1. The KS-23113, L12 is used in the fast backup feature, but other tape transport units with compatible specifications may be used. The tape transports use 120 V 60-Hz single-phase power. The tape transport unit has a plastic, hinged, front cover for protection from dust and foreign matter. The cutout portion of the cover allows access to the control panel (Figure 17, both tape units have similar controls). A circuit breaker is located behind the front door in the top right corner of each tape transport to provide overcurrent protection for the power supply circuit.

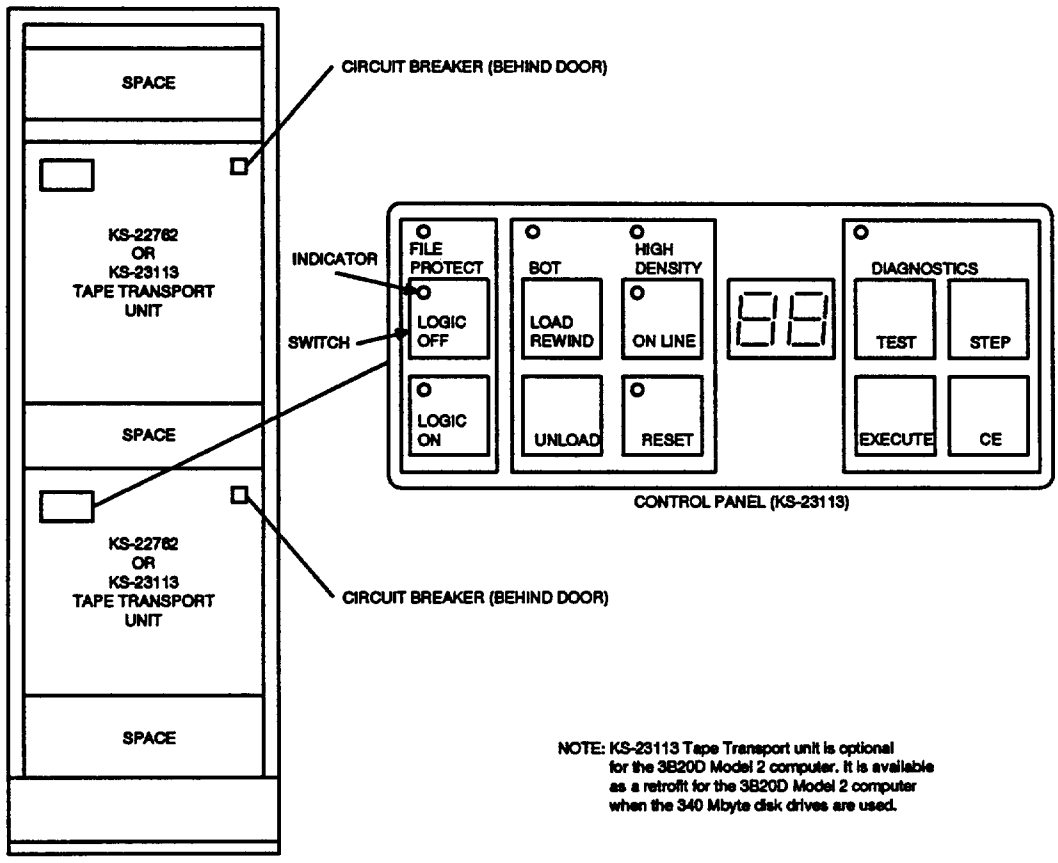


Figure 17. Tape Unit Frame

I. Power Distribution Frame

3.24 The J86334B power distribution frame (Figure 18) for the 3B20D Model 2 computer distributes power from a battery plant. It consists of up to five –48 V power distribution panels. Protective doors enclose the rear of the frame to protect personnel and frame circuitry.

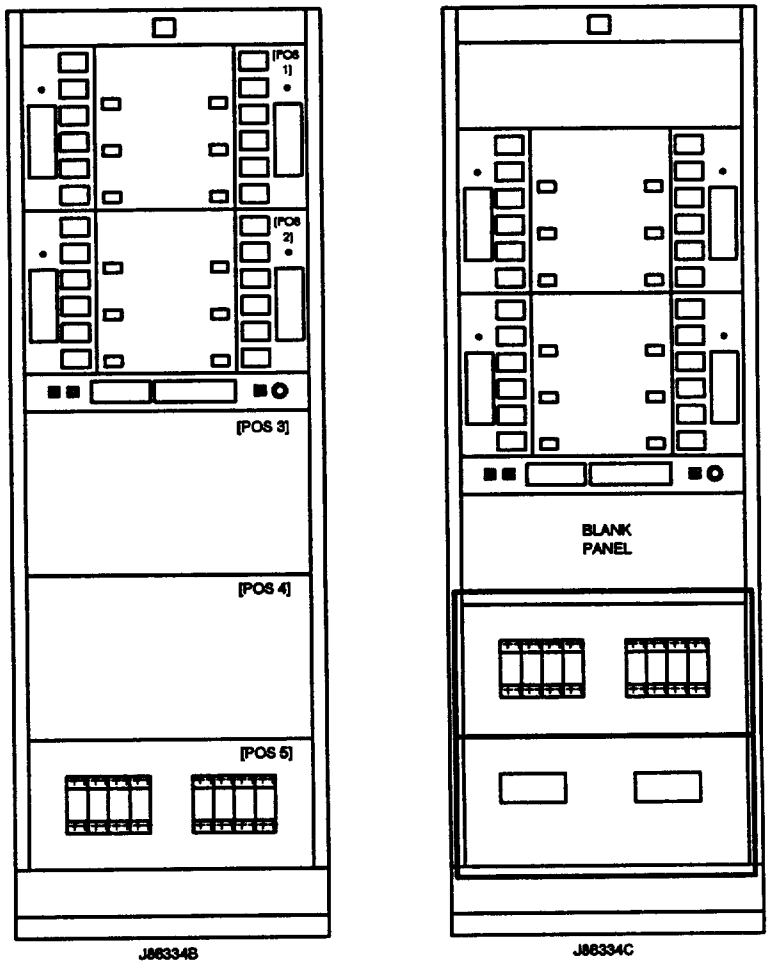


Figure 18. Power Distribution Frame

3.25 The J86334C power distribution frame (Figure 18) for the 3B20D Model 2 computer distributes power from a converter plant. It consists of up to four –48 V power distribution panels. The frame has the same dimensions as the J86334B frame. The ED-82947-30, G2, filter fuse panel assembly and ED-82947-30, G1, control panel assembly are used in both the J86334B and J86334C power distribution frames. The J86334C has additional capacitors to improve filtering of the converter plant output. Input power to the J86334C frame is terminated on a panel at the top of the frame.

3.26 The 3B20D Model 3 computer requires –48 V DC power. For host systems that can supply protected –48 V DC power, two options exist: power can be distributed from a power distributing frame to the power distribution units at the top of each cabinet, or the DC-to-DC option power cabinet in Figure 19 (a) may be used. This cabinet requires two –48 V buses (A and B) as inputs from the dc source. Power is then distributed from the power cabinet to the power distribution units.

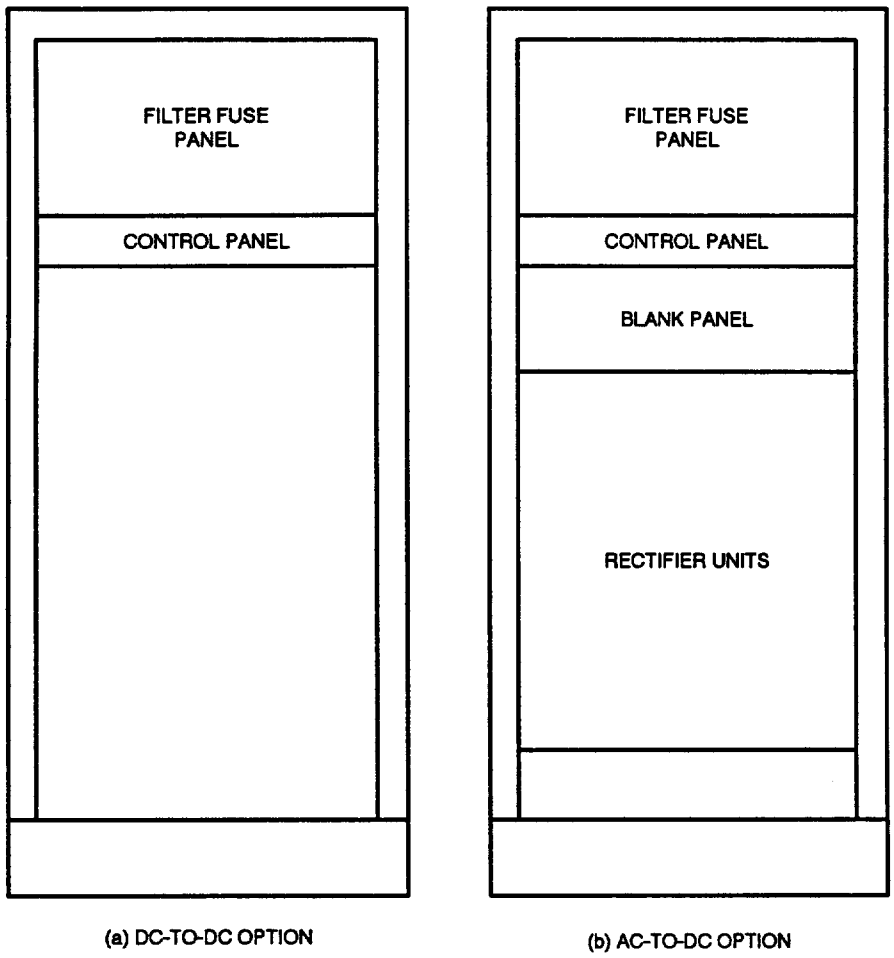


Figure 19. 3B20D Model 3 Computer Power Cabinet

3.27 Host systems with only AC power available require the AC-to-DC option in Figure 19 (b). The power cabinet in Figure 19 (b) is equipped with two AC-to-DC rectifiers and requires 208/220 V, 3-phase AC input. One rectifier supplies power via the filter fuse panel to computer bay 0 and its associated units. The other rectifier supplies power through the filter fuse panel to processor bay 1 and its peripherals. Each rectifier receives input from an independent ac source such that no single point failure of the power system will cause both computers to fail.

J. Maintenance Terminal and Printer for Model 2 and Model 3 Computers

3.28 The maintenance terminals (Figure 20) used with the 3B20D Model 2 computer are the KS-22497, L1 black and white video monitor terminal and the optional KS-22921, L2 color video monitor terminal. The color monitor became optional for the 3B20D Model 2 computer with the *UNIX* RTR Operating System Release 1. The 3B20D Model 3 computer uses the color video monitor terminal (KS-22921, L2). The terminals provide communications for system control and display, input and output messages, and emergency action interface (EAI) control and display. The maintenance printers used with the Model 2 and Model 3 computers are the *Teletype*® Models 40 and 5310 line printers.

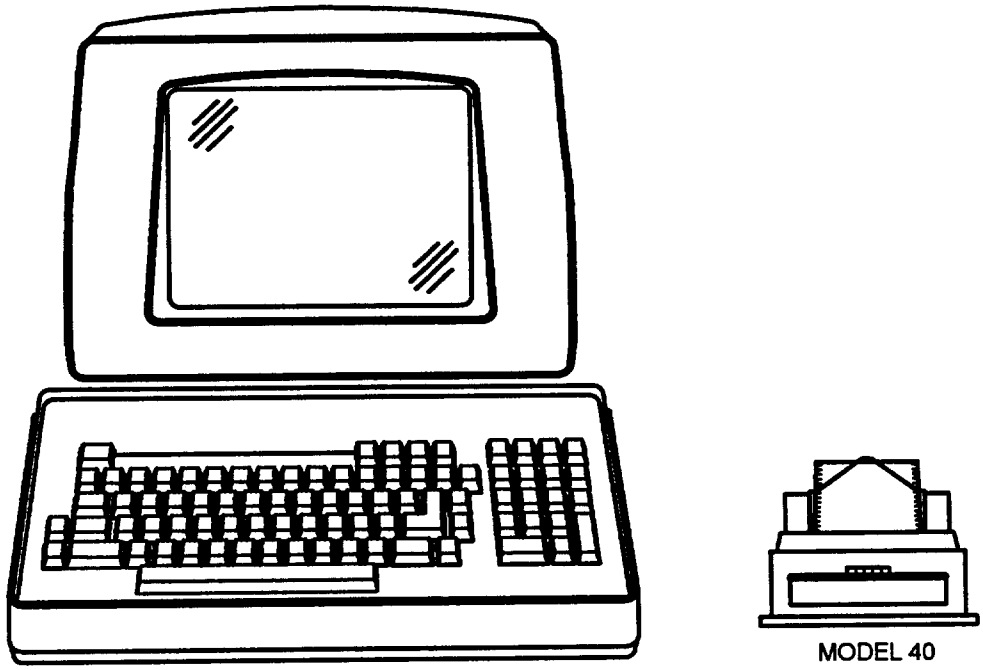


Figure 20. Maintenance Terminals and Printers for Model 2 and 3 Computers

4. Functional Description

4.01 Figure 4 shows the operating configuration of the AT&T 3B20D Model 2 and Model 3 computers. The system provides two independent duplicated processors (0 and 1). An entire processor consisting of the CPU, MAS, DMA, and I/O buses functions as a switchable (on-line/off-line) entity. One processor is always the on-line processor. The processors are not run in the synchronous and match mode of operation as done in earlier stored program control systems. However, the on-line processor keeps both main stores (on-line and off-line) and the duplex disk drives up to date in case a processor or disk switch becomes necessary. Figure 21 provides a functional overview of the computers.

A. Central Processor Unit

4.02 The 32-bit microprogrammed CPU (Figure 22) provides high-speed control functions (logic, control, and arithmetic processes) required by the computer. Each of the two duplicated (duplex) computers in the system has its own CPU. The physical location and arrangement of circuit packs comprising the CPU are shown in Figure 2, 3, and 6.

4.03 The machine-level program instructions for the computer are stored in the MAS as 40-bit words. There are 32 bits containing the instruction data, and 4 parity bits. The Main Store Controller (MASC) generates 8 Hamming bits for storage with the 32 data bits. The transfer of instruction and data words between the CPU and MAS involves only the 32 bits and the 4 parity bits (parity bit generated on a read). The Hamming bits are generated and processed within the MAS. The CPU can address and access all 32 bits, a 16-bit half-word, or a single byte (8 bits) for either read or write operations. The time required by the CPU to access MAS is 850 ns.

4.04 To increase real-time capabilities, an optional high-speed, temporary cache store can be used to store frequently read MAS locations. The access time for the cache store is 250 ns compared to the 850 ns of the MAS. The cache store is a 2K-word (4K word for R6) semiconductor memory. Each word read from the MAS is stored in the cache store, and the cache address is linked to the MAS address. If a succeeding memory fetch request is to that same address, the word in the cache store is accessed by the CPU using only 250 ns of computer time. If the word is not found in the cache store, it is fetched from MAS. In this manner, the 2048 (4096 for R6) most often fetched words will often be accessible to the CPU in 250 ns. Functionally, the cache store interconnects the CPU and MAS through a cache address bus, cache data bus, and control leads. The DMA path to the MAS is not through the cache store. The cache monitors DMA-to-MAS data writes; and if the MAS address contains data stored also in cache, the cache word is automatically invalidated. The cache circuit packs are the cache control (UN10B or UN616 for R6) and cache memory (UN11B or UN617 for R6).

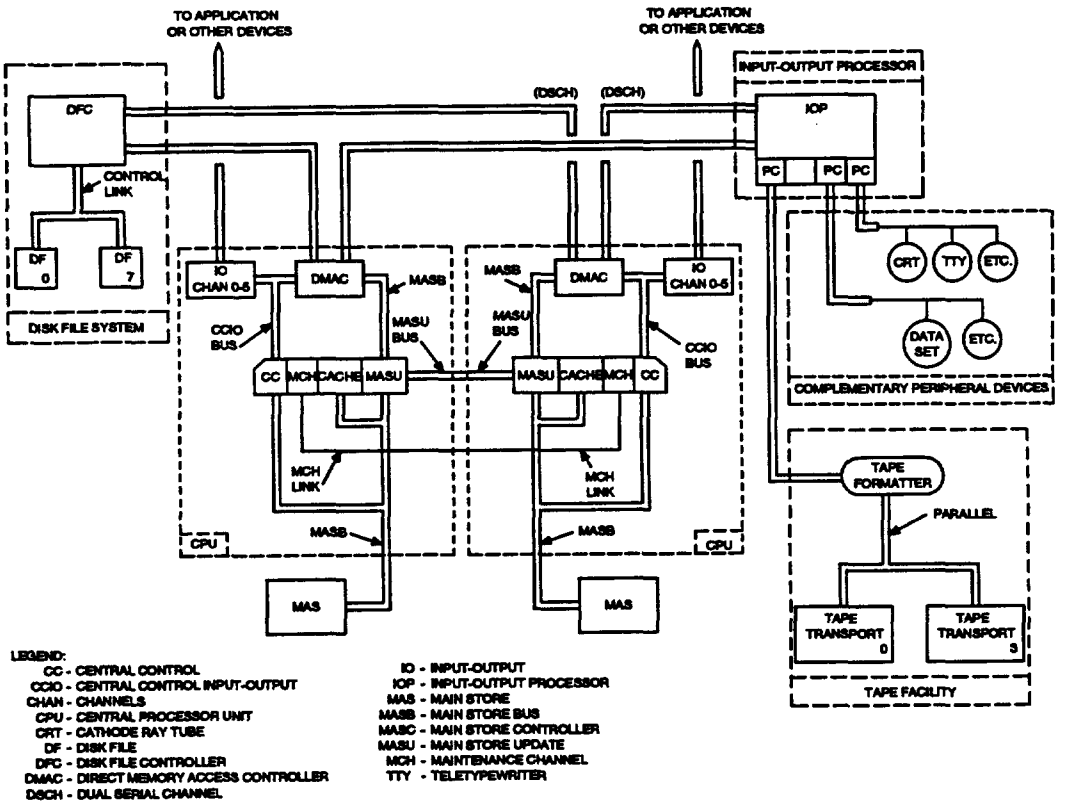


Figure 21. 3B20D Models 2 and 3 Computer Functional Overview

4.05 The execution of program instructions is under the control of a microcontrol circuit pack (UN135). The microcontrol translates the operation code of a program instruction into a starting address in the microstore containing a sequence of 64-bit microinstructions necessary to execute that program instruction. Microstore consists of one 2K word (256 words) of read-only microstore, which is preprogrammed read-only memory (PROM), and at least one 4K word (16K word for R6) of writable microstore units. The read-only microstore is a UN28B circuit pack, and each writable microstore (WMS) unit is contained on a UN48B (UN248 for R6) circuit pack. The microstore can be configured for a maximum of four circuit packs (one of each type required).

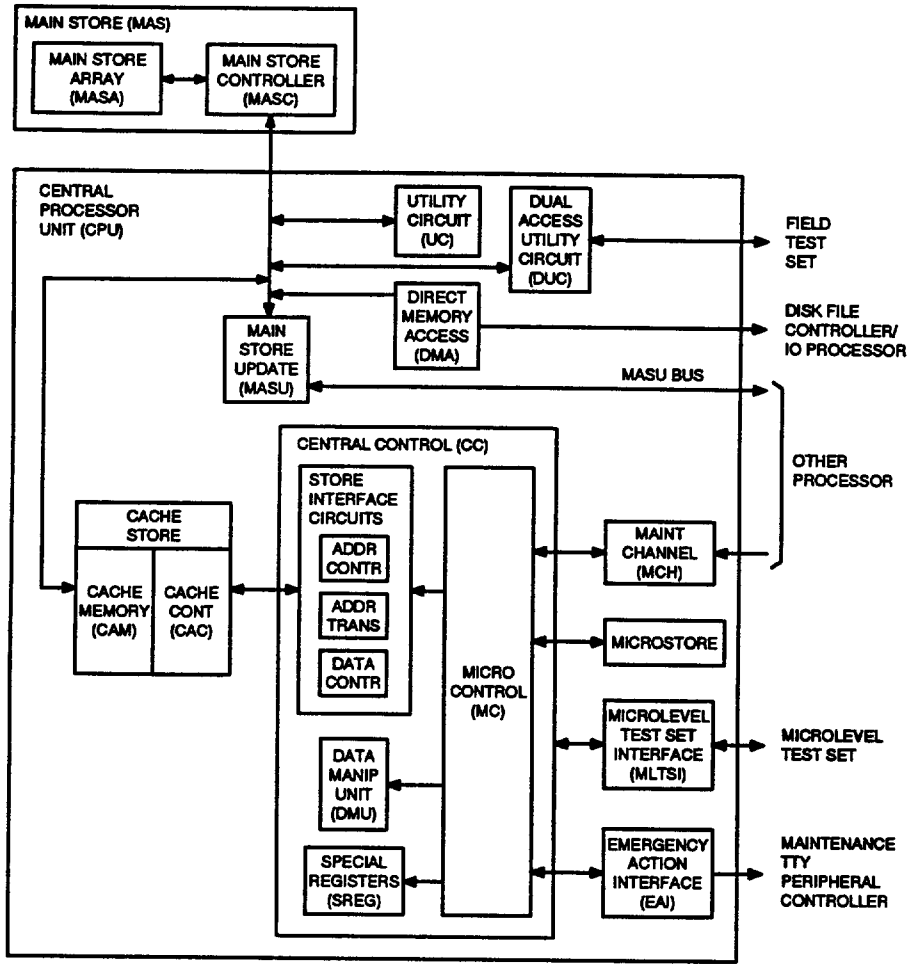


Figure 22. Central Processor Unit and Main Store Functional Diagram

4.06 The arithmetic and logic operations are carried out by the data manipulation unit (DMU) (circuit packs UN1C and UN23C). The DMU contains 16 general registers. A number of special registers associated with CPU operation are external to the DMU and are provided by the UN2B, UN3B, and UN3C circuit packs.
These special registers provide storage for control, status, I/O data, interrupt control, and error data.

4.07 Three functional units comprise the store interface circuits. The store address translator (circuit pack UN45B/UN45C or UN612 for R6) translates a logical address (virtual address) in the store address register to a physical address in the MAS. The store address control circuit pack (UN43B, UN43D, or UN611 for R6) provides the store address and control functions. The store data control (circuit pack UN6B) contains the interface and control for the store data and instructions.

4.08 The maintenance channel (MCH) circuit pack (UN22C) provides the interface between the CPUs of computer 0 and computer 1. The two MCH packs communicate over a dedicated serial data link (cable) to provide maintenance access and control of the off-line computer. The MCH provides the capability to run, stop, load, clear, and step the other processor. It allows the on-line computer to read some off-line computer registers directly and others indirectly using microcoded sequences. Diagnostic test programs can be loaded through the MCH to the off-line microstore or MAS.

4.09 The EAI circuit pack (TN10) provides low-level status and control access to the associated computer. The EAI indicates the computer status via light-emitting diodes (LEDs) located on the circuit pack. The EAI sends status signals to the maintenance teletypewriter peripheral controller (MTTYPC) on request. The MTTYPC subsequently conveys this status information on the emergency action page displayed on the maintenance cathode-ray tube. Control commands initiated at the maintenance cathode-ray tube are passed to the MTTYPC and then on to the EAI. The faceplate of the EAI is shown in Figure 23.

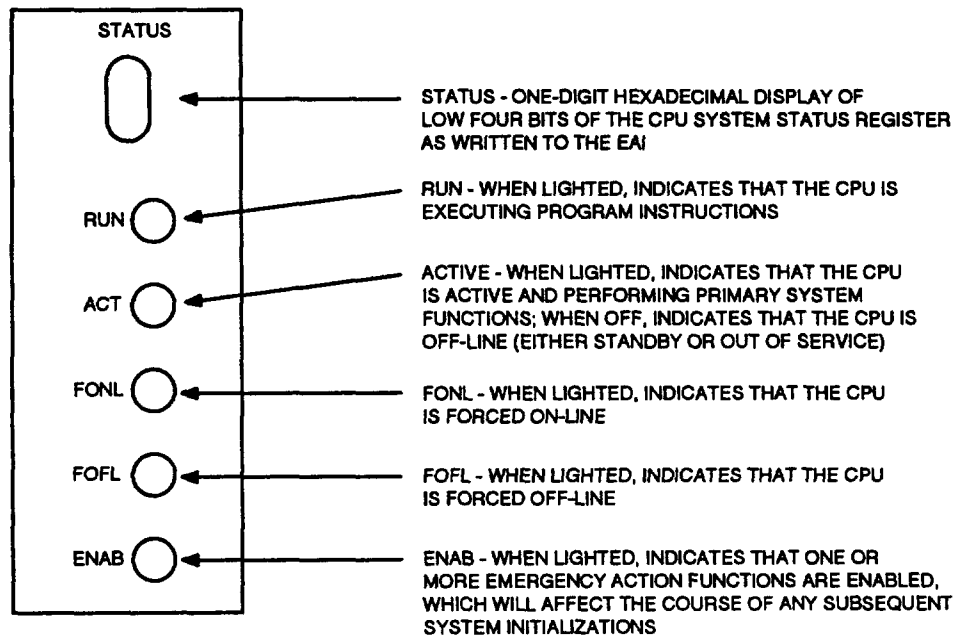


Figure 23. Emergency Action Interface

4.10 Power for the CPU is provided by the two power units (495FA circuit packs) and the CPU power control (TN5 circuit pack). The power converters provide power directly to the multilayer backplane serving the CPU. Current programming resistors, instead of fuses, provide backplane protection. The CPU power control circuit pack is used to apply power to (or remove power from) the computer and provide a –5 V power supply for CPU power-up initialization. The TN5 circuit pack faceplate is shown in Figure 8.

4.11 A microlevel test set is available for CPU testing. The test set can be used to input microinstructions and monitor CPU operation. The MLTS can be accessed locally through an RS-232 port or remotely via a built in modem. The interface between the computer and the microlevel test set is provided by the microlevel test set interface (UN16B circuit pack optional).

4.12 The utility circuit is an optional UN21B circuit pack that monitors the operations between the CPU and the main memory (cache or main store) for the purpose of program debugging and testing. The utility circuit consists mainly of matcher (comparator) and transfer-trace circuitry. The generic access package sets up the matchers and transfer-trace logic. All commands sent to the utility circuit are decoded from the bidirectional gating bus data and control lines.

4.13 The dual-access utility circuit is an optional UN61 (or UN615 for R6) circuit pack that monitors the operations between the CPU and the main memory (cache or MAS) for the purpose of program debugging and testing. The dual-access utility circuit consists mainly of matcher (comparator) and trace memory circuitry. The dual-access utility circuit is controlled by either the generic access package (resident memory) or the field test set. All commands sent to the dual-access utility circuit are decoded by either the bidirectional gating bus or the field test set data and control lines.

B. Main Store

4.14 The MAS (Figure 22) is a 40-bit semiconductor-type memory. The computer is a 32-bit machine; and each word stored in the MAS consists of four 8-bit bytes of information and 8 Hamming bits. The MAS is full-word (32 bits), half-word (16 bits), or byte (eight bits) addressable by the CPU. The physical location and arrangement of circuit packs comprising the MAS are shown in Figures 2, 3, 9, and 12.

4.15 The basic element of the MAS is the main store array (MASA) circuit pack. Depending on the option selected, each MASA circuit pack contains either one, two, or four megabytes of dynamic, volatile, random-access semiconductor memory. Dynamic means that the stored memory data is not permanent and must be refreshed at definite time intervals or the stored information will be lost. Volatile means that, if power is interrupted, stored information is lost. Random access means that any address in the MAS may be read out or written into on command without regard to previous or subsequent addresses. A single main store controller circuit pack interfaces the MAS bus with the MASA circuit packs.

4.16 The MAS may be equipped with either TN28 or TN56 (TN2012 in R6) MASA circuit packs as follows:

- **TN28 (1-Mbyte) Option**

  Each TN28 MASA circuit pack contains one megabyte (256K words) of semiconductor memory. The basic MAS consists of a configuration of eight TN28 MASA packs designated MASA 0-7 housed in the MAS, I/O, and DFC unit of the processor control frame shown in Figures 2 and 7. The MAS and IOP growth unit (see Figure 9) provides for up to eight growth TN28 MASA packs. The basic unit with the maximum of eight additional growth TN28 MASA packs provides the 3B20D computer with a maximum MAS storage capacity of 16 megabytes (4096K words). With the TN28 option, a UN59 main store controller (MASC) is used to interface the MAS bus with all MASAs including growth MASAs.

- **TN56 (2-Mbyte) Option (available with *UNIX* RTR Operating System Release 1)**

  Each TN56 MASA circuit pack contains two megabytes (512K words) of semiconductor memory. The basic MAS consists of a configuration of eight TN56 MASA packs designated MASA 0-7 housed in the MAS, I/O, and DFC unit of the processor control frame shown in Figures 2 and 9. With the EMM feature, eight additional TN56 circuit packs may be added to the IOP growth unit shown in Figure 12.

- **TN2012 (4-Mbyte) Option (available with R1 or R6)**

  Each TN2012 MAS circuit pack contains a 4 megabyte (1024 words) memory array that requires the UN618 MASC which has a default mode of 16 megabyte address range. There can be a maximum of 8 TN2012s (32 Mbyte) per control unit (CU) on the system.

4.17 The MAS bus provides an interface between the CPU, MAS units, MAS update unit, and the DMA. The flow of data, address information, and control signals over the MAS bus is controlled by the MAS update unit according to the operating configuration of the 3B20D computer. In the normal duplex mode, one computer (including the MAS) will be active (on-line) and the other standby (off-line). The operating environment for an active or standby MAS is basically as follows:

(a) Active (On-Line) MAS: Normally, the active MAS is being read or written into by its own CPU or DMA.

(b) Standby (Off-Line) MAS: Normally, the standby MAS is being written into by the active CPU or DMA of the active computer (in the opposite processor frame bay). This provides an up-to-date backup MAS for the active MAS should an error condition occur. In that case, the on-line computer may be switched to off-line or the on-line CPU, or DMA may decide to read from the off-line MAS.

4.18 The overall function of the MAS is controlled by the MAS update UN133 (UN614 for R6) circuit pack in each processor and the update bus which interfaces the two circuit packs. The MAS update circuit pack in each processor performs the access control function for the MAS of that computer. The on-line computer updates and maintains the MAS of the off-line computer via the MAS update circuit packs and the

MAS update bus. Also, in an error situation, the on-line computer can use the update bus to read the MAS of the off-line computer.

4.19 The MASC is a UN59, UN59B or UN59C (UN618 for R6) circuit pack that interfaces the MAS bus with all MAS arrays (including added growth MAS arrays). The UN59B or UN59C is required when using the TN56 circuit packs and UN618 is used with TN2012.

C. Input/Output System Interfaces

4.20 The computer supports a large number and variety of peripherals to accommodate a wide range of device speeds (teletypewriter versus disk), operational processing differences, and the lack of interface standards in the peripheral market. Three types of I/O interfaces are provided:

- Direct memory access controller (DMAC)
- Dual serial channel (DSCH)
- Application channel interface (ACHI).

4.21 The computer can be equipped with as many as six programmed I/O channels (DSCH or ACHI) and two DMACs. The DSCH and ACHI are directly controlled by the CPU microcode via the central control input/output (CCIO) bus. The DMAC provides the capability for direct memory transfers between the MAS and peripheral devices. The physical location and arrangement of circuit packs comprising the I/O interfaces are shown in Figures 2, 3, 9 and 12.

4.22 The CCIO bus links the CPU with the I/O channels. Operations over the bus are programmed I/O instructions. Control of the DMA circuits is exercised over this bus, but the data transfers via DMA are accomplished via the MAS bus. Each duplicated computer has its own dedicated CCIO bus.

4.23 A DMAC provides the facility for moving data between peripheral devices and MAS without involving the CPU directly in the data transfer. Each duplicated computer may be configured with up to two DMAC (UN46 for R1 and UN613 for R6) circuit packs. Each DMAC can support concurrent operation of as many as 32 peripheral devices (16 on each of two UN9B DSCH circuit packs). The data communication between the CPU, DMAC, and MAS is over parallel data buses. The DSCH provides a high-speed serial data link (RS422 industry standard) to each peripheral device. At the peripheral device, a duplex dual serial bus selector (DDSBS) (TN69 circuit pack) converts the serial data back to a parallel format. Two serial ports are provided on each DDSBS circuit pack to allow each peripheral device to communicate with the DMA systems of both computers. The CCIO bus provides the interface between the CPU and DMAC over which the CPU initializes the DMAC tables (the DMAC maintains the data) that contain the MAS address of the page tables involved in the transfer to/from a device. After initialization and setup of the DMAC tables, the device can initiate the transfer request when it is ready. The actual data transfer between the device and MAS is via the main store bus and DMAC and can be in either a word or block (16 words) mode. The device will continue this handshaking process of transfer requests followed

by datatransfers until the entire job specified in the peripheral device is completed. The maximum size of a DMA transfer job is 64 pages (128K bytes).

4.24 When the DSCH is on the CCIO bus, it provides high-speed serial links between the CPU and up to 16 peripheral devices. The DSCH data transfers use the parallel CCIO bus for control functions and the actual transfer of data. This type of I/O operation is completely controlled by software using specific programmed I/O instructions. A DSCH (UN9B circuit pack) provides a high-speed serial data link (RS422 industry standard) to each peripheral device. At the peripheral device, a DDSBS (TN69 circuit pack) converts the serial data back to a parallel format. Two serial ports are provided on each DDSBS circuit pack to allow each peripheral device to communicate with the DSCH in either computer.

4.25 The ACHI is a general-purpose parallel programmed I/O channel between the CPU and application-designed circuits. The ACHI, a UN19B circuit pack, provides a peripheral device (application-designed) access to the CCIO bus and hence the CPU.

D. Input/Output Processor and Peripheral Controllers

4.26 The IOP functions as a front-end processor to control I/O transfers between the computer and various peripheral units, thereby reducing the load on the CPU. The IOP is intended for use with terminals, data links, magnetic tape units, and other slow-speed/medium-speed peripheral units requiring block transfers of data to and from the MAS. The IOP itself is treated by the system as a peripheral device driven by a DMAC as shown in Figure 24. The physical location and arrangement of circuit packs comprising the IOP are shown in Figures 3, 11, and 12.

4.27 The IOP (Figure 21) interfaces the computer with up to four peripheral communities. The IOP basic unit provides for two communities (0 and 1). The IOP growth unit provides for the addition of communities 2 and 3. Each peripheral community contains four individual peripheral controllers (PCs).

4.28 The IOP interfaces with a DMAC in both processors via a DDSBS circuit pack (TN69B) as shown in Figure 24. These two identical serial interfaces allow either CPU-DMA to communicate with the IOP. The DDSBS converts the serial data from the DMAC to parallel format.

4.29 A bus interface controller (BIC) circuit pack (TN70B) functions as a buffer between the 32-bit DDSBS (serial-parallel converter) and the peripheral interface controller (PIC) circuit pack (TN61B), which is a 16-bit device. The BIC allows the 16-bit PIC to transmit and receive data from the higher capacity DDSBS at a rate that the PIC is able to accept. The BIC buffers data and commands to the PIC, buffers data and status information from the PIC, and performs the necessary handshaking protocols to communicate with the DDSBS.

4.30 The PIC consists of a controller circuit pack (TN61B) and a microcontrol store circuit pack (TN84). The microcontrol store is an 8K read-only memory (ROM) containing the PIC operational and diagnostic firmware. The controller circuit pack

includes a 4K random access memory (RAM) for data word storage as well as the necessary registers, interrupt circuits, and arithmetic/logic circuits to carry out the control functions. The PIC functions as a 16-bit, high-speed, bipolar microprocessor and, together with the BIC, multiplexes up to 16 separate peripheral controllers to the DDSBS interface. The PIC is capable of autonomously transferring blocks of data between the DMAC and peripheral controllers. An additional TN84 circuit pack can be added in the IOP basic unit of the processor system frame for additional PIC program memory.

4.31 The input/output microprocessor interface (IOMI) circuit pack (UN25B) serves to interface the 16-bit PIC with up to four communities of four PCs, which are 8-bit devices. A growth IOMI circuit pack can be added to the IOP basic unit in the processor control frame to provide for four more peripheral communities, which would be in addition to the two communities in the IOP basic unit and two growth communities in the growth unit.

4.32 Logic power for the IOP controller and all PC communities is controlled by the TN6 power control circuit pack (see Figure 8) located on the IOP basic unit on the processor control frame. The +5 V logic power for the IOP control portion and peripheral community 0 is supplied by a 495FA power unit H. The +5 V power for community 1 is supplied by an adjacent 494GA power unit J. The 495FA power unit G is provided for CPU growth and is not part of the IOP. Each community is equipped with a TN9 circuit pack that provides independent +12 V and –5 V power for the community peripheral controller memories and ±12 V power for communication interfaces.

E. Disk Storage System

4.33 The 3B20D Model 2 and Model 3 computers use microprocessor-based intelligent DFCs. The two types of DFCs discussed in this section are the SMD, and the SCSI.

SMD-DFC

4.34 The SMD - DFC consists of the following interrelated functional units:

- DDSBS
- BIC
- PIC
- MHDC
- WCS
- PDI.

4.35 The DFC (Figure 25) is a microprocessor-controlled peripheral unit that interfaces the CPU with as many as eight disk drives through a control cable. The DFC is duplicated for reliability, and either DFC can interface with the on-line or off-line CU.

The DFC itself is treated by the system as a peripheral device driven by a DMAC which facilitates the transmission of data blocks between the DFC and MAS. The physical location and arrangement of circuit packs comprising the SMD-DFC are shown in Figures 2, 3 and 9.

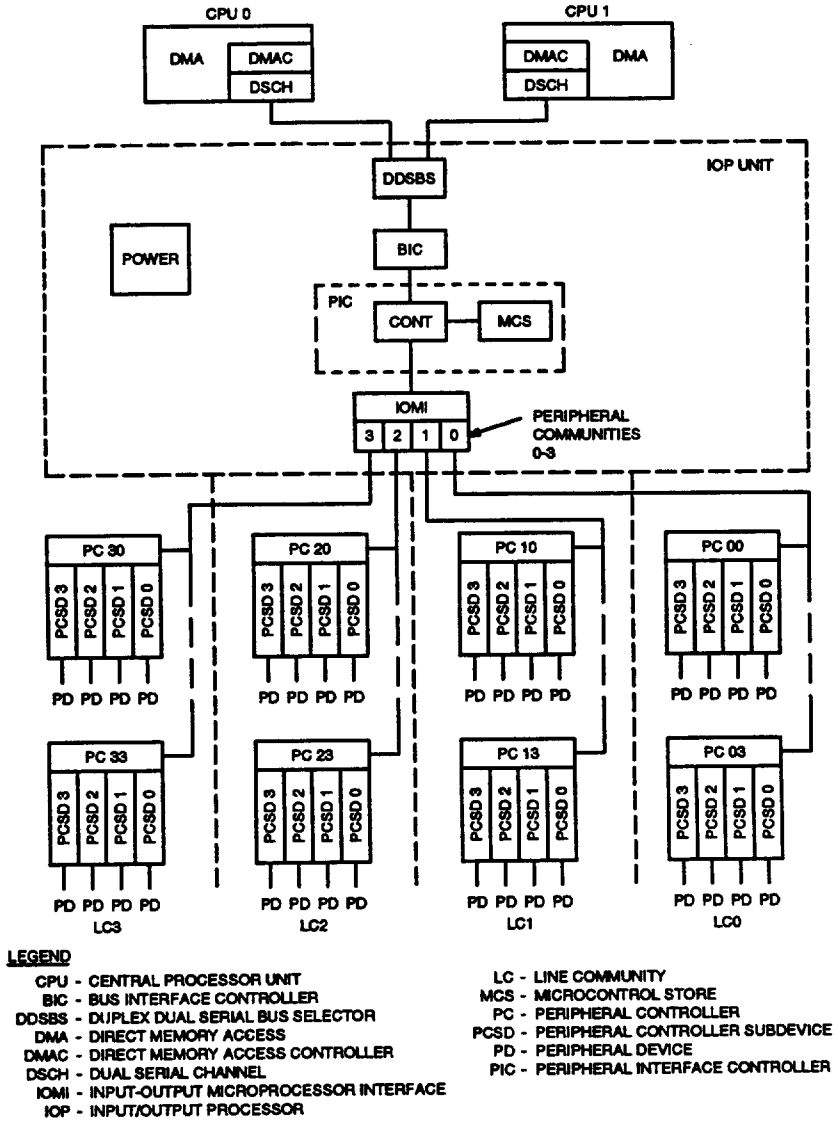
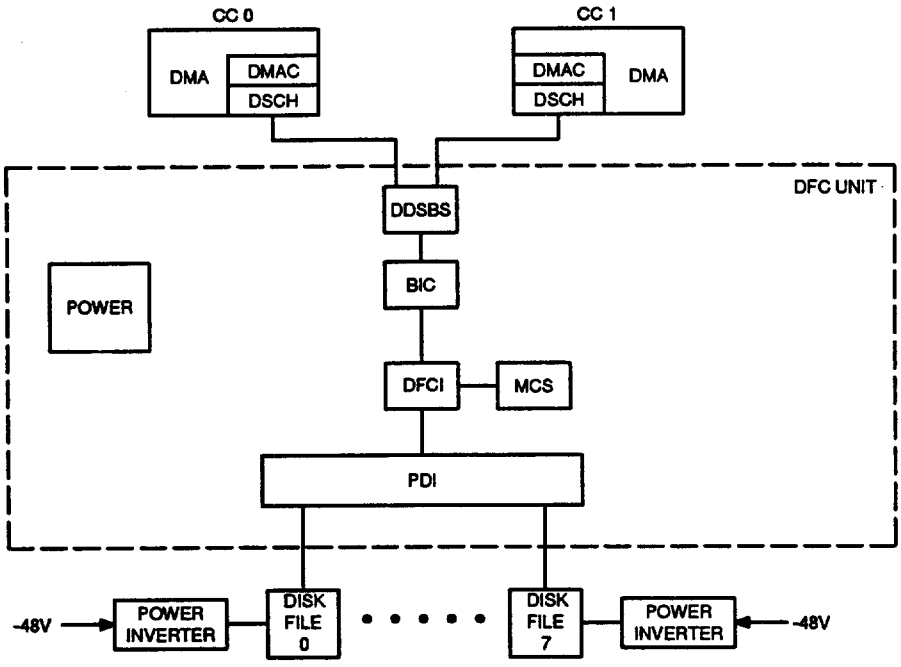


Figure 24. Input/Output Processor and Peripheral Controllers



LEGEND:

BIC - Bus Interface Controller
CC - Central Control
DDSBS - Duplex Dual Serial Bus Selector
DFCI - Disk File Controller Interface
DMA - Direct Memory Access
DMAC - Direct Memory Access Controller
DSCH - Dual Serial Channel
MCS - Microcontrol Store
PDI - Peripheral Device Interface

Figure 25. SMD Disk File Controller

4.36 The DFC (Figure 25) interfaces with a DMAC in both CUs via a DDSBS circuit pack (TN69B). These two identical serial interfaces allow either CPU-DMA to communicate with the DFC. The DDSBS converts the serial data from the DMAC to parallel format. A BIC circuit pack (TN70B) functions as a buffer between the 32-bit DDSBS (serial-parallel converter) and the disk file controller interface (DFCI) circuit pack (UN54/UN55), which is a 16-bit device. The DFCI contains a PIC circuit that functions as a microprocessor to perform all arithmetic, logic, and sequence operations for the DFC. The BIC allows the 16-bit PIC to transmit and receive data from the higher capacity DDSBS at a rate that the PIC is able to accept. The BIC buffers data and commands to the PIC, buffers data and status information from the PIC, and performs the necessary handshaking protocols to communicate with the DDSBS. Associated with the PIC is the microcontrol store (MCS). If the UN54 DFCI circuit pack is equipped, two TN68 MCS circuit packs, each containing 8K words of PROM, serve as the program store for the PIC microprocessor. If the UN55 DFCI circuit pack (available with *UNIX* RTR Operating

System Release 1) is equipped, one TN19 MCS circuit pack containing 16K words of erasable PROM (EPROM) is equipped. The peripheral device interface (PDI) circuit pack (UN64) contains a parallel-serial data interface and a MHD data/clock circuit. The parallel-serial data interface interfaces the PIC microprocessor (a parallel device) with the moving head disk data/clock circuit (a serial device). The data/clock circuit interfaces with the disk drives.

4.37 The 3B20D Model 2 computer disk drives may be either the KS-22072 300-Mbyte drives or the KS-22693 160-Mbyte drives or KS-22875, L10 340-Mbyte drives. When the 160-Mbyte drives are used with the UN54 DFC interface, a maximum of six drives per DFC can be used. When 300-Mbyte drives are used, as many as eight disk drives can be supported. Disk drives interface with the DFC by means of a control cable and individual read/write cables connected to each drive. The 3B20D Model 3 computer uses the 340-Mbyte disk drive only.

SCSI-DFC

4.38 The SCSI - DFC consists of the following functional units:

- DDSBS
- Host adapter (HA)
- SCSI bus.

4.39 The SCSI-DFC is interfaced to the central unit (CU) via the DSCH. The DFC connects to a DSCH in each CU via the DDSBS (Figure 26). Connecting a DSCH and DDSBS is a DSCH cable. Data and commands move between the CU and DFC via the DSCH cable.

4.40 The DDSBS also interfaces to the HA circuitry of the DFC. The HA functionally contains a BIC, control logic, and an interface to the SCSI buses. The BIC provides the interface between the HA control logic and the DDSBS.

4.41 The HA control logic interfaces to a SCSI bus via an SCSI Protocol Controller (SPC). The SPC interface handles the communication duties involved in moving data and commands between the HA and the disk drives attached to the SCSI bus.

4.42 Depending on option availability, there can be up to four SCSI-DFCs in a 3B20D computer configuration. Each DFC has two SCSI busses. Each SCSI bus can have up to four MHDs.

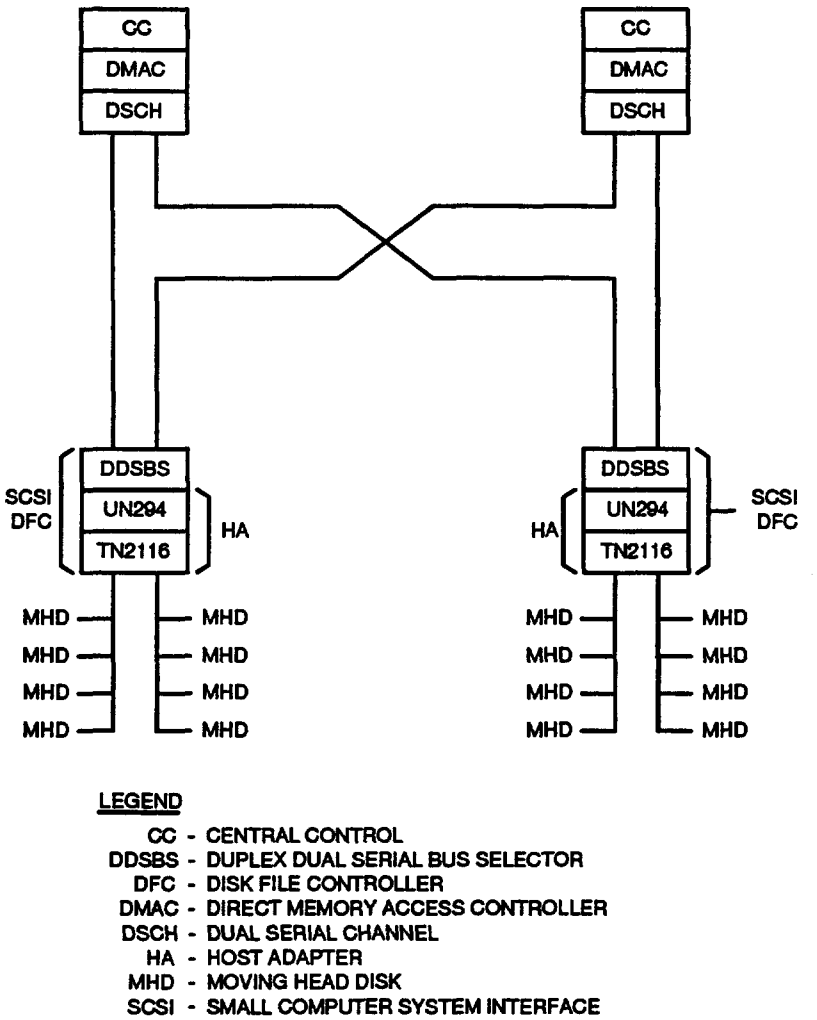


Figure 26. SCSI-DFC System Level Block Diagram

4.43 SCSI-DUP - The SCSI DUP is an enclosure that contains the SCSI disk drive, a fan for cooling, a power supply, and a power switch. Before being implemented on the 3B20D computer, a SCSI disk product must undergo rigorous testing, pass stringent environmental requirements, and meet critical timing and performance requirements.

4.44 SMD vs SCSI - The disk drives utilizing the SMD interface can only be attached to the SMD DFC and disk drives utilizing the SCSI interface can only be attached to the SCSI DFC. The SMD DFC can co-exist in the same 3B20D computer configuration with an SCSI DFC (Figure 27).

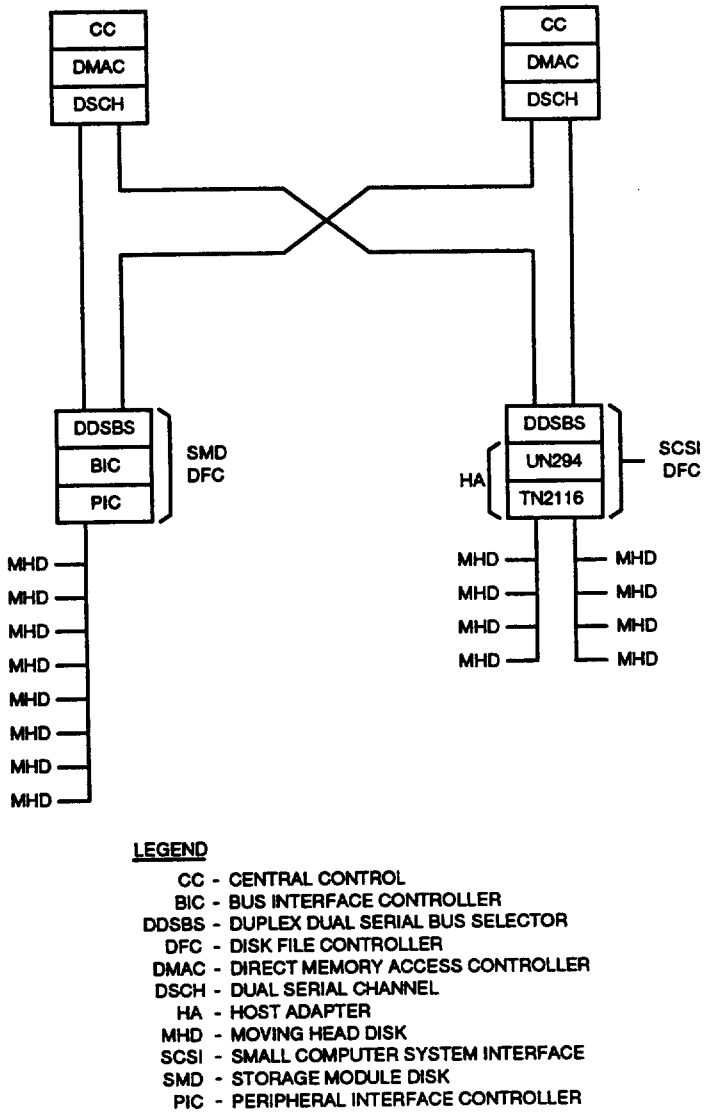


Figure 27. SMD/SCSI DFC Co-Existence Diagram

F. Magnetic Tape System

4.45 The tape unit is a manual load, reel-to-reel tape drive unit. It uses electronic circuits to control the movement of the magnetic tape between the supply reel and the take-up reel. The tape unit consists of the following functional areas:

- Formatter/control logic
- Read/write servo
- Read/write head assembly
- Pneumatic and cooling system
- Power supply and distribution.

G. Power Systems and Distribution

4.46 Primary power for the computer is –48 V dc obtained from an office battery or converter plant and distributed to the various frames in the system by a power distribution frame (PDF). The 3B20D Model 3 computer has the option of using the office power system or the power cabinets of Figure 18. The PDF may be a J86334B frame (Figure 28) that receives –48 V via cable pairs from the office battery plant or a J86334C frame (Figure 29) that receives two –48 V inputs from a converter plant. The two types of PDFs are summarized below:

(a) The J86334B PDF is supplied by –48 V from an office battery plant. The number of cable pair inputs from the plant is dependent on the size and configuration of the system. The frame may be equipped with a maximum of five distribution panels. The five panels may be any combination of 70-type fuse panels, 74- and KS-type fuse panels, or high-current fuse panels. A control panel assembly is provided on the PDF containing frame alarm monitoring circuits and charging circuits.

(b) The J86334C PDF is supplied by –48 V from a converter plant. It is identical in operation to the J86334B frame but contains capacitors for additional filtering.

4.47 The processor control frame receives distributed –48 V DC from the power distribution frame through a J1C147BE-1 power distribution unit located at the top of the frame. This unit contains fuses and terminal strips for convenient –48 V DC distribution through the frame. Distributed logic circuit power is provided by –48 V to +5 V power converters within the functional units (CPU, DFC, and IOP) of the processor frame. The distribution of +5 V DC is made directly to the multilayer backplane segment serving the unit.

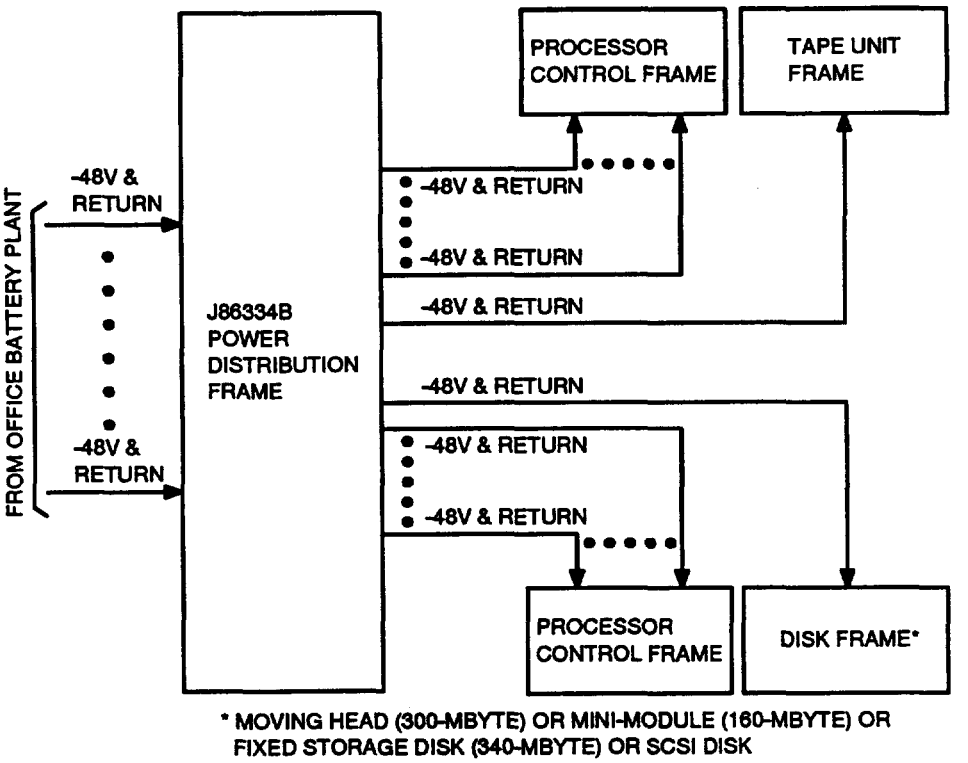


Figure 28. Block Diagram of Power Distribution Using J86334B Power Distribution Frame

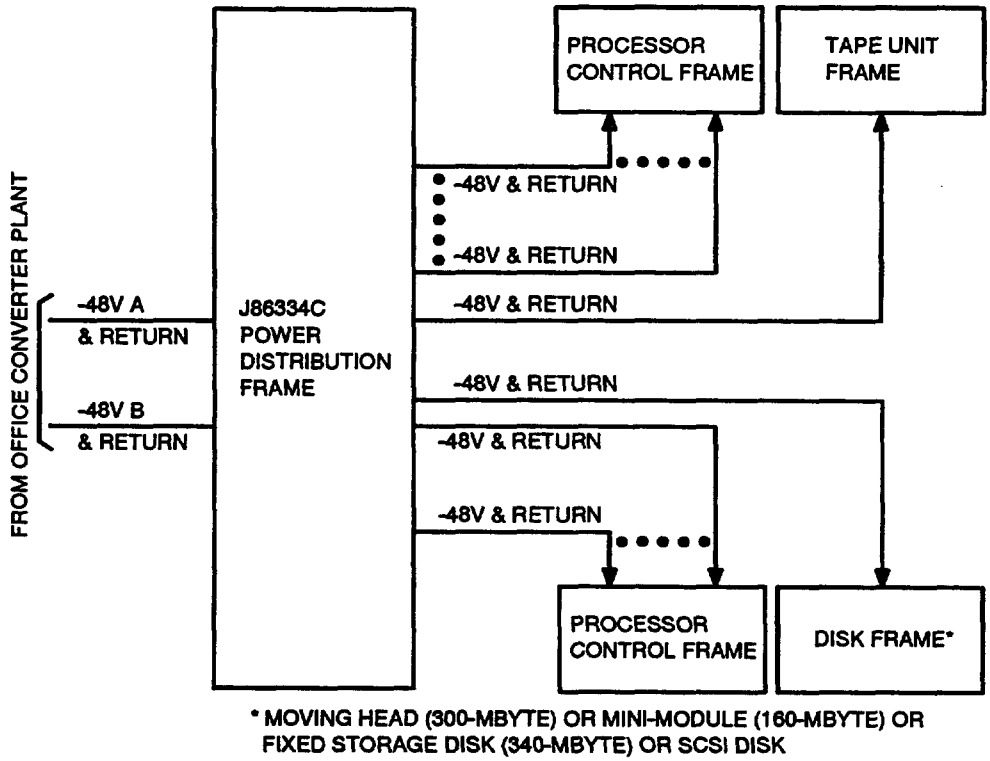


Figure 29. Block Diagram of Power Distribution Using J86334C Power Distribution Frame

4.48 Because power is distributed directly to the backplanes, fuses are not used. Instead, a feature called current programming is used to provide backplane protection. Each circuit pack has a resistor with a value related to the amount of current drawn by that circuit pack under normal conditions. The current programming resistors of all packs supplied by a given power converter are then wired together to form a parallel network. The network resistance value provides an indication to the converter of how much current it should normally expect to supply. If the converter senses it is supplying more current than the programming resistors indicate, the converter will shut down and generate an alarm signal.

4.49 From a power standpoint, the system consists of three functional units: CPU, DFC, and IOP. Each requires its own control/display facility. Such a facility is necessary to turn unit power on and off, to display power and alarm states, and to provide out- of-service request and display features. The TN5, TN3, and TN6 circuit packs shown in Figure 8 contain switches and indicators to provide this facility for the CPU, DFC (SMD), and IOP, respectively.

4.50 Each port switch subunit circuit pack is individually fused. The scanner/signal distributor interface circuit pack is a buffer circuit, which does not require fusing. The port switch unit contains a –48 V to +5 V converter that supplies logic power.

4.51 The computer may be equipped with either MHD drive frames or minimodule disk drive frames, tape/disk frames or SCSI disk cabinets. The MHD disk drive frame contains a KS-specification 300-Mbyte disk drive, 2000 VA inverter, and disk power control panel. The 300-Mbyte disk drive requires 208-V 60-Hz single-phase power, which is supplied by the inverter. Each inverter receives –48 V DC power from a dedicated 50-ampere fuse in the PDF. The minimodule disk drive frame contains from one to three KS-specification 160-Mbyte disk drives and from one to three 1200 VA inverters. Each disk drive requires 120-V 60-Hz single-phase power, which is supplied by the 1200 VA inverter. Each 1200 VA inverter receives –48 V DC power from a dedicated 50-ampere fuse in the PDF. A tape/disk frame may be equipped with up to eight 340 megabyte fixed storage disk drives. Each disk drive has its own KS-22927, L2 power supply to convert the –48 V DC power from the PDF to the dc voltages required for operation of the disk drive. The SCSI disk cabinet may be equipped with up to 16 SCSI DUPs. Each DUP has its own power supply which utilizes -48 vdc as input power.

4.52 The tape unit frame (see Figure 17) contains two KS-22762, tape transport units. Effective with *UNIX* RTR Operating System Release 1, the 3B20D Model 2 computer may be retrofitted with the KS-23113 tape transport unit, when the Model 2 computer is using the 340-Mbyte disk drives. This tape unit is part of the fast backup feature that is used to reload data to disk and dead start the system. The KS-23113 tape unit is standard for the 3B20D Model 3 computer. Both tape transport units require 120-V 60-Hz single-phase power. The KS-23113, L12 tape transport is capable of operating in two modes: a 25 inch per second start/stop mode, and a 75 inch per second streaming mode. Data is recorded in 1600 bits per inch phase encoded method and 6250 bits per inch group coded recording method.

H. ED-4C387 Cooling Unit

4.53 The cooling unit provides its own power switch, alarm features, and scan points. The cooling unit provides two scan points that are cabled directly to dedicated pins on a scanner circuit pack (UN33B). The first scan point signals a single fan failure, and the second scan point indicates multiple fan failures. The resulting alarm (single/multiple fan failures) is latched and can be reset by operating the ON/RESET switch or by activating the two SD points associated with the cooling unit under software control.

5. Fault Detection And Maintenance

5.01 The maintenance objective of the 3B20D Model 2 and Model 3 computers is to provide a system with a cumulative downtime of no more than an average of 2 hours per system over a 40-year period.

5.02 A duplex computer system is the primary method used to insure continuous system operation. The on-line computer keeps the off-line memory updated on each memory write so that it always agrees with the on-line memory. Extensive self-checking and equipment duplication provide an operating spare in case of serious fault. The basic fault recovery technique is to switch the off-line computer on-line. Once the faulty computer is off-line, further fault diagnostic and location procedures, both hardware and software, may be used.

5.03 The MCH is the circuit used to switch computers when an error occurs. The MCH is then used by the on-line computer to exercise and diagnose the off-line system. The MCH provides a serial channel link into the microcontrol structure of the computer. This provides maintenance and diagnostic access between the computers of a duplex system. The MCH functions in the same manner as a DSCH (same signaling but different control functions), although it is not considered to be a part of the I/O system.

5.04 Maintenance procedures are divided into nondeferrable and deferrable categories. Nondeferrable functions center around fault recovery, which might require a computer switch or removal of a DFC or IOP with a resulting equipment reconfiguration. Deferrable maintenance normally involves the man-machine interface since human intervention usually results in comparatively long downtimes.

5.05 An EAI is a part of the CPU and provides some manual control to be used primarily for troubleshooting, which requires forcing system configurations. The EAI unit is located in the central processor unit (see Figure 22). It has no controls of its own but instead accepts signals from the serial channel input and produces control signals to initiate certain operations. Indicators on the EAI unit provide status information to the craft person.

5.06 The maintenance TTY/video terminal and printer are provided to permit communication with the computer. The operator types commands on the terminal keyboard; status indications and return messages are displayed on the video terminal. Results of diagnostic tests may be printed out on the printer. The video terminal can display reversed video color and flashing characters and has a split-screen capability so that status messages and other long-term information can be continuously displayed on a part of the screen while other messages and displays may be placed on the other parts of the screen.

5.07 The video terminal connects to the computer through the MTTYPC and the EAI unit located in the CPU. Remote access to the computer through the EAI unit is made via a data link on a dedicated port in the MTTYPC.

A. Critical Indicator Administrator

5.08 Effective with *UNIX* RTR Operating System Release 1, critical indicators on the maintenance terminal can be routed to a terminal in a remote maintenance center (other than the switching control center). This feature requires growing a TN75 data link controller and changing the unit control block in the equipment configuration database. Software for this feature is available in the basic load.

B. Remote Terminal Printer

5.09 The remote terminal printer is an add-on feature for *UNIX* RTR Operating System Release 1. This feature permits an application to duplicate the maintenance terminal and the receive-only printer at a remote location. The remote maintenance terminal must have an intelligent printer port. This feature requires a dedicated TN74 teletypewriter controller in the IOP, sending and receiving data sets (modems), and the telephone line. The remote receive-only printer plugs into the terminal.

5.10 A microlevel test set is available to provide access to the microstore address bus, microstore data bus, maintenance channel bus, and bidirectional gating bus. This access is through a UN16B circuit pack in the CPU (see Figure 7). The microlevel test set provides a method of inputting microinstructions and monitoring operations of the computer. It is used only for installation testing or emergency testing.

5.11 In the event of a trouble condition, system outage, or other conditions that require manual intervention, an audible alarm alerts maintenance personnel that action is required. The audible alarm (critical, major, or minor) hardware is not provided by the computer. The computer provides alarm signals that application systems can use to activate the office alarm grid. The audible alarm is accompanied by a visual severity indication at the local maintenance position indicating the level of the alarm (critical, major, or minor). Other visual indications at the local maintenance position and output messages allow maintenance personnel to determine the source of the problem and the necessary corrective action.

6. Acronyms

6.01 The following acronyms are used in this practice:

ACHI	Application Channel Interface
BIC	Bus Interface Controller
CCIO	Central Control Input/Output
CAM	Cache Memory
CPU	Central Processor Unit
CSB	Cache Store Board
DFC	Disk File Controller
DFCI	Disk File Controller Interface
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DMU	Data Manipulation Unit
DUP	Disk Unit Package
DSCH	Dual Serial Channel
DDSBS	Duplex Dual Serial Bus selector
EMM	Extended Main Memory
EAI	Emergency Action Interface
EPROM	Erasable Programmable Read Only Memory
HA	Host Adaptor
I/O	Input/Output
IOP	Input/Output Processor
IOMI	Input/Output Microprocessor Interface
MAS	Main Store
MASA	Main Store Array
MASC	Main Store Controller
MASU	Main Store Update
MCH	Maintenance Channel
MCS	Microcontrol Store
MHD	Moving Head Disk

MLTS	Microlevel Test Set
MTTYPC	Maintenance Teletypewriter Peripheral Controller
PC	Peripheral Controller
PDI	Peripheral Device Interface
PIC	Peripheral Interface Controller
PMS	Programmable Microstore
PROM	Programmable Read Only Memory
RAM	Random Access Memory
ROM	Read Only Memory
SCSI	Small Computer System
SMD	Storage Module Disk
SAT	Store Address Translator
SAC	Store Address Control
SDC	Store Data Control
TTY	Teletypewriter
VLMM	Very Large Main Memory
WMS	Writable Microstore

7. References

7.01 The following is a list of references that may be used to obtain more information about the SCSI feature.

- AT&T 254-302-216
  AT&T 3B20D Model 2 and 3 Computers
  Small Computer System Interface Disk File Controller
  Description And Theory of Operation
- AT&T 254-302-213
  AT&T 3B20D Computer
  Small Computer System Interface Disk Unit Package
  General Description
- AT&T 254-302-020
  AT&T 3B20D Model 2 And Model 3 Computers
  Power Systems
  Description And Theory Of Operation

How Are We Doing?

Document Title: AT&T 3B20D Computer General Description

Document No.: 254-302-005 Issue 6 Date: February 1992

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