INPUT-OUTPUT PROCESSOR
DESCRIPTION AND THEORY OF OPERATION
3B2OD MODEL 2 PROCESSOR

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1. GENERAL

1.01 This section provides a physical and functional description and theory of operation of the input-output processor (IOP) used in the 3B20D Model 2 processor.

1.02 Whenever this section is reissued, the reason(s) for reissue will be listed in this paragraph.

1.03 The IOP serves as an interface between a variety of peripheral units and the central control (CC). The IOP is a flexible peripheral which provides:

- An interface between terminals, data links, other small peripheral units, and the CC
- An autonomous input-output (IO) function via the direct memory access (DMA) into the main store (MAS)
- Autonomous controls for the transfer of data blocks to and from peripheral devices (PDs)
- Buffering and data formatting as required by the different PDs
- A common software driver for all IOP peripherals.

1.04 The IOP interfaces the 3B20D Model 2 processor with as many as four groups of four peripheral controllers (PCs) (Fig. 1). Transfers of data between the PCs and MAS are made without requiring CC functions. This reduces real-time requirements on the CC and increases the effectiveness of the CC as a system controller.

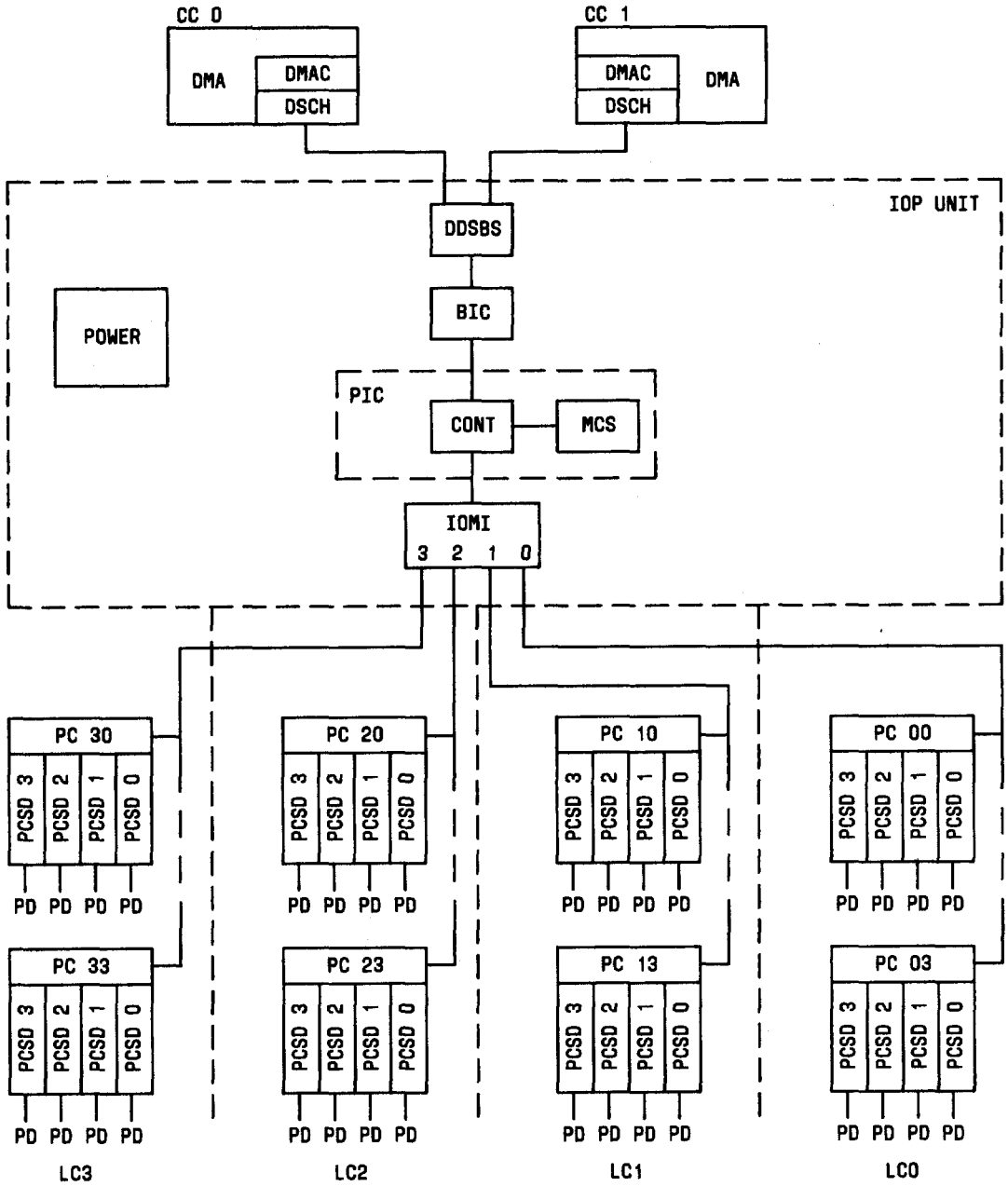
1.05 The IOP is connected to the CC via a dual serial channel (DSCH) associated with a direct memory access controller (DMAC) in the DMA IO unit. The DMAC facilitates transmission of data blocks between the IOP and MAS.

1.06 There are two IOP units, a basic unit and a growth unit. The growth unit is used with the basic unit to expand the capability of the basic unit.

2. PHYSICAL DESCRIPTION

2.01 The IOP basic unit (J1C147BD-1) and growth unit (J1C147BC-1) are housed in the processor control frame (Fig. 2). The basic unit and growth unit are approximately 22-1/2 inches wide and 15-1/4 inches deep. The basic unit is 16 inches high, and the growth unit is 10 inches high. Both units are mounted in 24-inch-deep frames with 11-inch-wide uprights. The frames are standard size (2 feet, 2 inches wide and 7 feet high).

2.02 The IOP basic unit contains the peripheral interface controller (PIC) and PC communities 0 and 1. The IOP growth unit contains PC communities 2 and 3. Power units are integrated within each of the two (0 and 1, 2 and 3) communities.



KEY

CC - CENTRAL CONTROL
BIC - BUS INTERFACE CONTROLLER
DDSBS - DUPLEX DUAL SERIAL BUS SELECTOR
DMA - DIRECT MEMORY ACCESS
DMAC - DIRECT MEMORY ACCESS CONTROLLER
DSCH - DUAL SERIAL CHANNEL
IOMI - INPUT-OUTPUT MICROPROCESSOR INTERFACE
LC - LINE COMMUNITY
MCS - MICROCONTROL STORE
PC - PERIPHERAL CONTROLLER
PCSD - PERIPHERAL CONTROLLER SUBDEVICE
PD - PERIPHERAL DEVICE
PIC - PERIPHERAL INTERFACE CONTROLLER

Fig. 1—Input-Output Processor Configuration

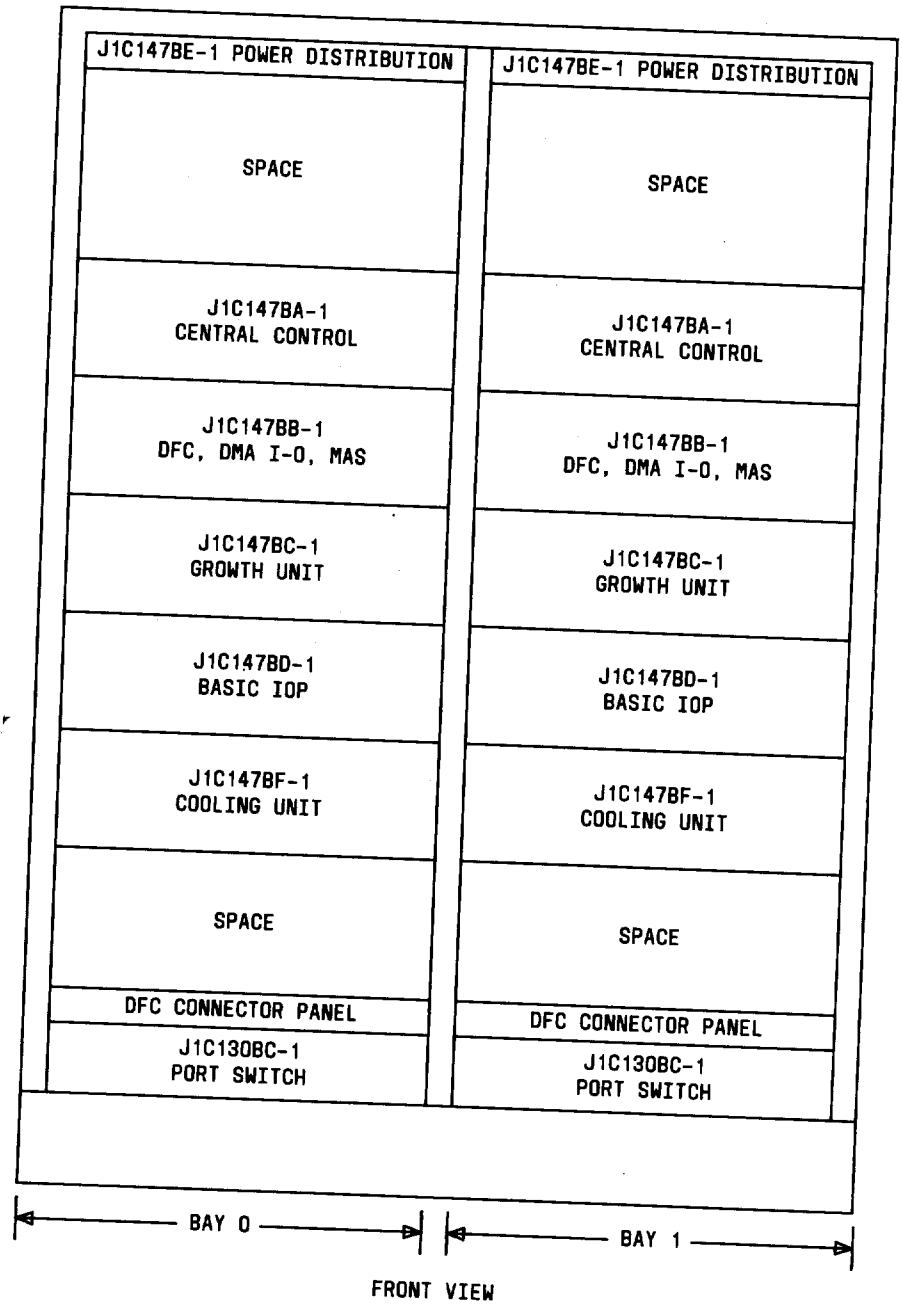


Fig. 2—Processor Control Frame

2.03 The IOP basic unit (Fig. 3) is made up of the following circuit packs:

- Input-output microprocessor interface (IOMI) (UN25)
- Peripheral interface controller (PIC) (TN61)
- Microcontrol store (MCS) (TN84)
- Bus interface controller (BIC) (TN70)
- Duplex dual serial bus selector (DDSBS) (TN69)
- IOP power control (TN6)
- Peripheral controller communities (0 and 1).

Each peripheral community is equipped with TN9 circuit packs, which provide independent +12V and −5V power for peripheral controller memories and +12V and −12V power for communication interfaces. The 495FA power converter on the right side of the unit (Fig. 3) provides 5V logic power for the IOP control portion and PC 0. The 495GA power converter on the left side of the unit is used for the IOP growth unit.

2.04 The IOP basic unit also provides space for a growth UN25 circuit pack and a growth TN84 circuit pack, although the MCS currently does not support this growth. The growth UN25 circuit pack can interface with a maximum of four peripheral controller communities.

2.05 The IOP growth unit is arranged to handle two more peripheral communities (2 and 3). Each community in the growth unit is supplied with +12V and −5V power by the TN9 circuit pack. The 495FA power converter on the left side supplies +5V logic power for both peripheral communities. The 495FA power converter on the right side can supply all power for the IOP growth portion depending on the way the MAS or dual access memory-IO is equipped.

2.06 The cooling unit (J1C147BF-1) is comprised of four plug-in fans. These fans provide filtered air without a common plenum between the modules. The fans are equipped on two trays, two fans per tray. The two trays plug into a common plenum. When a fan fails, the common plenum design allows the remaining three fans to partially replace the cooling provided by the broken fan. The cooling unit provides its own power switch, alarm features, and scan points. The major alarm, which is given for any fan failure, will be latched and can be reset by power-cycling the fan unit. The cooling unit provides two scan points that can be cabled directly to a scanner circuit (UN33 circuit pack). The first scan point signals a single fan failure; the second scan point indicates that more than one fan has failed. All fans can be cabled to the same two scan points or to different sets of two scan points.

3. FUNCTIONAL DESCRIPTION

3.01 The IOP functions as a front-end processor to control IO transfer between the MAS and various peripheral units, thereby reducing the load on the CC. A 16-bit bipolar microprocessor, called the PIC, interfaces the CC (via DDSBS, DSCH, and DMAC) with up to four PC communities. Each PC community contains four individual PCs, and each PC can be equipped with one to four peripheral controller subdevices (PCSDs). The PIC autonomously transfers blocks of data between PCs and the MAS. Additionally, the driver program and the PIC communicate via protocol tables stored in the MAS to initiate jobs and report job completion.

EQUIPMENT LOCATIONS	016	026	032	038	046	054	062	072	078	086	094	102	110	118	126	132	138	142	148	154	162	178
GUIDE POSITIONS	6	11	14	17	21	25	29	34	37	41	45	49	53	57	61	64	67	69	72	75	79	87
	495FA	494GA	TN9	PC13	PC12	PC11	PC10	TN9	PC03	PC02	PC01	PC00	UN25B	UN25B (OPTIONAL)	TN61B	TN84	TN84 (OPTIONAL)	TN60B	TN70B	TN69B	TN6	495FA

Fig. 3—Input-Output Processor Basic Unit

3.02 Essentially, an IOP consists of the following units:

- Duplex dual serial bus selector (DDSBS)
- Bus interface controller (BIC)
- Peripheral interface controller (PIC), which consists of a controller (CONT) and 8K words of microcontrol store (MCS)
- Input-output microprocessor interface (IOMI)
- Peripheral controller that controls up to four peripheral controller subdevices (PCSDs).

A. Duplex Dual Serial Bus Selector

3.03 The DDSBS (Fig. 4) provides a duplex interface between the peripheral unit BIC and DSCH in CC units 0 and 1. The DSCH can interface with up to 16 peripheral device DDSBSs. Private 2-bit serial links are employed to transfer data, status, and control information between the CC and the IOP. The CC always serves as the bus master, initiating an IO operation by serially transmitting job control information (called a start code) to the DDSBS. The DDSBS converts the serial information into a parallel form and decodes it to determine the operation type. After transmission of the start codes, serial data is transferred either to or from the CC as specified by the start codes. Additionally, the DDSBS always returns job completion information (called the return code) to the DSCH to report the success or failure of the operation. An asynchronous "handshaking" protocol is employed by the DDSBS and BIC to transfer data, commands, and status over a parallel 32-bit bus. A read-only memory (ROM) sequencer on the DDSBS serves to control all DDSBS/BIC transfers. An additional private serial link per DDSBS is also used to request DMA service or to interrupt the CC.

B. Bus Interface Controller

3.04 The BIC buffers processor data and commands to the PIC as well as data and status information from the PIC (Fig. 5). It also performs the mandatory "handshaking" to communicate with the DDSBS. The BIC allows the 16-bit PIC to transmit and receive data from the higher capacity 32-bit DDSBS at a rate the PIC is able to accept. The BIC verifies the integrity of data transferred between the DDSBS and BIC and the PIC and BIC via byte parity checks. The BIC 16-word by 32-bit data first-in-first-out (FIFO) register can be alternately accessed by the PIC and DDSBS for the transfer of data. The BIC contains a 32-bit command register that records processor commands to the PIC. The BIC also contains a 16-bit status flag register and a 16-bit error flag register. The status flags are used to request an interrupt or DMA service from the processor and to inform the PIC of a processor command or request for data transfer. The error flag records the occurrence of errors and aids in fault resolution and recovery. The PIC sanity and interval timing is also performed by the BIC.

C. Peripheral Interface Controller

3.05 The PIC consists of a controller (TN61) and one 8K-word MCS (TN84) circuit pack. The controller transfers data between internal registers and the various registers on the BIC and IOMI over a 16-bit data bus. The register to be gated onto the bus and the register being loaded from the bus are specified by the PIC. The PIC (Fig. 6) contains an arithmetic and logic unit, an 8-level interrupt unit, a 16-word general register file, a 4K-word data store, and a microcontroller sequence and pipe-line register. One 8K by 40-bit MCS pack stores the PIC operational and diagnostic firmware.

3.06 Associated with the PIC are the ROM emulator (WR1) and trace control unit (TN60) circuit packs. The ROM emulator and trace system (RETS) supports the PIC as a test tool during hardware and firmware debugging. The RETS also has hardware control over the PIC, providing program single-stepping and break-pointing capabilities. Program memory can be examined and modified under manual control or via a microprocessor development system (MDS). The RETS is equipped with three 16-bit by 256-word trace memories. One of the three is not dedicated and may be assigned by the user.

D. Input-Output Microprocessor Interface

3.07 The IOMI links the PIC to a maximum of four PC communities (Fig. 7) with four PCs per community. Each community interface with IOMI has a 16-bit dual port memory address, an 8+1 parity bit bidirectional data bus, and eight control pulses. Five private signals are used to establish an individual interface between each PC and the IOMI. Two of the private signals allow for a particular PC to be selected and permit the PC to indicate to the PIC the acknowledgement of the signal and when it was received. The remaining three private signals are used to report errors or to request service. The data, address, and control signals, which branch to each of the four communities, are driven from three common registers.

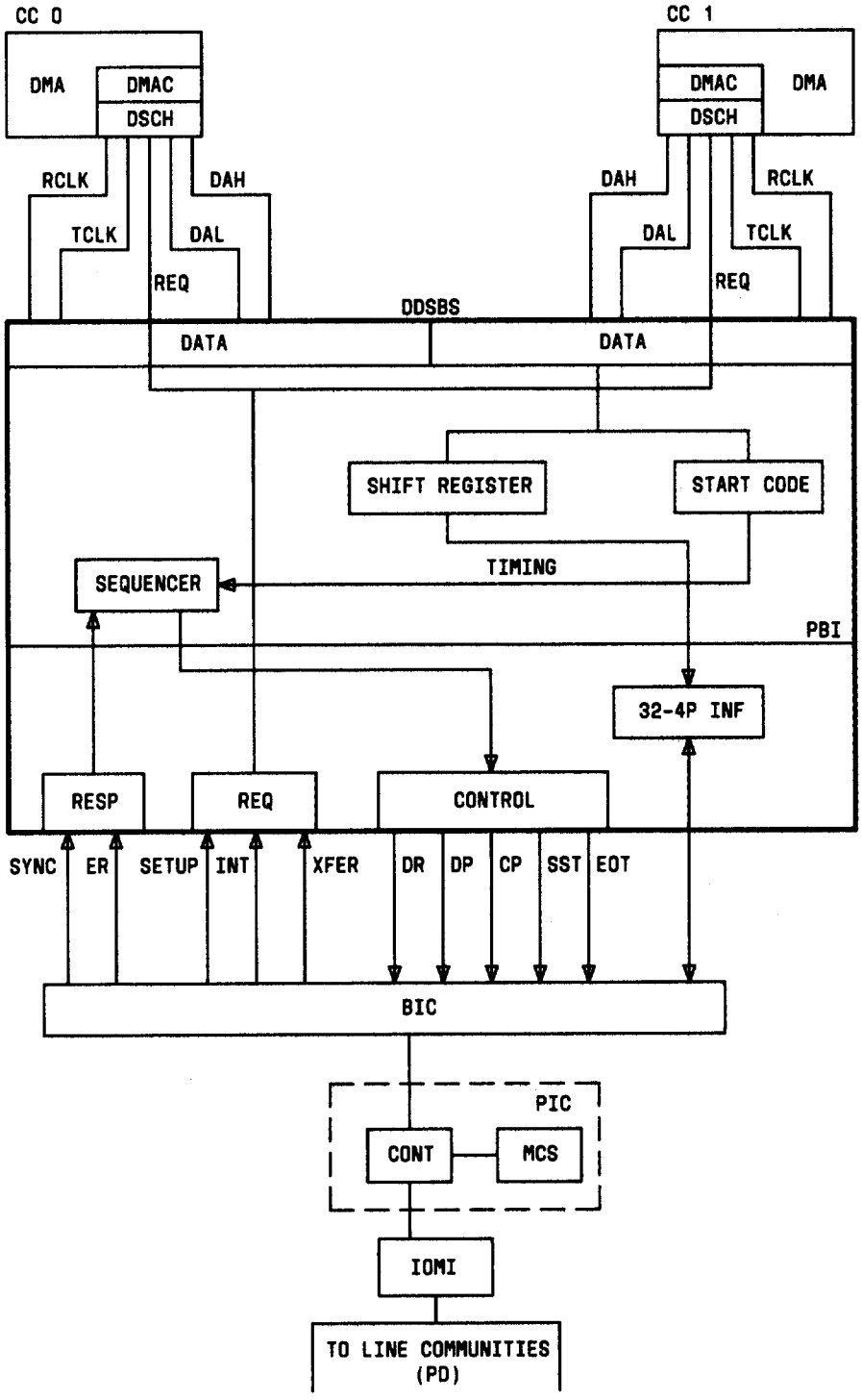


Fig. 4—Duplex Dual Serial Bus Selector Block Diagram

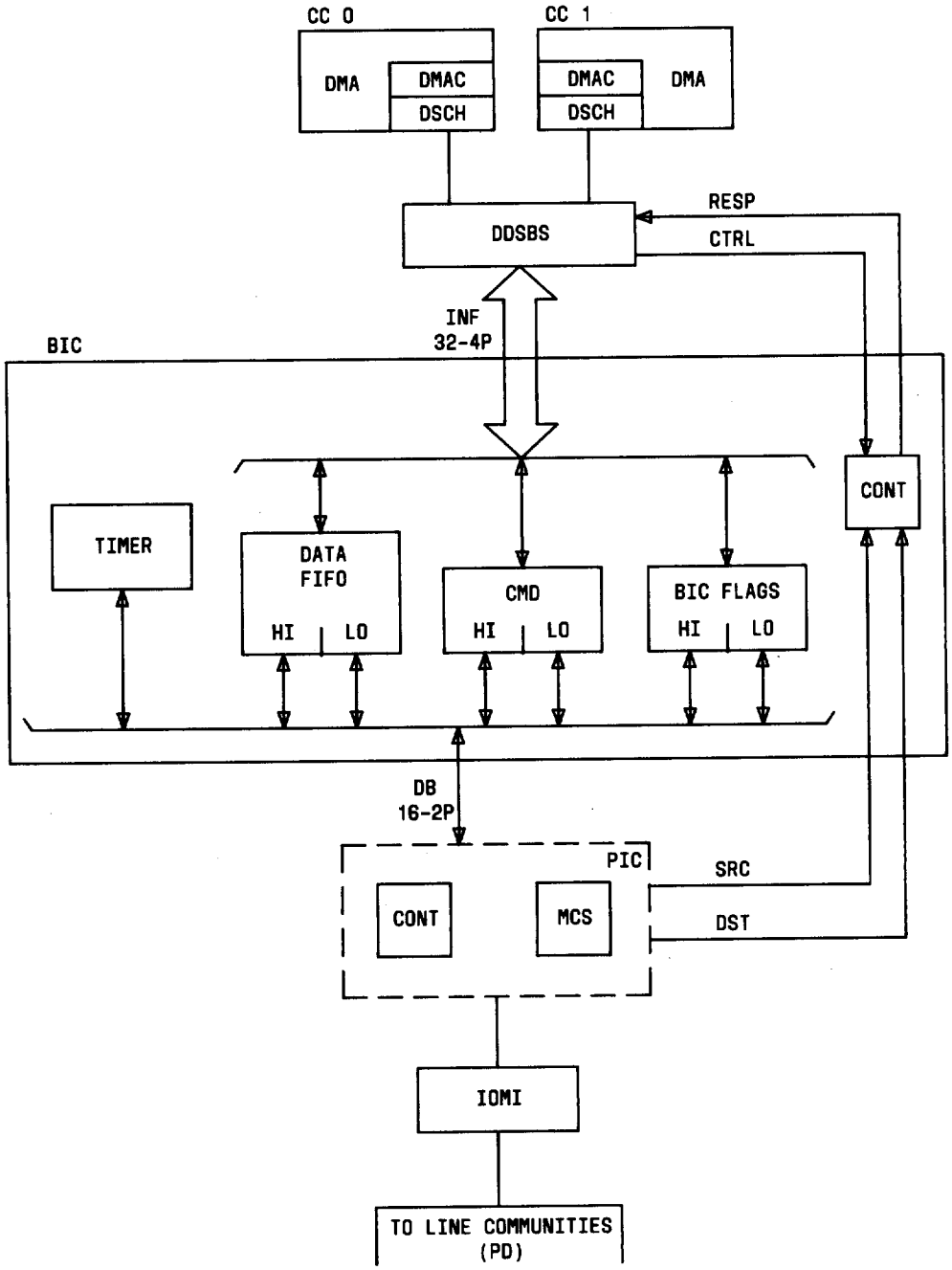


Fig. 5—Bus Interface Controller Block Diagram

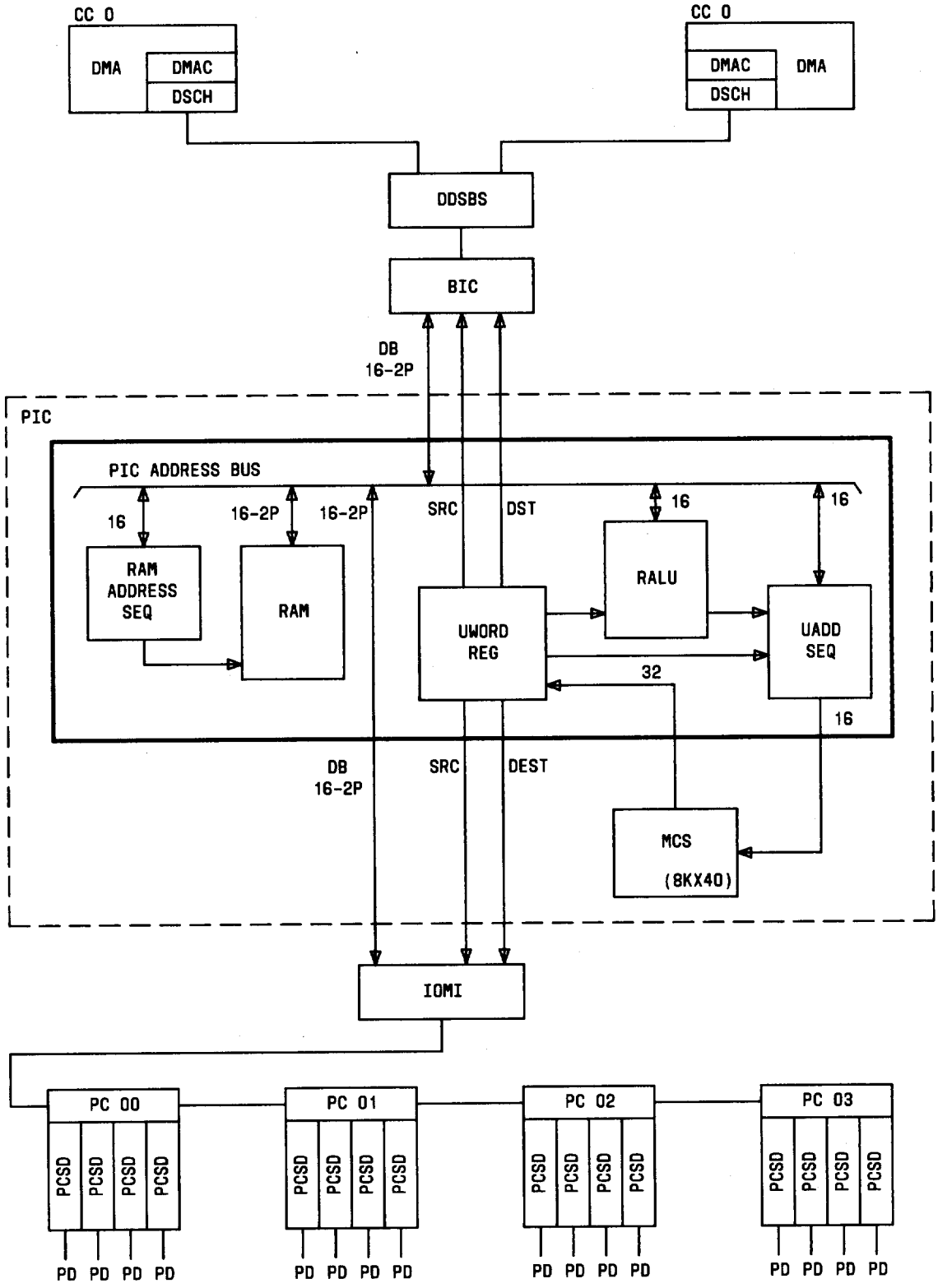


Fig. 6—Peripheral Interface Controller Block Diagram

E. Peripheral Controller

3.08 A PC may be either a TN or UN coded circuit pack. Both UN- and TN-type PCs are compatible with backplane power and ground pinouts in any of the dedicated PC locations. The PCs are microcomputer systems that interface between the PIC and slow-to-medium speed peripheral devices (Fig. 8).

3.09 All PCs have the same communication protocol with the PIC. The PC interprets commands from the PIC and effects the required action. The PIC can address up to four subdevices per PC. The subdevices activate a service or interrupt request to transfer data to or from main memory and report job completion. The interrupt request is used for high priority jobs, and the service request is used for base priority jobs. Any correspondence between the PIC and PC is done through the dual access memory located on each PC. The dual access memory enables the PC to accept commands from the PIC for data transfers, error detection, and fault recovery.

4. INTERFACE

4.01 The ICP interfaces the CC via the DMA IO unit and its periphery (Fig. 1). The DMA IO unit consists of a DSCH and a DMAC. The DMA IO unit is located in the processor control frame. The DDSBS is located in the processor control frame and is considered part of the IOP. The DDSBS interfaces the IOP with the DSCH. The DSCH interfaces the DDSBS with the DMAC, and the DMAC interfaces the DSCH with the 3B20D Model 2 processor via the DMA.

4.02 Interfacing between the IOP and the PDs is provided by the PCs. The PC is a single-board microprocessor which functions as an intelligent interface between the IOP controller and slow-to-medium speed peripheral units (up to four per PC).

A. Direct Memory Access Controller

4.03 The central control input-output (CCIO) bus provides the interface between the CC and DMAC over which the CC writes and reads the DMAC tables using the DMAC channel address data. Also, the IO orders to the PDs (connected to the DSCH) are executed by the channels after receiving data from the CC via the DMAC and DSCH. Separate buffers are provided in the DMAC for data and status information gated to or received from DSCHs.

4.04 Interfacing between the DMAC and the DSCH is provided by the DMA IO bus. The lead number and designation of this bus are similar to the lead number and designation of the CCIO bus. The DSCH service requests are individually wired into a priority resolution circuit in the DMAC.

B. Dual Serial Channel

4.05 The DSCH interfaces the CC via the CCIO bus and the PDs via 5-pair private serial data cables. One set of these cables is required for each PD (a maximum of 16). These cables contain two bidirectional data leads, a transmit clock, a receive clock, and a request lead. The DSCH interfaces the DMAC via the DIO bus.

C. Duplex Dual Serial Bus Selector

4.06 The DDSBS is interfaced with the DSCH via two bidirectional data leads, a transmit clock lead, a receive clock lead, and a request lead. The DDSBS is interfaced with the PD via the PBI which uses a bidirectional data bus (32 data bits and 4 parity bits), control leads (command present, data present, data request, sense status, and end-of-transfer), and response leads (sync, error, data transfer, DMA setup, and interrupt). The transmit clock from the DSCH may be 20 MHz for cable distances (between the DSCH and DDSBS) of up to 100 feet and 10 MHz for cable distances of up to 250 feet (a backplane option strap is required). (The IOP backplane is currently optioned for 20-MHz operation).

5. THEORY OF OPERATION

5.01 The IOP consists of the following subunits:

- Duplex dual serial bus selector
- Bus interface controller
- Peripheral interface controller, which consists of a PIC controller and 8K words of microcontrol store
- Input-output microprocessor interface
- Peripheral controller.

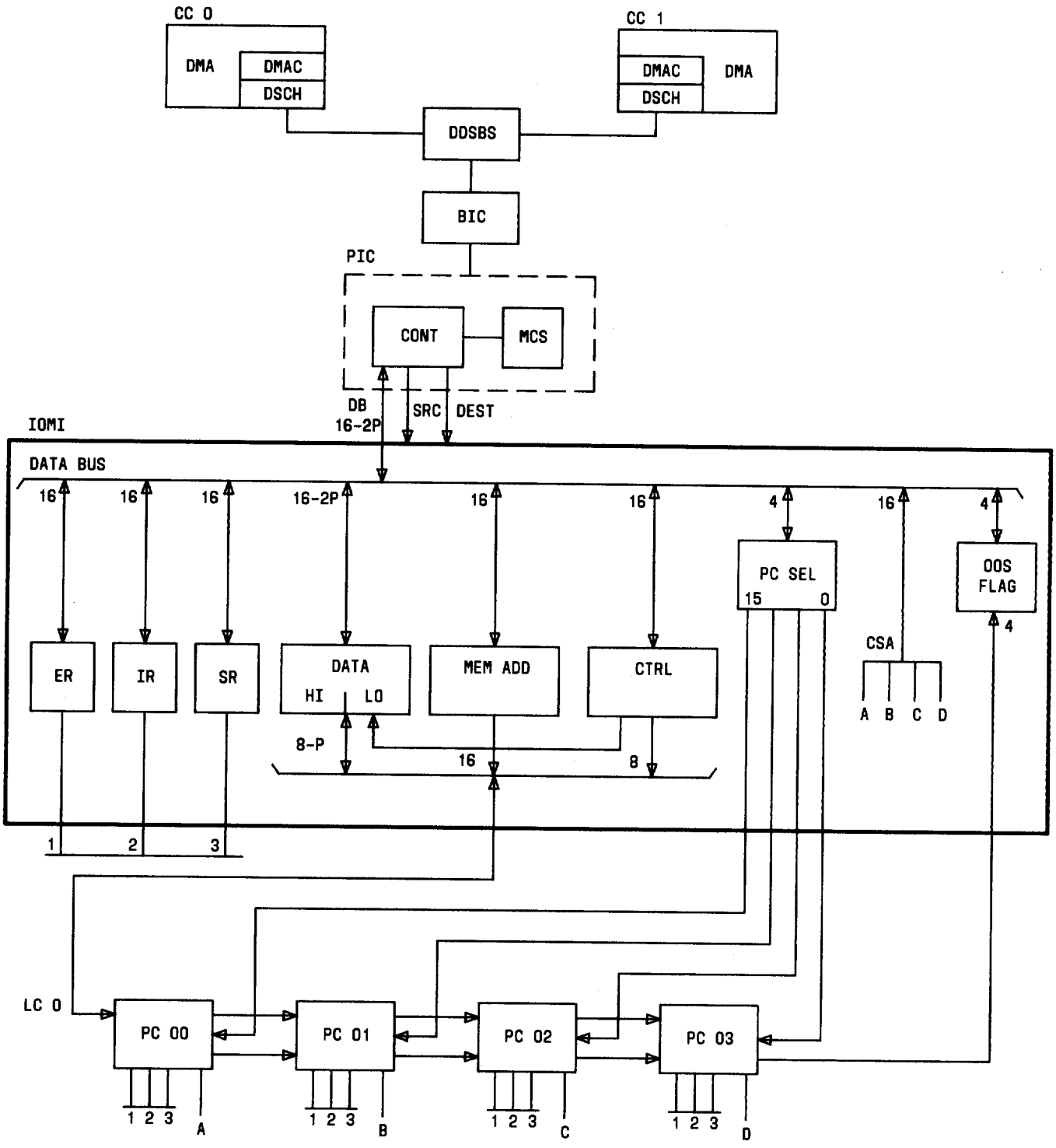


Fig. 7—Input-Output Microprocessor Interface Block Diagram

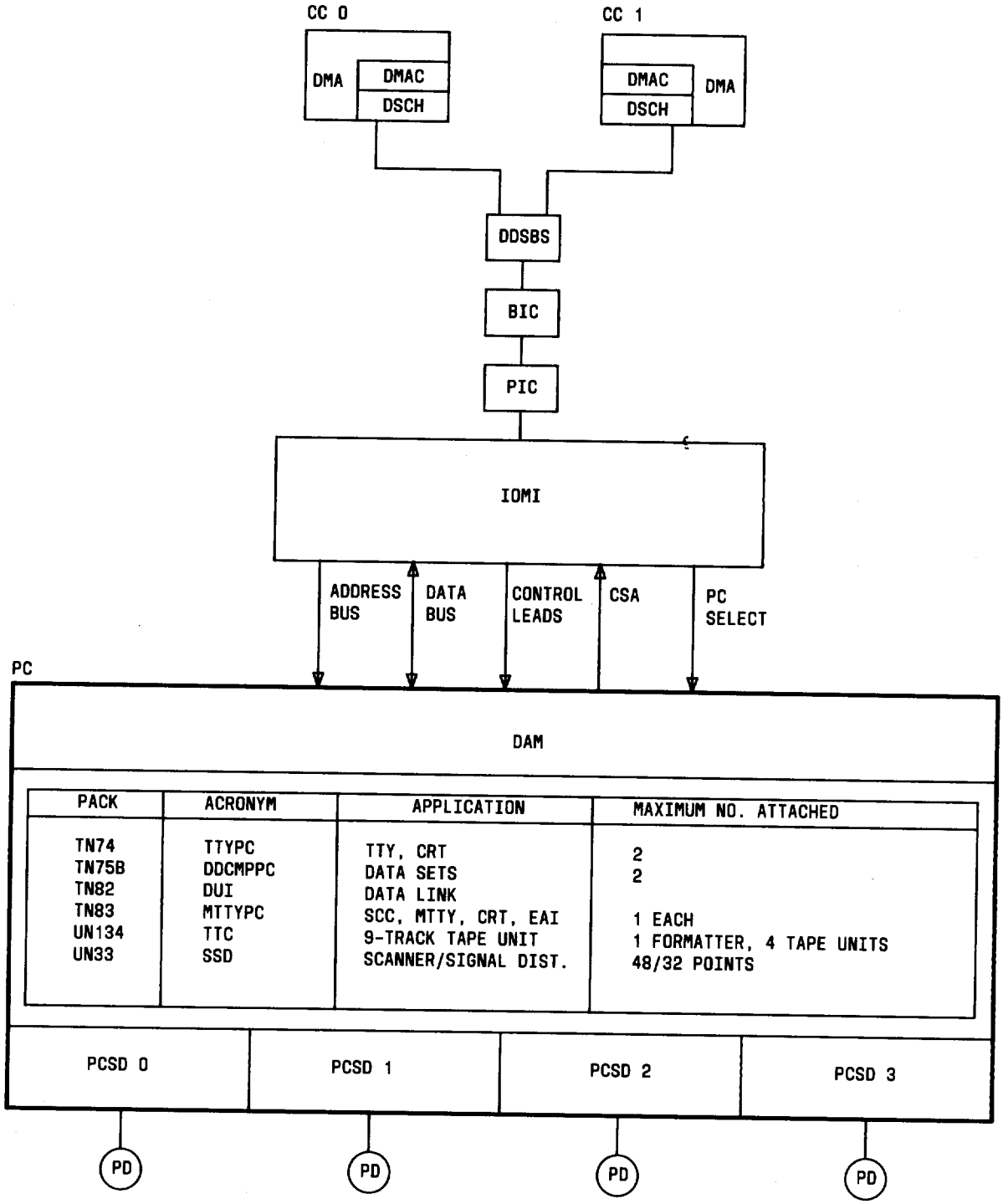


Fig. 8—Peripheral Controller

A. Duplex Dual Serial Bus Selector

5.02 The DDSBS functions as the interface between the IOP and the DSCH (Fig. 4). Two ports are provided on the DDSBS to facilitate duplex access to the IOP (ie, can be accessed by either CC). Each DDSBS interfaces the DSCH via two bidirectional data leads, a transmit clock, a receive clock, and a request lead. Data is simultaneously transferred via both data leads in conjunction with either transmit or receive clock pulses.

5.03 Identical start codes transmitted on each channel data lead identify the beginning of a message. All start codes begin with logic 1 followed by a 1-out-of-3 code. Three start codes are available: 0011 (3), 0101 (5), and 1001 (9). The start codes transmitted to the DDSBS specify the operation to be performed. The start codes are listed in Table A.

TABLE A

START CODES

HIGH	LOW	OPERATION
0011	0011	Write data (word mode)
0011	0101	Send device command
0011	1001	Write data (block mode)
0101	0011	Read data (word mode)
0101	0101	Sense status
0101	1001	Read data (block mode)
1001	0011	Signify end of transfer

5.04 Identical return messages from the DDSBS to the CC (via DSCH and DMAC) are coded to specify the success or failure of the operation. The return codes are listed in Table B.

5.05 The DDSBS receives and decodes incoming serial data, executes the specified operation with the BIC, and transmits serial reply data to the DSCH. Each DDSBS has a peripheral bus interface

TABLE B

RETURN CODES

HIGH	LOW	DEFINITION
0011	0011	All seems well
0011	0101	Device reported error
0101	0011	Invalid DDSBS command
0101	0101	Illegal start code received

(PBI) to interface the peripheral device with the DDSBS. The PBI consists of 46 active low transistor-transistor logic (TTL) signals which are: 36 directional data leads, 5 control signals, and 5 response signals.

5.06 ***Peripheral Bus Interface Signals:*** The 36 bidirectional data leads are used to send data or commands to the IOP or to receive data or status from the IOP. The data path is four bytes wide (eight bsits and one parity bit per byte for a total of 36 bits). Parity is odd over each byte and even over the entire 4-byte word.

5.07 The CC sends control signals to the IOP via the DDSBS PBI over five control leads:

(a) ***Command Present (CP):*** The IOP is instructed to interpret the contents on the data information (INF) leads as an IOP command.

(b) ***Data Present (DP):*** The IOP is instructed to interpret the contents on the data INF leads as data.

(c) ***Data Request (DR):*** The IOP is requested to gate its data onto the data INF leads.

(d) ***Sense Status (SST):*** The IOP is requested to gate its status onto the data INF leads.

(e) ***End of Transfer (EOT):*** The DMAC sends this signal to the IOP to signify the end of a DMA data block transfer.

5.08 The IOP responses are gated to the DDSBS on five response leads:

(a) ***Synchronization (SYNC):*** Upon reception of a control signal, the IOP performs the speci-

fied operation and sets the SYNC lead. The SYNC signal is cleared (inactive) in response to the removal of the control signal.

(b) ***Error (ER):*** The IOP sets the ER lead whenever an abnormal condition has been detected. The DDSBS checks the ER lead after reception of the SYNC signal.

(c) ***Interrupt (INTP):*** When the IOP requests CC actions (used to report job completions and detection or errors), it sets the INTP lead as an indication to the CC of its request.

(d) ***Transfer (XFER):*** The IOP sets the XFER lead to signal the DMAC that it is ready to send or receive another word during an autonomous DMA block transfer.

(e) ***SETUP:*** The IOP initiates a DMA setup by activating its SETUP lead. The DMAC will acknowledge the request by transmitting the data request control signal to retrieve the setup information.

5.09 Data transfers may be performed in one of two modes: 32-bit word mode or 16-word block mode. When operating in the 32-bit word mode, write operations require 23 shift cycles for transmission (4-bit start code, 16-bit data, two parity bits, and one lead cycle between data and the start code, simultaneously transmitted over both serial links). Four shift cycles are required for reception. The read operations require 4 shift cycles for transmission and 23 shift cycles for reception. Data signals are transmitted in a nonreturn-to-zero format.

5.10 When operating in the 16-word block mode, a single start code and a single return code will accompany 16 data words, each word containing 32 data bits and 4 parity bits. Each data word is separated by a single bit cell of dead time to facilitate transferring the next data word between its shift register and its FIFO buffer (in the DSCH and BIC). The IOP interrupt and DMA requests are received by the DSCH (via DDSBS) over the single request lead. Pulse-width modulated signals are used to make a service or interrupt (maintenance) request. Two types of service requests are provided to accommodate DMA transfers (DMA setup request and DMA data transfer request). An XFER request generates a 150-nanosecond-wide pulse, a setup request generates a 350-nanosecond-wide pulse, and an interrupt request generates a 550-nanosecond-wide pulse. Special circuitry is provided in the DDSBS to resolve conflicts caused by simultaneous multiple request. Included in the DSCH circuitry are three 16-bit registers which store mask bits to individually inhibit requests from each of the 16 PDs it controls. When masked, the request receivers are locked in an inactive state.

B. Bus Interface Controller

5.11 The BIC functions as a buffer between the 32-bit DDSBS and the 16-bit PIC (Fig. 5). The BIC contains:

- 16-word by 32-bit data FIFO buffer
- 32-bit command register
- 32-bit status flage circuit
- 16-bit sanity and interval timer.

Each of these elements is divided into 16-bit segments for PIC use. The BIC buffers data and commands from the DDSBS to the PIC and data and status information from the PIC to the DDSBS. It also performs "handshaking" protocols with the DDSBS for communication operations.

5.12 The BIC data FIFO buffer can operate in a single 32-bit word mode or in a 16-word block mode. It may be accessed by either the DDSBS or the PIC but not by both at once. Parity checks on transfers between the BIC and the DDSBS are always performed by the BIC; and, if a parity error is detected, an error flag is set. Parity checks on transfers between the BIC and PIC are performed if the state of an internal flag (controlled by the PIC) is not set.

5.13 The 32-bit command register contains command data for the PIC from the CC. When the PIC is signaled that a command is present and the PIC is not busy, the contents of the command register are gated to the PIC. For maintenance purposes, the PIC may write data into this register.

5.14 Sanity and timed interrupts are derived from the 16-bit sanity and interval timer counter. The PIC is provided read/write access to this counter. The counter is incremented every 2.5 or 5 microseconds (depending upon optional wiring). A timed interrupt is triggered whenever the two most

significant bits of the counter are ones (counter is set to 49,152). A sanity error flag is set whenever the counter overflows. To prevent sanity errors, the timed interrupt routine must be entered within 75 milliseconds after it is triggered. The interrupt routine will then restore the counter to its initial value. Interrupt intervals from 0 through 250 milliseconds can be obtained by loading an initial value of 49,152 through 0, respectively, into the counter. The timed interrupt routine will report job completions that have occurred during the last timed interval via an interrupt entry to the IOP driver. Sanity failures set a status bit in the BIC to report detection of an error to the CC.

5.15 Flags within the BIC are used to request interrupt and DMA functions from the CC, to alert the PIC of the presence of a pending CC command or data transfer request, and to record detection of errors. The BIC flags are segmented into 16 bits of status flags (Table C) and 16 bits of error flags (Table D).

BIC Status Flags

5.16 The ***command flag*** reports the status of the BIC command register. The command flag is set upon registration of a command from the CC in the command register and cleared when the command is read by the PIC. The PIC reads the register in two stages: the most significant bits first and then the least significant bits. The command flag is automatically cleared after the PIC reads the 16 least significant bits. When the command flag is set by the CC, a PIC interrupt is generated and the PIC will then retrieve the command and execute it.

5.17 The ***command in progress flag*** is automatically set when a command is received from the CC. After the PIC has executed the command, it clears the command in progress flag to signal the CC that the command was executed.

5.18 The ***data flag*** is used to specify the interface (PIC or DDSBS) that may access the data FIFO buffer. When the data flag is set, the PIC may

TABLE C

BIC STATUS FLAGS

FLAG	FUNCTION
Command	Reports status of BIC command register
Command in progress	Set until command has been executed
Data	Accesses the FIFO buffer
Transfer mode	Determines block or word format
Data buffer FIFO word count	Indicates the number of words stored in FIFO buffer
Interrupt	Requests 3B20D interrupt service
DMA transfer and setup	Requests service from DMA
End of data expected	Indicates the end of DMA block transfer
PIC data bus parity check enable	Enables or inhibits parity checks over PIC data bus
Interface enable	Prevents PIC from communicating with BIC (diagnostics)

TABLE D

BIC ERROR FLAGS

FLAG	FUNCTION
Command register overflow error	Signifies that the PIC has read from or written to the command register without being so instructed
Data register overflow error	Signifies that the PIC has accessed the FIFO buffer when in use by DDSBS
Data bus parity error	Signifies bad parity during PIC read or write
Sanity failure error	Signifies timer overflow
PIC fatal error summary error	Signifies unrecoverable error
End of data error	Signifies end of data flag not set when end-of-transfer signal sent or vice versa
Setup overwrite error	Signifies that the DMA tried to write over data before it is read out
INF parity failure error	Signifies bad parity from DDSBS to BIC

read or write data out of or into the buffer. When cleared, the CC may access the buffer via the DDSBS. The flag toggles between set and clear during data transfers and toggles alternately for the PIC to write data into the buffer and the CC to read it and vice versa. When the buffer is in the 16-word block mode, the flag will be toggled every 16th transfer. When in the 32-bit word mode, the flag is toggled after every data transfer.

5.19 The ***transfer mode flag*** is set when the buffer is in the 16-word block transfer mode and cleared when the buffer is in single-word transfer mode. Both the PIC and the CC (via DDSBS) have access to this flag in order to determine/specify the buffer mode at any time.

5.20 The ***data buffer word count flag*** is a 5-bit flag indicating the number of words stored in the data buffer (from 0 through 16). The count is incremented whenever a word is loaded into the buffer and decremented whenever a word is unloaded.

5.21 The ***interrupt flag*** is set whenever the PIC requests service from the CC. An interrupt mask is included in the DSCH to permit the CC block interrupt requests.

5.22 The ***DMA transfer and setup flag*** is set by the PIC to request DMAC functions. A mask is provided in the DSCH to permit the CC to block DMA requests.

5.23 The ***end of data expected flag*** is set by the PIC at the end of a DMA block transfer. The BIC will verify that the DMAC acknowledges the transfer to be complete. Any errors will result in the generation of an error signal (end-of-data error) and transmission of the error signal to the CC. The successful completion of transfer is indicated by the setting of the end of data received flag by the BIC. The PIC reads the BIC status flag to determine when the operation is completed.

5.24 The ***PIC data bus parity check enable flag*** enables or inhibits parity checks over the

PIC data bus. Correct parity is always forced by the BIC regardless of the state of the flag. When parity check circuits are disabled, the PIC may write information from the arithmetic logic unit (ALU) into the BIC and the BIC will provide the parity bits (parity is not gated through the PIC ALU).

5.25 The ***interface enable flag,*** when cleared by the CC, prevents the PIC from communicating with the BIC. The BIC is disabled for diagnostics by this flag.

BIC Error Flags

5.26 The ***command register overflow error flag*** may be cleared by both the PIC and CC. This flag is set if the PIC reads the command register while the command flag is cleared (register is empty) or attempts to write data into the command register while the command flag is set (the PIC essentially attempts to overwrite a CC command). The write operation is inhibited when the command flag is set.

5.27 The ***data register overflow error flag*** may be cleared by both the PIC and the CC. It is set if the PIC attempts to access the data buffer while the data is in the CC operation state. Also, the flag is set if the PIC attempts to read an empty buffer or if the PIC attempts to write data into a full data buffer. The data buffer is not loaded or unloaded when this error occurs.

5.28 The ***data bus parity error flag*** may be cleared by either the PIC or the CC. The flags are set if the parity check enable flag is set when parity is detected during a PIC read or write operation of the command register or data buffer. Separate flags are provided to record errors over the high and low bytes. Write operations are inhibited when this flag is set.

5.29 The ***sanity failure error flag*** may be cleared only by the CC. It is set if the PIC sanity and interval timer overflows.

5.30 The ***PIC fatal error summary error flag*** may be cleared only by the CC. It is set under program control by the PIC to report an unrecoverable error. Sanity failures also set this flag.

5.31 The ***end of data error flag*** may be cleared only by the CC. It is set if the end of data expected flag is set and the CC requests a read and write data operation (data transfer underrun error) or if the end of data expected flag is not set and the end-of-transfer (EOT) signal is received (data transfer overrun error).

5.32 The ***setup overwrite error flag*** may be cleared only by the CC. It is set if a DMA setup request is pending and the CC performs a write data operation. This will overwrite the setup information stored in the data buffer.

5.33 The ***INF parity failure error flags*** may be cleared only by the CC. These are set if even parity is detected over the INF bus during read and write operations of the data and during write operations of the command register. Individual flags are provided to record failures over each of the four bytes. Parity is neither checked nor generated during CC read status operations.

BIC Commands

5.34 The CC can address commands to the BIC to manipulate these flags. The BIC commands are not loaded in the command register and do not set the command flag. The BIC commands are differentiated from PIC commands by the presence of 00 in bits 1 and 2. Bit 0 is assigned for DSCH and DDSBS maintenance functions. The BIC command layout is shown in Table E.

5.35 The status is interrogated via the sense status (SST) control signal in the PBI in the DDSBS. The BIC does not maintain parity over its status word. The BIC word layout is shown in Table F.

5.36 The PIC reads and writes various data within the BIC over its data bus. The PIC specifies a 5-bit code source (SCR) defining the register data to be gated onto the bus and a 5-bit code destination (DST) defining the register to be loaded from the bus. The PIC can interrogate the state of the BIC status and error flags via codes 8 and 9 (decimal), respectively. The SCR codes define transmitting circuit, and DST defines receiving circuit. Layouts of the bit fields are shown in Table G.

5.37 The PIC manipulates various BIC flags via DST code 8 as shown in Table H.

5.38 The PIC reads and writes the various entities within the BIC via SCR and DST codes 8 through 15. See Table I.

TABLE E

BIC COMMAND LAYOUT

INF BIT	FUNCTION
3	Sets DMA XFER request
4	Sets DMA setup request
5	Sets end of data expected
6	Clears command in progress
7	Sets interrupt
8	Resets interrupt
9	Sets word transfer mode
10	Sets block transfer mode
11	Sets interface enable
12	Clears data FIFO buffer
13	Clears BIC
14	Resets PIC
15-31	Spare

C. Peripheral Interface Controller

5.39 The PIC (Fig. 6) consists of a controller (TN61) and up to 65K words of microcontrol store (MCS); however, the MCS in the IOP PIC is an 8K-word MCS. The MCS circuit pack (TN84) contains an 8K by 40-bit program store and the PIC clock circuit. Also, the MCS circuit pack contains a parity check circuit. The PIC controller contains a 16-bit register and arithmetic logic unit (RALU) and a 16-bit microprogram sequencer.

5.40 The four output conditions of the RALU (carry, overflow, sign and zero), accompanied by the four external conditions, are gated into a condition test multiplexor. The multiplexor is used during conditional branch instructions. The four external test inputs are specified by the application system. The IOP assignments are as follows:

Test 0	Connected to BIC data flag (DFLG) and used to determine when BIC data buffer is available
Test 1	Spare
Test 2	Connected BIC error summary
Test 3	IOMI data register parity error.

5.41 A 4K by 18-bit (16 data and 2 parity) random access memory (RAM) is contained on the controller and used for data storage. Associated with the RAM is a 12-bit RAM address sequencer, which serves as a 4-level stack for storage of interim addresses as well as a circuit that provides automatic incrementing of addresses.

5.42 Eight vectored priority interrupt levels are designed into the PIC circuit. A 7-bit mask register is included to individually block selected levels. Level 0 is reserved for a reset function and is unmaskable. Level 1 is assigned to parity failures over the microdata word, and level 2 is assigned to the instruction timer. The IOP interrupt assignments are as follows:

Level 0	Spare and left unconnected.
Level 1	MCS parity errors.
Level 2	Instruction timer.
Level 3	Connected to the command flag (CFLG) in the BIC. (This interrupt is used to alert PIC of the presence of a command from the CC awaiting execution in BIC.)
Level 4	Spare and left unconnected.
Level 5	Connected to the PC interrupt request summary formed in the IOMI.
Level 6	Spare and left unconnected.
Level 7	Derived from the interval timer on BIC.

TABLE F

BIC STATUS WORD LAYOUT

INF BIT	DEFINITION
0-3	Device address
4	DMA setup overwrite error
5	INF parity failure over byte 0 (most significant)
6	INF parity failure over byte 1
7	INF parity failure over byte 2
8	INF parity failure over byte 3 (least significant)
9	End-of-data error
10	PIC fatal error summary
11	PIC sanity error
12	PIC data bus parity error (low byte)
13	PIC data bus parity error (high byte)
14	PIC data FIFO overflow
15	PIC command register overflow
16-20	Data FIFO word count
21	Interrupt
22	DMA XFER request
23	DMA setup request
24	End of data expected
25	End of data received
26	Data transfer mode (0—word, 1—block)
27	Enable PIC data bus parity checks
28	PIC interface enabled
29	Data flag
30	Command in progress
31	Command flag

TABLE G

BIC BIT FIELD LAYOUTS

FLAG	DB BIT	DEFINITION
BIC status flag (source 8)	0-4	Data buffer word count
	5	Interrupt request
	6	DMA XFER request
	7	DMA setup request
	8	End of data expected
	9	End of data received
	10	Data transfer mode (0–word, 1–block)
	11	Enable PIC data bus parity checks
	12	PIC interface enabled
	13	Data flag
	14	Command in progress
	15	Command flag
BIC error flag (source 9)	0-1	Unused (0)
	2	PIC data bus parity error (low byte)
	3	PIC data bus parity error (high byte)
	4	PIC data buffer overflow
	5	PIC command register overflow
	6	PIC sanity error
	7	INF parity error (byte 0)
	8	INF parity error (byte 1)
	9	INF parity error (byte 2)
	10	INF parity error (byte 3)
	11	3B DMA setup overwrite
	12	End-of-data error
	13	PIC soft error summary
	14	PIC fatal error summary
	15	3B Error summary

TABLE H

PIC WRITE FLAG OPERATION (DESTINATION 8)

DB BIT	FUNCTION
0	Sets DMA XFER request
1	Sets DMA setup request
2	Sets interrupt
3	Clears end-of-data expected and end-of-data received
5-6	Set word/block transfer mode
7	Sets/resets data bus parity check enable
8	Sets PIC fatal error flag
9	Clears PIC soft errors
10	Clears data FIFO buffer
11	Toggles data flag
12-13	Set-reset command in progress

TABLE I

PIC-TO-BIC ENTITIES

SOURCE	DESTINATION	ENTITY
8	8	BIC status flags
9	—	BIC error flags
10	10	Command high
11	11	Command low
12	12	Data high
13	13	Data low
14	14	Data low (sets XFER)
15	15	Timer

5.43 Sixteen interrupt vectors are stored at locations 3F0 through 3FF. The layout of this interrupt jump table is shown in Table J. Bit 7 of the interrupt mask is used to specify whether the normal or maintenance routine should be entered. This feature, along with the capability to write the interrupt register, is used by the PIC to verify proper operation of the interrupt circuitry.

5.44 A 32-bit microdata register resides in the controller. The output of this register controls the various entities within the PIC. To select the instruction operands, 5-bit SCR and DST fields are used. The first eight SCR and DST codes are defined by the PIC. The PIC SCR and DST codes are listed in Table K.

5.45 An overlay field in the PIC instruction word is used to specify parameters of the instruction. A 2-bit field in the microinstruction specifies whether a branch or arithmetic/logic operation is to be performed (ie, how the overlay field contents are to be interrupted). Arithmetic/logic instructions use the overlay field to specify the operation type. A 9-bit instruction is gated into the RALU to specify an operation [function (FCN) field] and its operands (SCR and DST fields). The carry-over into the RALU is specified by another bit. Internal to the RALU are 16 general registers and a single special register (Q). Instructions specifying pairs of general registers as operands use the A- and B-address fields. The RALU uses a 2-address architecture; ie, the A-address operates on the B-address, and the result is placed in the B-address field.

5.46 Branch instructions can be of two basic types: conditional and unconditional. Unconditional jumps and subroutine calls to an immediate 15-bit address are included as branch functions F and E, respectively. Conditional jumps, subroutine calls and returns, and file movements use a 3-bit condition field and a 12-bit immediate address. The 3-bit condition field controls the test conditions. Both branch-if-true and branch-if-false instructions are provided.

5.47 The overlay field may be used for transferring immediate data to a destination register external to the RALU. Immediate data operations do not permit RALU operations since the fields overlap. To move immediate data into an RALU register, it must first be moved to an external register and then into the RALU. A special scratch register has been provided in the PIC for this purpose.

TABLE J

INTERRUPT JUMP TABLE

LOCATION	MICRODATA WORD FUNCTION
3F0	Jump to normal interrupt subroutine for interrupt 0
3F1	Jump to normal interrupt subroutine for interrupt 1
3F2	Jump to normal interrupt subroutine for interrupt 2
3F3	Jump to normal interrupt subroutine for interrupt 3
3F4	Jump to normal interrupt subroutine for interrupt 4
3F5	Jump to normal interrupt subroutine for interrupt 5
3F6	Jump to normal interrupt subroutine for interrupt 6
3F7	Jump to normal interrupt subroutine for interrupt 7
3F8	Jump to maintenance interrupt subroutine for interrupt 0
3F9	Jump to maintenance interrupt subroutine for interrupt 1
3FA	Jump to maintenance interrupt subroutine for interrupt 2
3FB	Jump to maintenance interrupt subroutine for interrupt 3
3FC	Jump to maintenance interrupt subroutine for interrupt 4
3FD	Jump to maintenance interrupt subroutine for interrupt 5
3FE	Jump to maintenance interrupt subroutine for interrupt 6
3FF	Jump to maintenance interrupt subroutine for interrupt 7

5.48 A 2-bit field in the microinstruction is used to specify whether interrupts are enabled or inhibited. When inhibited requests on interrupt lines 1 through 7 are not honored, interrupt level 0 (RESET) cannot be blocked and, when active, will always initiate an interrupt. Each microinstruction contains a 4-bit field that specifies the instruction execution time.

5.49 Instruction speeds may vary from 100 through 300 ns in increments of 50 ns. The instruction timing circuitry resides on the MCS. Because of the usage of 8-bit-wide program read-only memories (PROMS), the MCS parity bit is byte-sliced (8-bit partitioned). Parity is maintained across bit 0 of each PROM, across bit 1 of each PROM, etc. The detection of a parity failure will trigger an interrupt.

5.50 A 16-bit scratch pad overlay function has been provided. When selected as the operation destination, the data bus contents selected by source field replace the overlay field of the microinstruction. This provides a mechanism for implementing table-driven sequences of operations used for diagnostics.

TABLE K

PIC SOURCE AND DESTINATION CODES

SRC CODE	DST CODE	SOURCE AND/OR DESTINATION REGISTER	CIRCUIT CONTAINING SOURCE AND/OR DESTINATION REGISTER
0	0	RAM address	PIC CONT
1	1	Instruction counter	PIC CONT
2	2	Interrupt	PIC CONT
3	—	Immediate data	PIC CONT
—	3	Sequencer macro register	PIC CONT
4	4	Scratch register	PIC CONT
5	5	RAM	PIC CONT
—	6	Scratch pad overlay	PIC CONT
7	—	ALU	PIC CONT
8	8	BIC status flag	BIC
9	—	BIC error flag	BIC
10	10	Command high	BIC
11	11	Command low	BIC
12	12	Data high	BIC
13	13	Data low	BIC
14	14	Data low (also sets XFER)	BIC
15	15	Sanity and interval timer	BIC
16	—	Control signal acknowledge	IOMI
17	—	Service request register	IOMI
18	—	Interrupt register	IOMI
19	—	IOMI error register	IOMI
20	20	IOMI data register	IOMI
21	21	PC memory address register	IOMI
22	22	Control register	IOMI

TABLE K (Contd)

PIC SOURCE AND DESTINATION CODES

SRC CODE	DST CODE	SOURCE AND/OR DESTINATION REGISTER	CIRCUIT CONTAINING SOURCE AND/OR DESTINATION REGISTER
23	23	PC address register	IOMI
24	23	PC community out of service	IOMI
—	25	Clear error	IOMI
23	26	Maintenance	IOMI
—	27	Performance monitoring command	IOMI
—	28	Performance monitoring first data register	IOMI
—	29	Performance monitoring second data register	IOMI
—	31	Enable UN25	IOMI

D. Input-Output Microprocessor Interface

5.51 The IOMI (Fig. 7) functions as the interface between the 16-bit PIC and the 8-bit PCs. It consists of a 16-bit memory address, a 9-bit (eight data and one parity) bidirectional data bus, and eight control signals. Also, a private PC select signal is connected to each of the 16 PCs. The selected PC acknowledges reception of a control signal by setting the control signal acknowledge (CSA) signal. The 16 CSA bits are compared to the 16 PC select signals to indicate to the PIC when the acknowledgment has been received.

5.52 Each PC has three request leads that are used to indicate errors or to request service. Each PC is assigned a bit in each of the three 16-bit request registers. A low level on the error signal will set the PC error flag. The trailing edge of the active low interrupt and service request signals will set the designated bit in the interrupt and service request registers, respectively. A summary bit, provided over the interrupt register contents, triggers a PIC interrupt whenever any bits are set. The PIC reads the data and clears the interrupt and service request registers via destinations 17 and 18. Special circuitry is provided to ensure that requests will not be lost nor sensed twice by the PIC. The PIC can read the contents of the error register using destination 19 and can clear the register via destination 25. A read-and-clear operation consists of two sequential operations 200 nanoseconds apart.

5.53 The four fanout branches of the data, address, and control signal (one per PC community) are driven from three common registers. The 16-bit memory address register is implemented using binary up/down counters to provide auto-increment and auto-decrement capability. The mode of operation is specified by bits 8 and 9 of the control signal register. Special circuitry is provided to ensure 200 nanoseconds of address setup and hold times around the trailing edge of the active low memory read and write control signals. The PC memory access and cycle times are approximately 400 and 600 nanoseconds, resptectively.

5.54 The 18-bit (16 data and 2 parity) data register is divided into high and low bytes to be transmitted a byte at a time to and from the 9-bit (eight data and one parity) PC data buses. A flag in the control register selects the high or low bytes as the SCR or DST of the data transfer between the IOMI and the selected PC. An additional bit in the control signal register is used to toggle the data byte selector flag after a memory read or write cycle. A delay tim-

ing chain circuit is provided to ensure 50 nanoseconds of data hold time during memory write operations.

5.55 The control signal register is segmented into two fields: an 8-bit register (the outputs of which directly drive the control signal buses) and an 8-bit field (which controls the internal functions in the IOMI). The control signal register bits and corresponding functions are listed in Table L.

5.56 An out-of service bit is provided for each of four PC communities. This 4-bit register can be read and written by the PC. Additionally, a power-down condition within a PC community will automatically set its out-of-service flag. When out of service, the interrupt requests of the four PCs within that community are not ORed into the interrupt register summary.

5.57 The IOMI SCR and DST codes are listed in Table M.

E. Peripheral Controller

5.58 The PC is a microcomputer that functions as the interface between the PIC and slow-to-medium speed PDs (Fig. 8). The PIC can directly address the four PCSDs of the PC community. The PCSD also indicates to the PIC (via the PC using service request signals) jobs to be performed. The PIC reads the PC service request status information to determine the type of job to be performed.

5.59 A PCSD activates a service request in order to transfer data to or from the MAS or to indicate that a job has been completed. The PCSD may initiate an interrupt request that results in a PIC in-

TABLE L

CONTROL SIGNAL REGISTER BITS

BIT	DEFINITION
0	CLR0 — Clears PC
1	RISL80 — Sets PC isolate flip-flop
3	CINT0 — Command interrupt (PIC->PC)
4	DMAWR0 — DMA memory write
5	DMARD0 — DMA memory read
6	DMAOC0 — DMA operation complete
7	DMARQ0 — DMA request
8-9	Memory address register mode: 00 — Autoincrement 01 — Autodecrement 1X — Holds present contents
12	DRVDAT0 — Enables data to be gated on PC community buses
13	Forces high data byte to be selected
14	Forces low data byte to be selected
15	Toggles data byte selector

TABLE M

IOMI SOURCE AND DESTINATION CODES

SRC CODE	DST CODE	SOURCE AND/OR DESTINATION REGISTER
16	—	Control signal acknowledge
17	—	Service request register
18	—	Interrupt register
19	—	Error register
20	20	Data register
21	21	Memory address register
22	22	Control register
23	23	PC address register
24	23	PC community out-of-service flag
—	25	Clears error register
23	26	Maintenance register

terrupt request status information read operation. The interrupt request is activated by a PCSD to transfer high-priority information to or from the MAS or to indicate completion of a high-priority job.

5.60 All communication between the PIC and the PC is accomplished via a dual access memory circuit in the PC. Dedicated memory locations are reserved within the dual access memory which contains pointers used by the PIC to locate PCSD data buffers, data transfer parameters, and status and command areas. In addition, the dual access memory has memory locations that contain PC data. An asynchronous response register is provided for each PCSD. The PC data consists of service and interrupt request data and PC command area pointers.

5.61 The PIC gates commands to the PC to set up data transfer jobs and to administer error detection and fault recovery action. There is a command area located in the dual access memory for the PC and each PCSD. The PC interprets the commands and initiates appropriate action as required.

5.62 The PC consists of the following circuits:

- Microprocessor (MP)
- Read-only memory (ROM)
- Random access memory (RAM)
- Isolation circuitry
- Hardware error detection
- Clock check circuit
- Routine maintenance diagnostics (RMD)
- Sanity check
- Scan back circuitry
- Service and interrupt request generation
- Status register.

5.63 ***Microprocessor (MP):*** The PC uses an MP to administer the transfer of data between its

PDs (via PCSD) and MAS. The MP receives inputs from the PD and the PIC with the PIC inputs assigned control priority.

5.64 ***Read-Only Memory (ROM):*** The PC contains a bootstrap program, stored in the ROM, which is entered when power is initially applied or when the PC reset function is activated by the PIC. The bootstrap program, when used, causes the MP to initialize the PDs (via PCSDs) and to scan for PIC commands. In addition to the bootstrap program, the ROM may contain operational and diagnostic programs (determined by application system).

5.65 ***Random Access Memory (RAM):*** The PC uses RAM to store operational program, buffer transient data, and PIC communication parameters. The portion of the RAM containing data buffers and communication parameters is accessed by both the PIC and PC MP. Some PCs have separate program store and data store. In such cases, the PIC has direct access only to the data store.

5.66 ***Isolation Circuitry:*** The isolation circuitry provides the capability of removing all response signals generated by the PC from the communication bus connected to the PIC. Isolation is provided by removing +5 volt power from the device(s) generating the response signals. An isolation control logic (ICL) circuit on the PC accomplishes this isolation. Upon receiving a set of isolation flip-flop (FF) or clear signals from the PIC, the isolation control logic circuit removes the +5 volt power from the designated device(s). The PC isolation state remains in effect until a reset isolation FF signal is sent from the PIC. This circuit is used to inhibit MPs from overloading the communication bus with invalid data if a fault condition develops.

5.67 ***Hardware Error Detection:*** The PC provides parity checking and generating for data contained in RAM. Since most microprocessors and microprocessor peripherals available today do not carry parity within the device, routine diagnostics must take over the responsibility of error detection for these devices. Parity over ROM data is not a requirement. This enables PC designs to take advantage of the circuit board ROM program storage. However, a program sanity error FF is used to store the indication of an RAM parity failure. If a separate dual access memory RAM system is used, a separate parity checker/generator and parity error FF indicator are provided for this memory system. The PC also provides this memory control logic with the ability to invert parity generation in order to check the parity circuits.

5.68 ***Clock Check Circuit:*** The PCs operate autonomously with respect to PIC activity and therefore provide their own system clock. A system clock check citcuit is provided by the PC to detect clock activity abnormalities. A clock error FF is used to store the clock failure indication. The error lead is employed to report the detection of such failures.

5.69 ***Routine Maintenance Diagnostics (RMD):*** The PC uses RMD to increase error detection capabilities. Redundant software (instead of redundant hardware circuits) is used to detect fault conditions. The PC MP periodically (dependent upon application system) executes routine maintenance diagnostics during nonpeak data transmission time intervals. An RMD FF is provided to store the RMD failure indications.

5.70 ***Sanity Check:*** To ensure program execution, the PC provides a sanity check circuit. This circuit is used to detect MP failure and to prevent an MP failure from resulting in a fatal IOP operation. A sanity failure FF is used to store the sanity failure indication.

5.71 ***Scan Back Circuitry:*** The PC provides four directly addressable read-only bytes of information for the scan back circuitry. These are as follows:

BYTE	CONTENTS
0	Status and error information
1	Address lower loop-around data
2	Address upper loop-around data
3	PC-type identity code.

5.72 The PIC retrieves the information located at the associated address by activating the corresponding PC select lead, sending the correct DMA address code, and activating the DMARDO signal. Only the two least significant address bits are used to select one of the scan back bytes. The remaining address bits are not used and can be in any state. The scan back data is returned to the PIC via the common data bus. The scan back circuitry is disabled during

a PIC access of the PC dual access memory to prevent interaction with the dual access memory data that is selected by the DMARQ signal.

5.73 The DMA address leads are connected to scan back locations 1 and 2. The PIC uses the scan back address data in a loop-around mode to check the integrity of the DMA address and data buses and to verify that the designated PC is receiving the complete address information. The PC-type identity code is located at scan back address 3 and is used by fault recovery and administration programs to determine and verify the PC type.

5.74 ***Service and Interrupt Request Generation:*** The PC generates a service request (SR) and/or interrupt request (IR) whenever a data transfer to or from the MAS is required or to indicate that a command completion response is available. The PC provides a separate pulse source for the IR and SR indications. The PIC IOMI circuit pack uses the trailing edge of the active low SR or IR to set the associated job-pending indicator flip-flop. The PC should not gate a new SR or IR until the previously sent request has been detected by the PIC. The PIC indicates recognition of an SR or IR by clearing the associated request-pending flag in the PC dual access memory.

5.75 ***Status Register:*** Each PCSD within the PC is assigned four bytes of the dual access memory which contain status information for the assigned PCSD. The status information is comprised of generic and user-defined data.

6. POWER

A. Introduction

6.01 The IOP power circuits (Fig. 9) require 15 amperes at −48 Vdc which is supplied by the power distributing frame from the −48V office source. See Section 254-302-020 for system power requirements. The voltages provided by the IOP power circuits are partitioned into the PIC circuit and each PC community. These voltages are:

- −48V for PC community (TTY current loop)
- +12V and −12V for each PC community [Electronic Industry Association (EIA) RS232C line drivers and receivers]
- +12V and −5V for each PC community (TN9 for the memory devices)
- +5V for each PC community and PIC circuit (TTL)
- +12V for reference circuits on the TN9 circuit pack.

6.02 When power is applied, the power control switch first enables the 495FA dc-to-dc converter start leads to produce +5V. In the PIC, this lead is interlocked by the BIC; and, in each PC community, it is interlocked by converter/monitor circuit TN9. (If any of these circuit packs are not equipped, power cannot be supplied.) Approximately 600 milliseconds later, the start B-sequence occurs which starts the memory power converters (TN9). The TN9 circuitry will internally sequence memory power so that −5V is on before the +12V.

6.03 Approximately 1 second after the beginning of the voltage sequence, the power clear (INIT) and bus power enable (BPEN) signals become active. The input voltage to the power control switch is sensed to verify that the sequence has been completed prior to activation of these signals.

6.04 When power is removed, the reverse sequence occurs. Power clear (INIT) and bus power enable (BPEN) signals become inactive. Then the +12V (memory) and −5V (memory) powers, which are self-sequenced by the TN9 circuitry, are removed. Finally, the +5V logic power is removed before the OFF lamp on the power control switch is lighted.

6.05 Power is segmented in the IOP so that any PC community may be individually powered down without affecting the remaining active portions of the IOP. There are interlocking switches on the 495FA dc-to-dc converter and the TN9 power monitor/converter so that these may not be removed from the frame without first removing power from the PC community. Removal of the TN9 circuit pack also removes −48V from that community. Also, if the PIC is powered down, the entire IOP will be automatically powered down.

6.06 In the event of a failure in any PC community, the power alert lamp is lighted on the power control switch. This closes a set of contacts that can

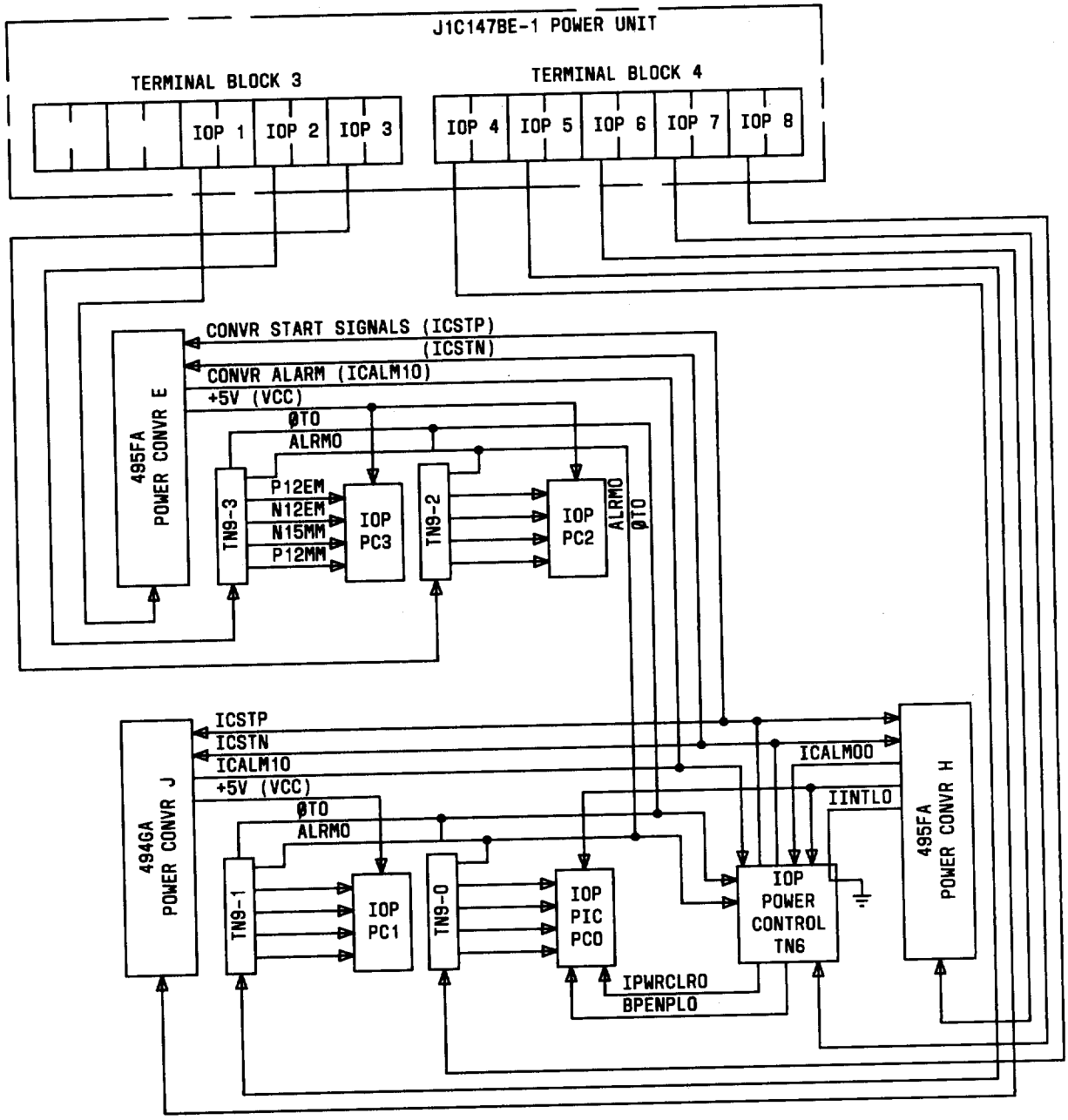


Fig. 9—Input-Output Processor Power Functional Block Diagram

be user-connected to the office minor alarm circuit. If a failure causes the loss of all +5V power from a PC community, memory power is sequenced down by the converter/monitor TN9 circuit. That PC community will be marked out of service to the IOMI. If any fuse fails in the PIC circuit, the entire IOP unit is powered down by the power control switch. This closes a set of contacts that can be connected to the office major alarm circuit.

6.07 Due to the volatile nature of the memory in each PC community, each voltage in the PC community is monitored as follows:

(a) The EIA voltages supplied by the TN9 converter/monitor must be no greater than 18V. The converter/monitor TN9 circuit checks to verify that voltage is greater than ±4.5V (backplane).

(b) Memory voltages are generated and checked on the converter/monitor TN9 to verify that the voltages are within 10 percent of nominal value.

(c) Logic voltages supplied by the 494FA converter are compared to a reference voltage on the TN9. Any deviation from the reference voltage is amplified and transmitted to the 495FA converter remote sense leads. (The logic voltages generated by the 495FA converter are checked to verify that the voltages are within 10 percent of nominal value).

In the event that any of these conditions are not met, the power alert lamp on the power control switch is lighted. Also, the PC community is marked out of service by the IOMI.

6.08 Two light-emitting diodes (LEDs) are mounted on the front of the converter/monitor (TN9) circuit pack. These indicate:

(a) If any one of the TN9 internal voltages [+5V (TTL), +12V or −12V (EIA), −5V or +12V (memory)] is out of tolerance (OOT) (red LED)

(b) PC unit marked out of service (OOS) by the IOMI (yellow LED).

B. Power Control Switches

6.09 The power control switch (TN6) (Fig. 10) provides the control (application and removal) for the IOP power. Three-phased start signals are provided by the IOP PC to control the application sequence of logic power and input-output bus power. The craft may perform the following functions:

- Sequentially apply or remove power.
- Initiate system request to remove from service or restore to service the associated unit.
- Test indicator lights on the power switch.
- Retire a major office alarm generated at the associated unit.

6.10 Five switches provide power control. These are located on the front power panel of the TN6 and are ON, OFF, ROS/RST (request out of service/restore), ACO/T (alarm cutoff/test lamps), and

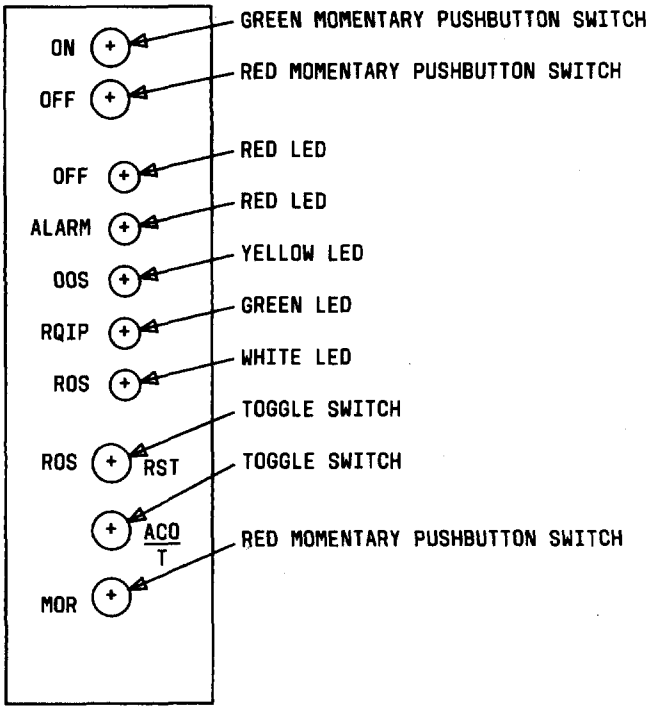


Fig. 10 — Input-Output Processor Power Control Panel

MOR (manual override). The ON, OFF, and MOR switches are momentary pushbutton switches, and the ROS/RST and ACO/T switches are 2-position latching switches. Input voltage requirements are −48 volts from the office supply and +5 volts from the BELLPAC power converters controlled by the TN6.

6.11 The power control switches are described below:

(a) ***ON Switch:*** Momentarily depressing the ON switch when the ACO/T switch is not in the alarm cutoff state initiates the power-up sequence. Depressing the ON switch when the ACO/T switch is in the alarm cutoff state or when frame power is up causes no change in the state of the TN6.

(b) ***OFF Switch:*** Momentarily depressing the OFF switch when the unit is in the out-of-service state initiates the power-down sequence. Depressing the OFF switch when the unit is in service or when power is off causes no change in the state of the TN6.

(c) ***ROS/RST Switch:*** Depressing the ROS/RST switch to the ROS position requests that the unit be taken out of service via scan point SCX and lights the ROS LED. Depressing the ROS/RST switch to the RST position requests that the unit be restored to service.

(d) ***ACO/T Switch:*** Depressing the ACO/T switch to the alarm cutoff state tests all lamps on the TN6, silences the office major alarm, and permits the ALM LED to extinguish (when the ACO/T switch is returned to its normal position).

(e) ***MOR Switch:*** Simultaneously depressing the OFF and MOR switches defeats the interlock between the off switch and unit out-of-service state and initiates the power-down sequence.

C. Power Control Indicators

6.12 Five indicator lights on the front panel of the TN6 indicate the state of the unit being controlled. These lights are OFF, ALM (alarm), OOS (out of service), RQIP (request in progress), and ROS (request out of service). The five indicators are 549-type LEDs. The indicators are described below:

(a) ***OFF LED:*** A red LED labeled OFF is lighted when the unit is in the power-off state and extinguished when the unit is in the power-on state.

(b) ***ALM LED:*** A red LED labeled ALM is lighted to indicate the presence of power-related faults.

(c) ***OOS LED:*** A yellow LED labeled OOS is system-activated via the OOS signal distribution point when the unit is marked out of service.

(d) ***RQIP LED:*** A green LED labeled RQIP is lighted to indicate that the system has received a request to take the unit out of service or restore it to service. This LED, which is system-activated via the RQIP signal distribution point, flashes to indicate that the request has been denied.

(e) ***ROS LED:*** A green LED labeled ROS is lighted when the ROS/RST switch is in the ROS state.

6.13 ***Scan, Alarm, and Signal Distribution Points:*** Two scan points (SCX and SCY), two alarm points (MJ and PA), and two signal distribution points (OOS and RQIP) are provided. Each scan and alarm point consists of an isolated metallic contact. The active "1" state appears as a resistance of less than 200 megohms. The inactive "0" state appears as an open circuit. Each distribution point consists of an opto-isolator input diode.

6.14 ***Scan and Alarm Points:*** The scan and alarm point states are summarized in Table N. On automatic power-off alarms, the MJ alarm contact closes and remains closed until the ACO/T switch is depressed. When power is left up in the presence of a major alarm fault, the MJ alarm point remains closed until either the fault is removed (PA alarm point also goes inactive) or the ACO/T switch is depressed (PA alarm point remains active).

6.15 ***Signal Distribution Points:*** The active "1" state of the RQIP signal distribution point indicates that a system software acknowledgment of a request for removal from service or restoral to service of the associated unit has been made. If the request is granted, the RQIP signal distribution point will become inactive ("0" state). If it is denied, the RQIP SD point will intermittently flash under system control. The OOS signal distribution point becomes active when the unit has been taken out of

TABLE N

SCAN AND ALARM POINT STATES

CONDITION	BPP	SCX	SCY	MJ	PA
Normal in service	1	0	0	0	0
Request out of service	1	1	0	0	0
Manual power off	0	1	1	0	0
Automatic power off	0	1	1	1	0
Power up with major fault present	1/0	0	1	1	1
Power up with minor fault present (such as supply out of tolerance)	1	0	1	0	1

service. The RQIP and OOS LEDs provide a visual indication of the state of the RQIP and OOS signal distribution points, respectively. The signal distribution point states are summarized in Table O.

D. Power-Up Sequence

6.16 Power-up is initiated by momentarily depressing the power ON switch. Control circuitry ensures that power is supplied in the proper sequence via three start signals and an initialization phase. In the power-off state, the initialization circuit that starts the power-up sequence is powered from a fused −48V source through a normally open ON switch (momentary contact). Initialization signals enable +5V frame converters that power TTL sequence circuitry and initialize power control and alarm circuitry. The power-off LED is lighted in the power-off state and is not extinguished until the power-up sequence is complete.

TABLE O

SIGNAL DISTRIBUTION POINT STATES

CONDITION	RQIP	OOS
Normal in service	0	0
Remove-from-service or restore to-service request with disposition pending	1	0
Request denied	Flash	0
Diagnostic failure after a restore-to-service request	Flash	0
System-granted out-of-service request	0	1

E. Power-Down Sequence

Normal Power Down

6.17 To prevent inadvertent removal of frame power, the OFF switch (momentary contact) is interlocked with a system-granted OOS signal. Depressing the power OFF switch causes no change in state of the circuit pack unless the OOS signal distribution point is active, in which case frame power is sequentially removed. The power-off LED remains extinguished until the power-down sequence is complete.

Emergency Power Down

6.18 Craft personnel have the option of overriding the power OFF switch OOS interlock under emergency conditions. Simultaneously depressing the power OFF and MOR (manual override) switches sequentially removes frame power, providing an emergency manual power control if needed. See Section 254-302-020 for additional details concerning the power systems for the 3B20D Model 2 processor.

7. MAINTENANCE

7.01 Each CC is equipped with dedicated peripheral units; however, the IOP may be accessed by either CC. If a fault is detected in the IOP, recovery action is initiated; if the recovery action fails to correct the fault, the IOP is placed out of service. When the IOP is placed out of service, the appropriate alarm is given accompanied by a TTY printout. If the fault is detected in the CC, MAS, or DMA units, a switch to the duplicated CC and its dedicated periphery is made.

7.02 A fault in a PD connected to the IOP will result in the PD being placed out of service. The functions provided by the PD will be lost by the system until the PD is repaired or replaced.

7.03 The maintenance provided is mainly software; the IOP uses loop-around messages to check its circuits. These loop-around messages are used when the IOP is placed in the maintenance state (start code) by the CC to detect circuit faults. The IOP also implements status messages to signal the CC of faults detected during normal operations.

7.04 The IOP also uses internal software to detect internal faults (ie, the dual access memory in the PIC) and to initiate fault recovery. Also, hardware checks are provided in the IOP for fault detection such as start code, parity, error detection logic, and power error circuits. Additionally, the IOP is provided with clock checks for timing, sanity check circuit, and routine maintenance diagnostics.

7.05 The IOP is partitioned so that, if a PC community is out of service, the other equipped community can function normally. This is accomplished via appropriate software commands.

7.06 Power failure(s) and/or cooling unit failure(s) will automatically initiate the power-down sequence.

8. REFERENCE

8.01 Refer to Section 254-302-000 for a description of documentation relevant to this section.

9. GLOSSARY

9.01 A glossary of terms is provided to aid in the understanding of this section:

Asynchronous—Functional units operate or interface without a fixed time relationship.

Autonomous—The device can perform its primary function without external assistance.

Buffer—A storage device used to compensate for a difference in the rate of flow of information or time of occurrence of events when transmitting from one device to another. Normally a register.

Bus—One or more conductors over which information is transmitted from any of several sources to any of several destinations.

Diagnostic—A program which functions to isolate a fault within the unit under test.

Flag—An indication signal used to signify a fault condition and/or operation status.

Flip-Flop—A device capable of assuming two stable states (set or clear), thereby storing a bit of information. It remains in either state until a signal changes it to another state.

Gate—A circuit which has ability to produce an output dependent upon specified type or the coincident nature of the input(s).

Interrupt—A signal generated by a device to notify the CC that the device requires attention.

10. ABBREVIATIONS

10.01 The following is a list of abbreviations used in this section.

ACO/T—Alarm Cutoff/Test

ALM—Alarm

ALU—Arithmetic Logic Unit

BIC—Bus Interface Controller

CC—Central Control

CCIO—Central Control Input-Output

CONT—Controller

DDSBS—Duplex Dual Serial Bus Selector

DFLG—Data Flag

DMA—Direct Memory Access

DMAC—Direct Memory Access Controller

DMA IO—Direct Memory Access Input-Output

DP—Data Report

DR—Data Request

DSCH—Dual Serial Channel

DST—Destination

EIA—Electronic Industry Association

EOT—End of Transfer

ER—Error

FCN—Function

FIFO—First-in-First-Out

FF—Flip-Flop

ICL—Isolation Control Logic

INTP—Interrupt

IO—Input-Output

IOMI—Input-Output Microprocessor Interface

IOP—Input-Output Processor

IR—Interrupt Request

LC—Line Community

LED—LIght-Emitting Diode

MAS—Main Store

MCS—Microcontrol Store

MDS—Microprocessor Development System

MOR—Manual Override

MP—Microprocessor

OOS—Out Of Service

OOT—Out Of Tolerence

PA—Program Address

PBI—Peripheral Bus Interface

PC—Peripheral Controller

PCSD—Peripheral Controller Subdevice

PD—Peripheral Device

PIC—Peripheral Interface Controller

PROM—Program Read-Only Memory

RALU—Register and Arithmetic Logic Unit

RAM—Random Access Memory

RETS—ROM Emulator and Trace System

ROM—Read-Only Memory

RQS—Request Out Of Service

RQIP—Request In Progress

RST—Restore

SCR—Source

SR—Service Request

SST—Sense Status

SYNC—Synchronization

TTL—Transistor-Transistor Logic

TTY—Teletypewriter