AT&T 3B20D Computer
Small Computer System Interface
Disk File Controller
Description And Theory Of Operation

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1. Overview

1.01 This AT&T Practice provides a physical and functional description and theory of operation for the Small Computer System Interface (SCSI) Disk File Controller (DFC). The SCSI DFC is the logic unit that allows SCSI disk drives to be connected to the 3B20D computer.

1.02 This practice is reissued to update information pertaining to changes in the SCSI. The specific reasons for reissue are listed below:

(a) Reference to 3B20D computer models 2 and 3 deleted so that information in this document pertains to all models of the 3B20D computer.

(b) Modified Figure 4 to reference the new system configuration.

(c) Modified Figure 5 for the growth and conversion configuration.

(d) Modified Figure 6 to show only the interface of the disk file controller.

(e) Modified the wording in Tables F, G, and H to better reflect SCSI functions and descriptions.

(f) Removed Figure 13, SCSI DFC Fuse Connections, because it does not represent all fuse configurations.

1.03 This practice contains no admonishments.

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1.07 Depending on model, the 3B20D computer can have up to four SCSI DFCs. Each SCSI DFC has two SCSI buses. Although the SCSI standard provides for up to eight devices on each SCSI bus, the 3B20D computer will support only magnetic disk drives and only up to four per bus.

1.08 The SCSI DFC (Figure 1) is connected to the computer through a dual serial channel (DSCH). Each SCSI DFC can interface with either of the control units (CUs) within the computer. The SCSI DFC can coexist with the Storage Module Drive Disk File Controller (SMD DFC).

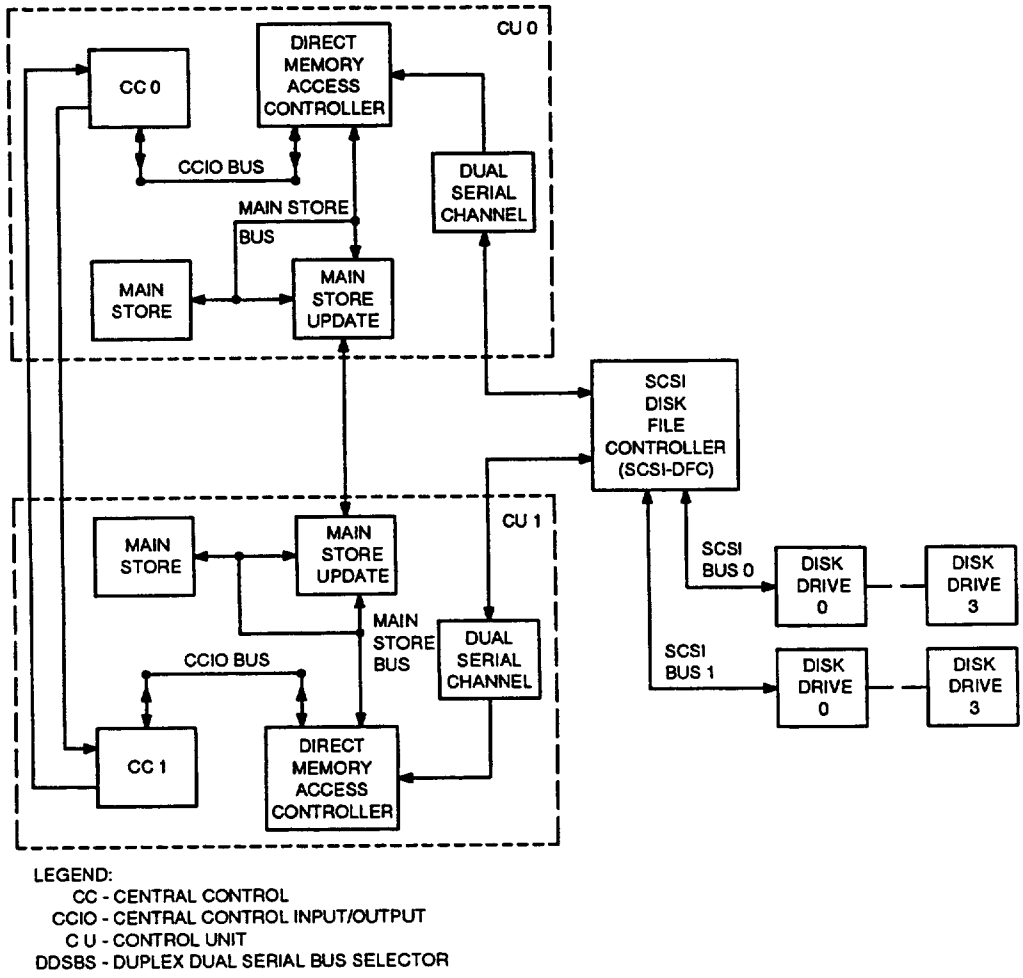


Figure 1. Interface Between CU and SCSI DFC

2. Physical Description

2.01 The SCSI DFC includes the following circuit packs (Figure 2 for a new system configuration or Figure 3 for growth configurations).

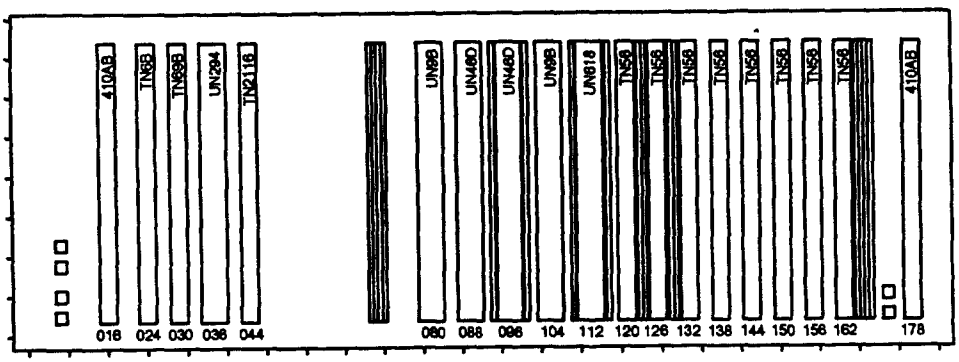


Figure 2. SCSI DFC Circuit Pack Locations (New Systems)

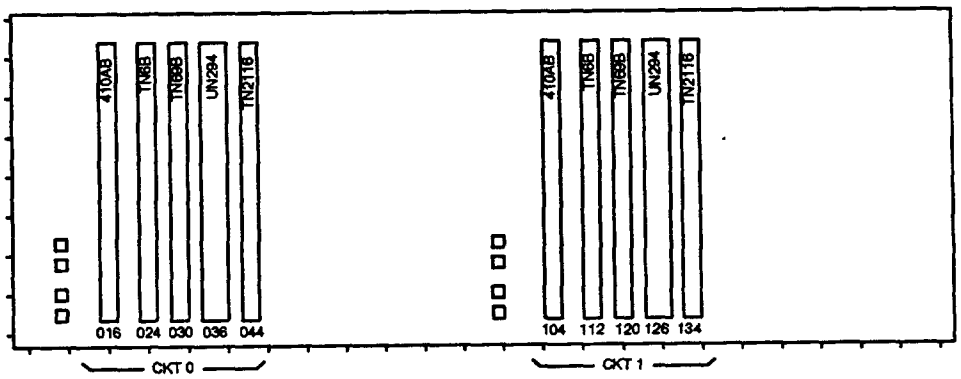


Figure 3. SCSI DFC Circuit Pack Locations (Growth/Conversion)

(a) **Duplex Dual Serial Bus Selector (DDSBS)**: The DDSBS circuit pack (TN69B) interfaces the host adapter (HA) with the dual serial channel (DSCH) of each CU.

(b) **SCSI Host Adapter:** The SCSI HA includes one UN294 and one TN2116 circuit pack. In addition to the two circuit packs, the HA includes two SCSI bus cables connected to the HA backplane. Each SCSI bus cable is a 50-conductor twisted-pair ribbon cable. One end of each SCSI bus cable has a connector that plugs directly into the HA backplane. Each device on the cable connects through a stub. SCSI bus signal termination is provided by resistor networks that plug into each end of the SCSI bus cable.

(c) **Power Control Circuit:** The power control circuit, TN6B, monitors the +5 V and –5 V DC power on the SCSI DFC backplane.

(d) **Power Converter:** The power converter, circuit pack 410AB, converts –48 V DC into +5 V DC to be used by the DDSBS and HA circuit packs.

2.02 A 132B apparatus mounting houses plug-in UN-type and TN-type circuit packs used by the SCSI DFC.

2.03 A multilayer board backplane provides circuit continuity for the signal, control, and power among the plug-in circuit packs. The connector pins are square pins that protrude through the multilayer board backplane. The power input terminals are push-on terminals instead of wire-wrapped pins.

2.04 The basic circuit pack used is equipped with either a 200-pin connector (TN-code series) or a 300-pin connector (UN-code series). The circuit logic is comprised of standard transistor-transistor-logic (TTL) circuits and compatible large scale integration circuits.

2.05 In new system configurations, the SCSI DFC circuit packs are located in the main store-input output (MAS-IO)-DFC unit of the processor control frame cabinet (see Figure 4). In growth and conversion configurations, the SCSI DFC is located in the SCSI Disk Cabinet (Figure 5).

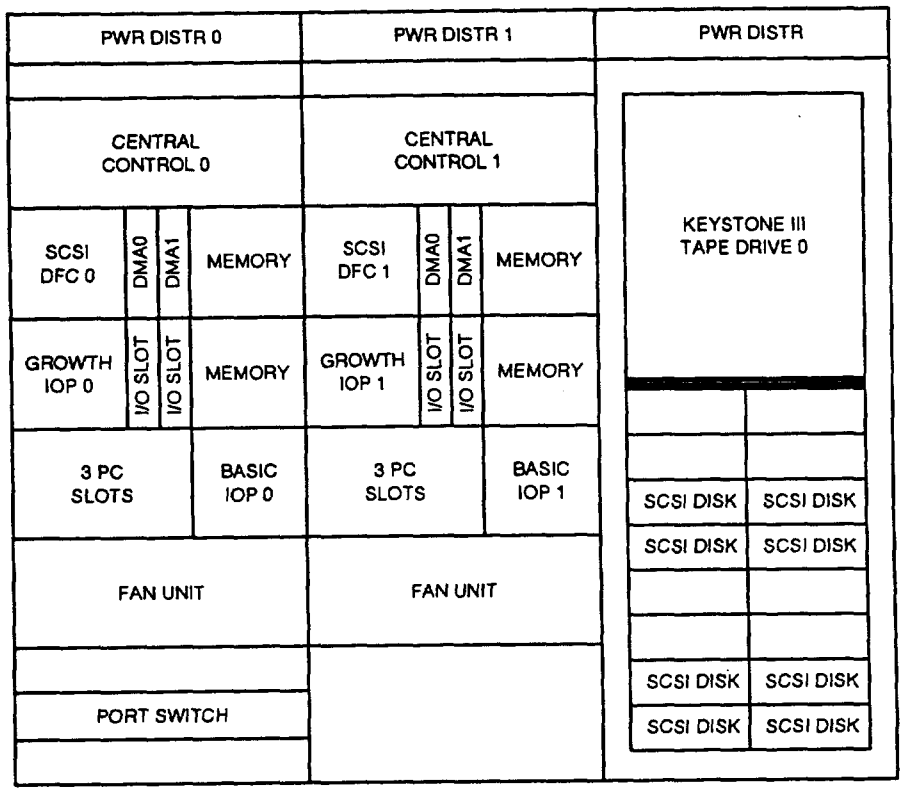


Figure 4. 3B20D Model 3 Computer — Typical New System Configuration Equipped with 5.25 SCSI Disk Drives

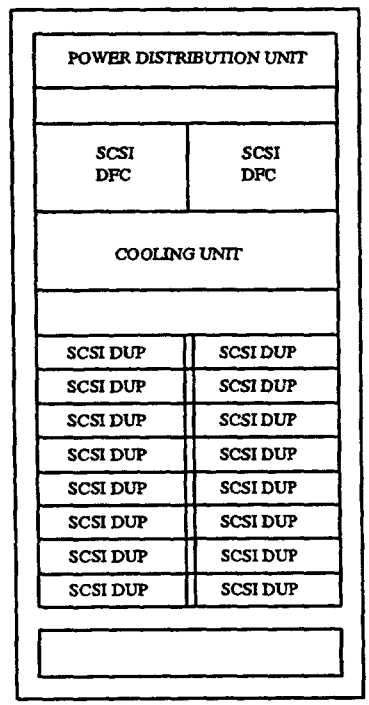


Figure 5. SCSI Disk Cabinet

3. Functional Description

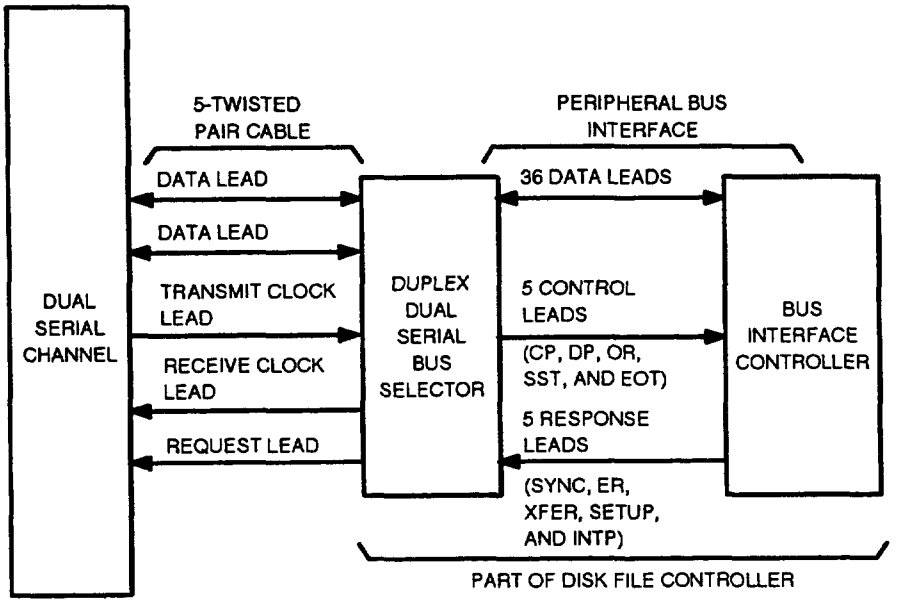
General

3.01 The SCSI DFC interfaces the SCSI disk drives with the CU of the 3B20D computer. The CU issues commands (DFC driver) and data to the SCSI DFC where they are interpreted and executed under microprocessor control. The microprocessor controls the transfer of data between the SCSI disk and memory in the HA. Also controlled by the microprocessor is the transfer of data between the HA memory and the 3B20D computer I/O interfaces.

A. Input/Output Structure

3.02 The SCSI DFC is interfaced to the central control (CC) and main store via the DSCH (Figure 6). The DFC connects to a DSCH in each CC via the DDSBS. The DDSBS communicates with the serial channel (SCH) through two data leads and three control leads.

The DDSBS is part of the SCSI DFC and communicates with the bus interface circuit (BIC) in the HA over the peripheral bus interface (PBI).



LEGEND:

CP	-	COMMAND PRESENT
DP	-	DATA PRESENT
DR	-	DATA REQUEST
EDT	-	END OF TRANSFER
ER	-	ERROR RESPONSE
INTP	-	INTERRUPT REQUEST
I/O	-	INPUT/OUTPUT
SETUP	-	SETUP REQUEST
SST	-	SENSE STATUS
XFER	-	TRANSFER REQUEST

Figure 6. Interface Between Central Control, Main Store, and Disk File Controller

3.03 Data and commands for the SCSI DFC are transmitted by the DSCH to the DDSBS over a 5-twisted-pair cable that is duplicated for each computer (Figure 6). The 5-twisted-pair cable consists of two bidirectional data leads, a transmit clock lead, a receive clock lead, and a request lead. The transmit clock from the DSCH is 20 MHz for cable distances (between the DSCH and DDSBS) of up to 100 feet. Data is transmitted between the DSCH and the DDSBS (32 data plus 4 parity bit words) as two serial (16 data plus 2 parity bit) words. The low order bits (0 through 15 data plus 2 parity) and a 4-digit start code are transmitted over a data low lead; the high order bits (16 through 31 data plus 2 parity) and a 4-digit start code are transmitted over the data high lead. The start code is used to set up the mode of operation or to signal that a command is present.

After information is received by the SCSI DFC, a response code is transmitted to the DSCH to let the computer know how the data or command was received.

B. Internal Disk File Controller

3.04 Internally, the SCSI DFC (Figure 7) consists of the DDSBS and SCSI HA.

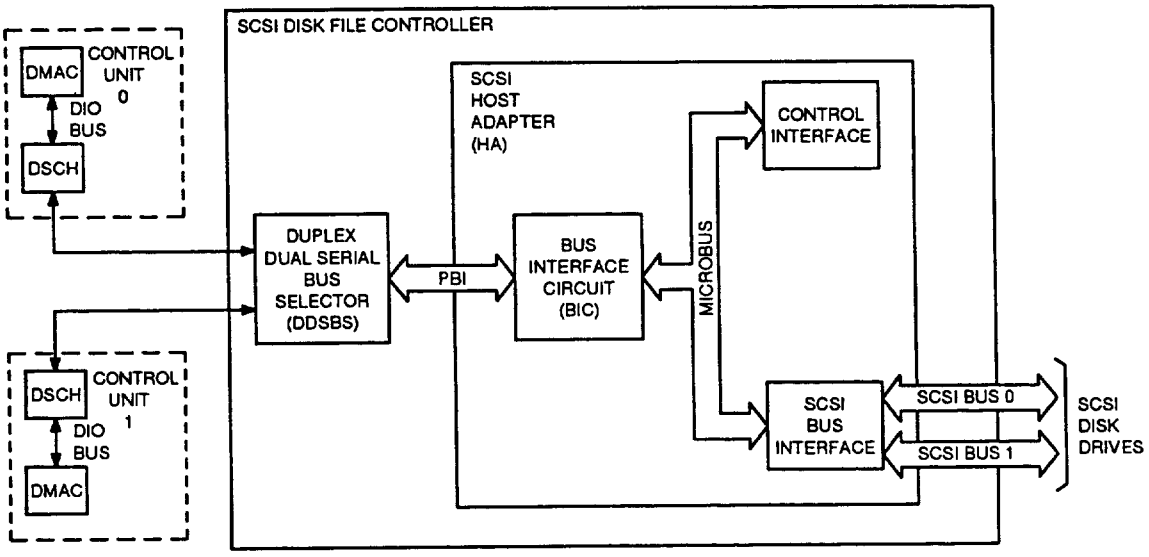


Figure 7. SCSI Disk File Controller Functional Diagram

3.05 The DDSBS is interfaced to the BIC by the PBI that consists of 46 active-low transitor-transitor logic TTL signals: 36 data leads, 5 control leads, and 5 response leads (Figure 6). The 36 bidirectional data leads are used to transmit data and commands or to receive data and status information from the DFC. The 36 data bits include four bytes with odd parity over each byte and even parity over the 36 bits. (One parity bit is associated with each 8-bit byte.)

3.06 The HA consists of the BIC, SCSI bus interface, and control interface. These functional units communicate over the microbus, a 32-bit parallel communications bus. The HA communicates with the SCSI disk drives via two independent differential SCSI buses.

C. SCSI Disk Unit Package

3.07 The SCSI disk unit package (DUP) consists of 5.25 inch SCSI disk drives, –48 V DC power supply converted to ±5 and ±12 V DC for the disk drives, power switch, and cooling fan. A growth package is available. Depending on system configuration, there can be up to 32 disk units: 4 SCSI DFCs, 2 SCSI busses per DFC, and 4 disks per bus.

Duplex Dual Serial Bus Selector

3.08 The DSCH to BIC interface is provided by the DDSBS. Two DSCH signal ports are provided on the DDSBS so either CC can access the disk drives. Access of the DDSBS by the CCs is arbitrated on a first-come-first-serve basis. Requests from the BIC are sent to both CCs. The DDSBS does the conversion between the serial format of the DSCH and the parallel format required by the HA. The DDSBS also does the signal-level conversions to drive the TTL level PBI between the DDSBS and the BIC.

A. Internal Circuitry

3.09 There are three types of communication between the HA and the 3B20D computer:

- Data transfers between the BIC and the 3B20D computer DMAC through the DSCH and DDSDB. Data is transferred between the DMAC and the HA as either single 32-bit words or 16-word blocks.
- Commands from the 3B20D computer are written into the command register and the control register.
- Status is read by the 3B20D computer from the BIC status register (BSR) and HA shadow register.

3.10 The DDSBS (Figure 8) consists of the following circuits.

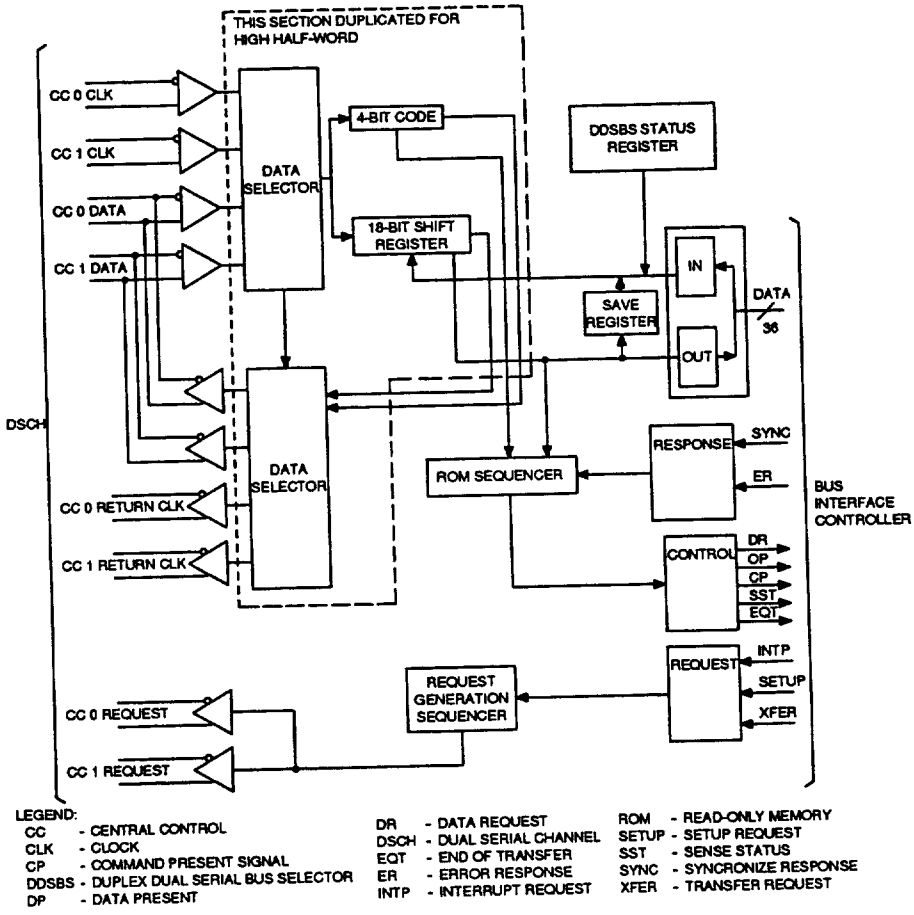


Figure 8. Duplex Dual Serial Bus Selector Functional Diagram

(a) **4-Bit Code:** The 4-bit code counts the number of bits in the CC half-word that have been shifted into the DDSBS. Two 4-bit code counters are cascaded to accommodate the CC word (2 half words).

(b) **DDSBS Status Register:** The DDSBS status register contains a 16-bit status word used to report status information to the CC describing the DDSBS internal conditions. (Only bits 0 through 7 are used.) Each bit is set by a response for a circuit operation (normal or abnormal). Bits 0 through 7 of the DDSBS status register are described in Table A.

Table A. Duplex Dual Serial Bus Selector Status Register Layout

BIT	DESCRIPTION
0	A peripheral device reported error indicates the current state of the error lead from the peripheral device.
1	An overflow error indicates one of two possible overflow conditions: overwrites or overreads. Overwrites occur on a block write to a peripheral device when a word of the block has been completely shifted into the DDSBS before the previous word read has been accepted by the peripheral device. Overreads occur on a block read of a peripheral device when a word of the block has been completely shifted out of the DDSBS before the next word has been delivered by the peripheral device. Both sources of overflow cause an interrupt to be generated.
2	A sequencer error indicates that the channel sequence has branched to an illegal location.
3	An illegal DDSBS command indicates an illegal DDSBS command which is not defined has been received.
4	The maintenance flop-flop state indicates the state of the maintenance flip-flop.
5	The peripheral device interrupt state indicates the status of the interrupt queue generated while the DDSBS is in the maintenance mode.
6	The peripheral device setup indicates the status of the setup queue generated while the DDSBS is in the maintenance mode.
7	The peripheral device transfer indicates the status of the transfer queue generated while the DDSBS is in the maintenance mode.

(c) **18-Bit Shift Registers:** Two 18-bit shift registers, each consisting of five 4-bit shift registers, shift either incoming (BIC to DDSBS) or outgoing (DDSBS to DSCH) messages (by half-words). The one used to handle incoming messages is left-adjusted, and the one used for outgoing messages is right- adjusted to handle the offset of 20 bits versus 18 bits (I6 data bits plus 2 parity bits).

(d) **Read-Only Memory Sequencer:** The read-only memory (ROM) sequencer controls DDSBS internal operations. While the DDSBS is idle, the ROM sequencer is forced into an idle state. When one port becomes active, the ROM sequencer executes a loop while waiting for the start code to complete shifting. When shifting of the start code is completed, a routine is accessed and then executed.

(e) **Request Generation Sequencer:** The request generation sequencer accepts three types of requests from two sources and encodes them as three pulse widths in a single request line. The three types of requests are transfer, set up, and interrupt. The two sources are the BIC and the DSCH. Priority of the two sources of request inputs is determined by the maintenance register.

(f) **Save Register:** When the DDSBS is in the maintenance mode, a "write word" operation places information into the save register while a "read word" operation retrieves information from the save register.

(g) **Data Selector:** The data selector consists of two cross-coupled retriggerable 1-shots used to determine the CC to be acknowledged. Only one 1-shot may be active at a time.

(h) **Interface Logic:** Ten gates interface the DDSBS to the BIC by the PBI signals.

B. Interfaces

3.11 The DDSBS is interfaced to the DSCH by two bidirectional data leads, a transmit clock lead, a receive clock lead, and a request lead. The DDSBS is interfaced to the BIC by the PBI. The transmit clock from the DSCH is 20 MHz allowing a cable length (between the DSCH and DDSBS) of up to 100 feet.

3.12 The PBI provided in the DDSBS consists of 46 active-low TTL signals: 36 data leads, 5 control leads, and 5 response leads (Figure 6). The 36 bidirectional data leads transmit data/commands or receive data/status from the BIC. The 36 data bits include four bytes with odd parity over each byte and even parity over the 36 bits (eight data bits and one parity bit). (See Table B for a description of the PBI signals.)

Table B. Peripheral Bus Interface Signal Descriptions

SIGNALS	DESCRIPTION
Command present (CP)	Indicates to the DFC that information has been placed on the information (INF) leads, is valid, and is to be interpreted as a command. (The INF leads consist of 32 data plus 4 parity signals.)
Data present (DP)	Indicates to the DFC that information has been placed on the INF leads, is valid, and is to be interpreted as data.
Data request (DR)	Indicates that the DDSBS would like the DFC to gate data information onto the INF leads.
Sense status (SST)	Indicates that the DDSBS would like the DFC to gate data information onto the INF leads.
End of transfer (EOT)	Indicates that the DDSBS has received an EOT indication from the direct memory access controller (DMAC).
Synchronize (SYNC)	Upon receiption of a control signal, the DFC performs the prescribed operation and sets the SYNC signal. This signal is cleared in response to removal of the control signal.
Error (ER)	The DFC sets the ER signal whenever an abnormal condition has been detected. Signal ER is checked by the DDSBS after the SYNC response is received.
Interrupt request (INT)	When a DFC requests CC actions, the INT signal is set to inform the CC of need.
Transfer request (XFER)	The DFCs connected to the DSCH set the XFER signal to notify the DMAC that it is ready to transmit or receive another word or block during a data transfer. Also, this signal can be used to generate service request interrupts to the CC for DFCs connected to the DSCHs equipped on the central control input/output (CCIO) bus.
Setup request (SETUP)	A DFC may initiate a DMAC setup by setting the SETUP signal. The DMAC will acknowledge the request by transmitting the DR control signal to retrieve the setup information. The setup signal can be used to generate service requests for DFCs connected to DSCHs equipped on the CCIO bus.

C. Operation

3.13 The DDSBS operation is controlled by the command signal (maintenance mode). Bits 1 through 4 (4-bit code) of the DDSBS command word determine the operation. Bit 0 of the DDSBS command word is always a 1 and is used as a detection bit in the shift register. The format and corresponding DDSBS maintenance operation of bits 1 through 4 of the DDSBS command word are as follows.

(a) Bit 0000 clears the DDSBS error register.

(b) Bit 0011 sets the DDSBS in the maintenance mode.

(c) Bit 0101 sets the DDSBS in the operational mode.

(d) Bit 1001 generates the setup request.

(e) Bit 1010 generates the interrupt request.

(f) Bit 1011 generates setup and interrupt requests.

(g) Bit 1100 generates the transfer request.

(h) Bit 1101 generates transfer and setup requests.

(i) Bit 1110 generates transfer and interrupt requests.

(j) Bit 1111 generates transfer, setup, and interrupt requests.

3.14 Input receivers and output drivers to the CC (in the DSCH) are wired so that only one CC can access the DDSBS at any given time. These circuits interface the bus connected to the DSCH with the data selectors and request generation sequencer.

3.15 The 36-bit data leads (two) are bidirectional and are used to send and receive information between the DSCH and the DDSBS. The request signal lead, when set, notifies the CC that the DDSBS requires its services. The transmit clock signal lead provides internal timing for the DDSBS. The receive clock gates timing information to the DSCH from the DDSBS.

3.16 A sync signal is generated by the BIC in response to any control signal that has been properly received and processed by the BIC. The interrupt transfer and setup leads are set to 1 at any time the BIC needs to interrupt the CC, whether it is addressed or not.

3.17 Data from the DSCH is gated into the DDSBS receivers and then into the data selectors. Data from the data selector is shifted into the 18-bit shift register. Data is then checked for the start code. Information is gated to the ROM sequencer that generates the signals to control internal operations of the DDSBS. After the data is checked and is determined to be valid, the appropriate command is sent to the BIC and data transmission follows.

3.18 When the BIC has information for the CC, it sets its request signal. The CC responds with the appropriate command. The DDSBS sets up to receive the data from the BIC. The data is sent to the shift register, is shifted out to the data selector, and is gated to the DSCH.

3.19 Status information from the BIC and DDSBS is gated into the DDSBS status register. This information is retrieved by the CC by an RST command. Data in the status register is shifted into the shift register and is then shifted out into the data selector and gated to the DSCH.

3.20 The CC generates the command to clear the status register and error circuits and sets the DDSBS into a known state. The CC also generates the command to set the DDSBS into the maintenance mode for diagnostics.

SCSI Host Adapter

3.21 The SCSI host adapter (HA) consists of one UN294 circuit pack, one TN2116 circuit pack, and a 32-bit microbus.

A. UN294 and TN2116 Circuit Packs

3.22 The UN294 circuit pack contains the bus interface circuitry and the SCSI bus interface. The TN2116 contains the control interface and a WE®32104 integrated circuit DMAC.

B. Microbus

3.23 The microbus is a 32-bit parallel communications bus that connects the functional circuits within the BIC, control interface, and the SCSI bus interface. All UN294 and TN2116 registers are memory mapped and addressable by the HA CPU.

3.24 The address map for the microbus is shown in Table C.

Table C. Microbus Address Map

Address	Devices	Location
00000000-000FFFF	RAM (1 Mbyte)*	TN2116
01000000-0103FFF	EPROM (256 Kbytes)*	TN2116
02XXXXXX	FIFO	UN294
030000XX	BIC Status Register†	UN294
030001XX	BIC Command Register†	UN294
030002XX	PIC Pulse Points†	UN294
030003XX	System Timer Control†	UN294
030004XX	BIC Control Register†	UN294
030005XX	Host Adapter Status Register†	TN2116
030006XX	SCSI Status Register†	UN294
030007XX	USART†	TN2116
030008XX	Write Protect Register†	TN2116
030009XX	SPCA†	UN294
03000AXX	SPCB†	UN294
03000BXX	FDCR†	UN294
04000000-040FFFFF	RAM (1 Mbyte)*	TN2116

* When bit 15 in the HASR (Address Overlap Inactive) is cleared, the address range 00000000-000FFFFF is mapped to the EPROM (address bits MADD181 and MADD191 are ignored). The EPROM responds to all read operations in the address range 00000000-000FFFFF and 01000000-0103FFFF. Write operations while overlap is active in these address range are ignored.

An attempt to access any memory location outside the address table shown above will generate a fault to the HA CPU, the HA CPU hence will go through a fault routine.

While the address overlap is active, the SRAM can be accessed through the address range 04000000-040FFFFF which is not affected by the address overlap but in the HASR. When the address overlap is inactive, the SRAM can be accessed by two physical addresses 00000000-000FFFFF or 04000000-040FFFFF.

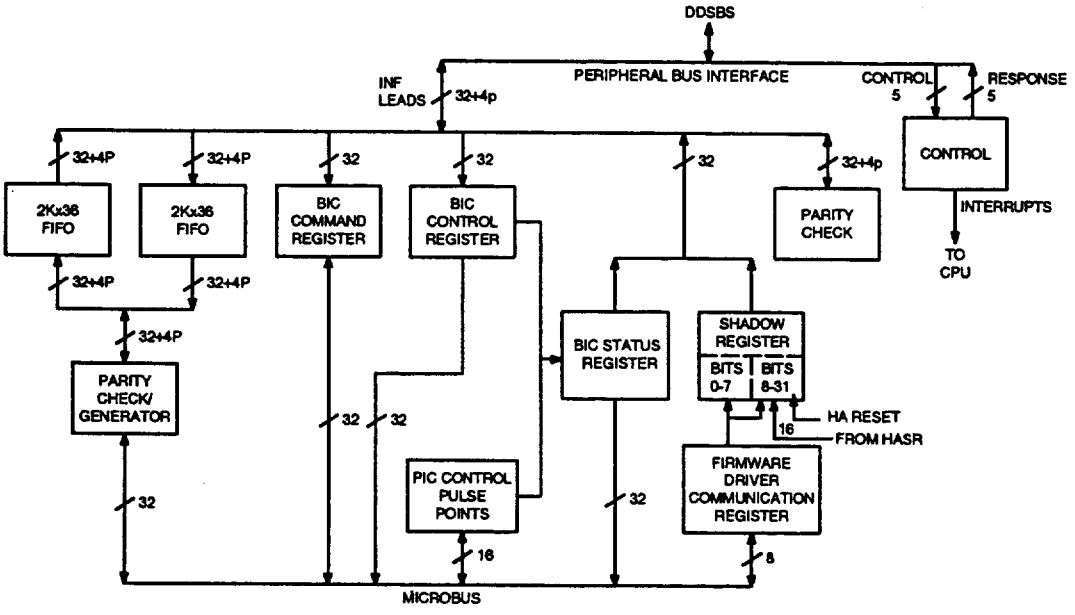
Notice that after RESET, level 15 interrupt acknowledge, or nonmaskable interrupt knowledgeable, address overlap is active.

When a certain part of memory (SRAM) is write protected, the SRAM is write protected irrespective of the two different address spectrum for the same physical address.

† The address bits 13-19 (MADD131-MADD191) are ignored for address decoding.

C. SCSI Bus Interface Circuit

3.25 The BIC (Figure 9) provides a buffer for the data, commands, and status information that passes between the 32-bit 3B20D computer, DDSBS, and the 32-bit SCSI HA and does the necessary handshaking to communicate with the DDSBS.



Legend:

BIC – Bus Interface Controller
CPU – Central Processing Unit
DDSBS – Duplex Dual Serial Bus Selector
FIFO – First-IN-First-Out
PIC – Peripheral Interface Controller

Figure 9. Bus Interface Controller Functional Diagram

The SCSI BIC contains:

(a) 32-bit BIC command register

(b) 32-bit BIC status register (BSR)

(c) 32-bit BIC control register

(d) 32-bit PIC control pulse points

(e) Control logic

(f) Parity checkers.

BIC - HA Communication

3.26 The BIC communicates with the other circuits in the HA via the microbus. The BIC first-in first-out (FIFO) data buffers, BIC command register, BIC control register, BIC status register, firmware-driver communication register, and the counters associated with 3B20D computer to BIC data transfers are all addressable by the HA CPU.

3.27 Data is transferred between the HA and the BIC FIFOs under the control of the HA DMAC or the HA CPU. The HA CPU/DMAC can transfer data between the FIFOs and the HA static random access memory (SRAM), and between the FIFOs and the SCSI protocol converters (SPCs). Transferring data between the SRAM and the FIFOs allows double-buffering of data (e.g., data can be transferred from the SPCs to SRAM and then from the SRAM to the FIFO).

3.28 The BIC FIFOs support single-word, double-word, and quad-word transfers. A single word is 4 bytes. Half-word and byte transfers are not supported.

3.29 Parity is checked when the HA CPU or DMAC reads the BIC FIFO, and is generated when the FIFO is written. The results of the parity checks are saved as two bits in the BSR. The HA CPU can enable and disable the BIC FIFO parity checks through two bits in the PIC control pulse points. When the parity checking is disabled, the check results are not clocked into the BSR, and bad parity is not written into the HA SRAM or onto the SCSI bus because the parity from the FIFOs is not carried on the microbus. New parity is generated on writes of the SRAM and when the SPCs place data on the SCSI bus.

BIC Command Register

3.30 The BIC command register is used for commands from the CU. The CU writes commands into this register, using CU programmed input/output (PIO) instructions, that are read and executed by the HA CPU under firmware control. The HA CPU can also write this register for diagnostic use. The command present (CP) signal from the DDSBS signifies the presence of a command to the BIC circuitry. The three low order bits (2-0) in the command word signify the destination of the command word as follows:

- 000 signifies the BIC control register as the destination
- 010 signifies the BIC command register as the destination
- XX1 signifies the DDSBS (maintenance command) as the destination.

3.31 When the CU writes the command register, the command flag in the BSR is set and the "information present in BIC command register" interrupt is sent to the HA CPU. The program executing in the HA CPU controls the interpretation and execution of the command.

BIC Status Register

3.32 The BSR provides 32 bits of status and error flags that can be read by both the CU and the HA. The CU reads the BSR through the sense status (SST) control signal. When the DDSBS asserts SST, the status word is gated onto the INF leads. The HA CPU can read this register as either a full 32-bit word or as two 16-bit half-words. Neither the CU nor the HA CPU has direct write access to the BSR, but both can set and reset some flags through the BIC control register and the PIC control pulse points. Many of the flags are set and reset by asynchronous hardware events. The layout of the BSR is shown in Table D. These flags are segmented into status flags (16 bits) and error flags (16 bits). The status flags are as follows.

(a) **Command Flag:** The command flag is set when the BIC hardware signifies that the CU has written a command into the BIC command register. The flag is cleared when the HA CPU reads the command register. The command flag is used as the "information present in BIC command register" interrupt to the HA CPU. When the HA firmware is in single-thread mode (executing one job at a time), this interrupt is masked and the command flag is polled.

(b) **Command-in-Progress Flag:** The command in progress flag signifies that a command from the 3B20D computer is being executed. It is set when the command flag is set. It is cleared by the HA CPU and in the SCSI DFC when cleared, indicates that the DFC is not actively involved in writing a disk and therefore, it is safe to reset the DFC if necessary for recovery. It can also be set by the HA CPU. The CU can clear this flag through a bit in the BIC control register.

(c) **Data Flag:** The data flag signifies whether the CU can access the BIC FIFOs. When it is cleared (0), the CU can access the FIFO. The HA CPU can set and clear this flag. Under some circumstances, the HA firmware will poll this flag to detect when a 3B20D computer DMA job is done. The BIC hardware can set this flag to signify that a DMA job is complete. The "read/write word/block complete" interrupt is sent to the HA CPU when a DMA job finishes. The hardware toggles the data flag when the EOT signal is asserted to signify that an EOT transfer has completed.

(d) **Data Transfer-Mode Flag:** The data transfer mode flag signifies whether data transfers between the BIC FIFOs and DDSBS occur as single 32-bit word transfers or as 16-word block transfers. This flag can be set (1) to block mode and cleared (0) to word mode under software control by both the 3B20D computer and the HA CPU.

Table D. BIC Status Register

Bit	Function
0-3	Device address
4	3B20 Computer DMA setup overwrite error
5	INF parity error - byte 0
6	INF parity error - byte 1
7	INF parity error - byte 2
8	INF parity error - byte 3
9	End-of-data error
10	HA fatal error summary
11	Sanity error
12	BIC FIFO parity error - low halfword
13	BIC FIFO parity error - high halfword
14	FIFO overflow/underflow
15	BIC command register overflow/underflow
16-20	Word-in-block count
21	3B20 Computer interrupt request
22	3B20 Computer DMA transfer request
23	3B20 Computer DMA setup request
24	End-of-data expected
25	End-of-data received
26	Data transfer mode (0=word, 1=block)
27	BIC FIFO parity checks enabled
28	BIC - HA CPU interface enabled
29	Data flag (0=3B20D computer, 1=HA)
30	Command in progress
31	Command flag

(e) **Word-In-Block Count:** The word-in-block count flag is a 5-bit valve. When data is transferred between the BIC and the CU in block mode, the 5-bit word-in-block count flag IFO memory (0 through 16). The count is incremented whenever a word is loaded and decremented whenever a word is unloaded.

(f) **Interrupt Flag:** is unloaded.

(g) **3B20 Computer Interrupt Request Flag:** The interrupt request flag is set whenever interrupt service from the CU is requested. It is set and cleared under software control. The CU sets and clears this bit through the BIC control register. The HA CPU sets this bit through the PIC control pulse points. The HA uses this bit to request service of (or signal job completions to) the 3B20D computer.

(h) **3B20D Computer DMA Transfer Request Flag:** The 3B20D computer DMA transfer request flag signifies that a DMA transfer has been requested from the 3B20D computer DMAC. When a series of DMA transfers are to be done, this flag is initially set by the HA CPU under program control. Further DMA transfers are requested by the BIC hardware until all the data in the DMA job has been transferred. These hardware-initiated transfers are halted if an error is detected during a transfer. The term "error" refers to any of the errors registered in the BSR. The HA CPU sets this flag again for the final transfer of a DMA job. The expected response from the 3B20D computer DMAC to this final request is the end-of-transfer (EOT) signal. The CU can set this flag through the BIC control register for 3B20D computer diagnostics. The transfer request flag is cleared when the CU reads or writes the FIFOs. It is also cleared by the EOT signal.

(i) **3B20D Computer DMA Setup Request Flag:** The 3B20D computer DMA setup request flag signifies that the HA has requested a 3B20D computer DMA setup. The HA transfers setup information to the 3B20D computer DMAC by sending it two setup words. When a setup word is present in the FIFO, the HA sends a setup request to tell the DMAC that the setup information is available. The setup request flag is set under software control by the HA and the CU. Allowing the CU flag to set if it is provided for diagnostics.

(j) **End-of-Data Expected Flag:** The end-of-data expected flag is set by the HA CPU before it requests the final transfer of a DMA job. The expected response to this request is EOT. The HA CPU can reset this flag along with the end-of-data received flag. The end-of-data expected flag can be set under 3B20D computer control through the BIC control register for 3B20D computer system diagnostics.

(k) **BIC FIFO Parity Checks Enabled Flag:** Parity is checked when the HA CPU/DMAC reads the BIC FIFO. These parity checks can be enabled and disabled by the HA CPU. When this flag is set, the parity checks are enabled.

(l) **BIC-HA CPU Interface-Enabled Flag:** This flag signifies that the HA CPU/DMAC can access the BIC FIFO, registers, and counters. The ability to disable this interface is provided to prevent the HA from making requests of the 3B20D computer DMAC when the 3B20D computer DMAC is not prepared for them.

3.33 The following flags are set by "soft" HA errors. They can be cleared by the HA CPU through a clear soft errors command, by the 3B20D computer through a clear BIC command and by a power clear. The HA CPU is inhibited from writing all PIC control pulse points except for clear soft errors when a soft error flag is set.

(a) **BIC Command Register Overflow/Underflow Flag:** This flag is set if the HA CPU attempts to read the command register when it is empty or write it when it is full. This write is inhibited.

(b) **FIFO Overflow/Underflow Flag:** This is automatically set when the HA CPU/DMAC or 3B20D computer attempts to read the FIFO when it is empty or write it when it is full. The FIFO integrated circuits (IC)s automatically inhibit these reads and writes. FIFO overflow/underflow generates a maskable interrupt to the HA CPU.

(c) **FIFO Parity Error Flags:** These two bits are the result of parity checks on reads of the BIC FIFO by the HA CPU or DMAC.

3.34 The following flags are fatal HA errors. They can only be cleared by the CU through a BIC clear command or a power clear.

(a) **Sanity Error Flag:** This flag is set automatically when the HA sanity timer overflows.

(b) **HA Fatal Error Summary Flag:** This flag is set automatically when the HA sanity timer overflows. It can also be set under firmware control by the HA CPU.

3.35 The following flags are 3B20D computer interface errors. They can only be cleared by the 3B20D computer through a BIC clear command and by a power clear.

(a) **End-of-Data Error Flag:** This flag is automatically set if the 3B20D computer attempts a data read or write when the end-of-data expected flag is set, or if the EOT signal from the DDSBS goes active when the end-of-data expected flag is not set. This error signifies miscommunication between the HA and the 3B20D computer DMAC.

(b) **DMA Setup Overwrite Error Flag:** This flag is automatically set if a 3B20D computer DMA setup request is pending (the setup word for the DMAC is in the FIFO), and the 3B20D computer attempts to write data into the FIFO. This error signifies miscommunication between the 3B20D computer DMAC and the HA.

(c) **Information Parity Failure Error Flags:** These are the results of the parity checks done on command and data transfers across the INF leads. This error signifies a hardware failure.

PIC Control Pulse Points

3.36 The peripheral interface controller (PIC) control pulse points provide the HA firmware with a means to control operations within the BIC. The HA CPU sets and resets BIC status flags by writing these pulse points. They are called the "PIC" control pulse points because the function of the HA CPU is done by the "PIC" in the SMD DFC.

3.37 The PIC control pulse points (bits) are not latched and therefore not a physical register. The instructions derived from the bits are executed immediately by the BIC circuits. The bit layout of the PIC control pulse points is shown in Table E.

Table E. PIC Control Pulse Points Bit Layout

Bit	Function
0	Set 3B20 computer DMA transfer request
1	Set 3B20 computer DMA setup request
2	Set 3B20 computer interrupt request
3	Clear end-of-data expected and end-of-data received
4	Set end-of-data expected
5	Set word transfer mode
6	Set block transfer mode
7	Disable BIC FIFO parity checks
8	Enable BIC FIFO parity checks
9	Set HA fatal error flag
10	Clear soft errors
11	Clear BIC FIFOs
12	Point data flag toward 3B20 computer (0)
13	Point data flag toward HA (1)
14	Set command in progress
15	Clear command in progress
16	Next XFER is 3B20 computer write to HA
17	Next XFER is 3B20 computer read from HA

BIC Control Register

3.38 This 32-bit register stores the BIC control instructions from the CU. These control instructions manipulate the BSR and control operations in the BIC. The instructions are executed immediately, and the bits are latched so that the HA CPU can read them. The layout of the BIC control register is shown in Table F.

Table F. BIC Control Register Layout

Bit	Function
0-2	000 designates this as a BIC control instruction
3	Set 3B20 computer DMA transfer request
4	Set 3B20 computer DMA setup request
5	Set end-of-data expected
6	Clear command in progress
7	Set 3B20 computer interrupt request
8	Clear 3B20 computer interrupt request
9	Set word transfer mode
10	Set block transfer mode
11	Set BIC - HA CPU interface enable
12	Clear BIC FIFOs
13	Clear BIC
14	Reset HA
15	Set shadow register read
16-31	Used only for driver-firmware communication

Shadow Register

3.39 The shadow register provides an additional path of communication from the HA firmware to the 3B20D computer disk driver. The CU reads this register after the HA has been reset. A reset HA instruction from the CU loads the shadow register with the state of the HA before the reset. After the CU reads the shadow register, the disk driver uses the information from the register to make choices about fault recovery. The register is written under hardware control. Bit 15 in the BIC control register allows the CU to read the shadow register through a sense status signal. The layout of the shadow register is shown in Table G.

Table G. Shadow Register Layout

Bits	Description
0-7	FDC register - current contents
8-15	FDC register - contents prior to last reset
16	HASR bit 01 - write protect violation
17	HASR bit 02 - parity error on SRAM
18	HASR bit 03 - BIC access error
19	HASR bit 08 - diagnostics in progress
20	HASR bit 10 - fault caused by diagnostics
21	HASR bit 11 - diagnostics passed
22	HASR bit 12 - DMAC channel 1 high priority
23	HASR bit 15 - address overlap inactive
24	HASR bit 18 - SCSI bus 0 enable
25	HASR bit 22 - SCSI bus 1 enable
26	HASR bit 30 - 3B20D computer DMA transfer in progress
27	HASR bit 31 - Power on reset
28	SCSI bus status register bit 03 - bus 0 differential sense
29	SCSI bus status register bit 07 - but 1 differential sense
30	Spare
31	Spare

Firmware-Driver Communication Register

3.40 This 8-bit register is used by the HA firmware as a repository for information for the 3B20D computer disk driver. The firmware-driver communication (FDC) bits are completely controlled by the HA firmware.

BIC FIFOs

3.41 To provide a data transfer rate between the 3B20D computer and the HA that meets the HA performance requirements, the BIC contains two 2K by 36-bit FIFO memories. One FIFO buffers data from the 3B20D computer to the HA and the other FIFO buffers data from the HA to the 3B20D computer.

Sequencers

3.42 Special sequencers in the BIC control the data transfers between the BIC FIFOs and the DDSBS. The sequencers do the handshaking between the BIC and the DDSBS needed to transfer data, provide the read and write signals for the FIFOs, monitor the number of words or blocks to be transferred, and control the issuing of 3B20D computer DMA transfer requests. This accelerates data transfers by offloading these responsibilities from the HA CPU.

3.43 The sequencers use several counters to interface with the FIFOs and as test inputs to decide when to provide the appropriate handshakes. These counters are:

(a) **Word/Block Counter:** This 16-bit counter monitors the number of words or blocks to be transferred in a job. The HA CPU has read/write access to this counter and loads it with the appropriate initial value at the start of each job.

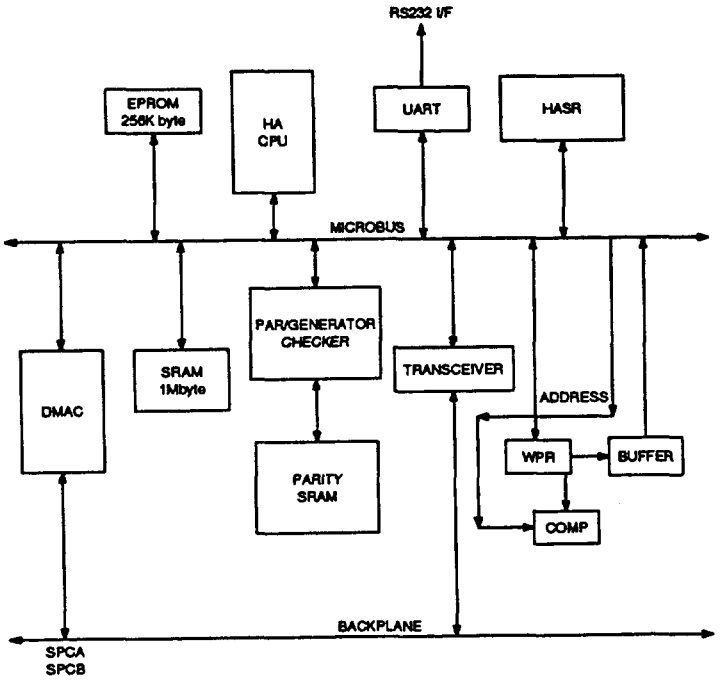
(b) **Word-Within-Block Counter:** This 5-bit counter monitors the number of words within a particular 16-word block that are in the FIFOs. It counts down from 16 to 0 during 3B20D computer reads of the FIFO and up from 0 to 16 during writes. The output of this counter is registered as bits 16 - 20 of the BSR.

(c) **Transfer Request Delay Counter:** This 16-bit counter allows the time between successive 3B20D computer DMAC transfer requests to vary. Providing delays between transfer requests insures that the HA does not monopolize its DSCH. The HA CPU has read/write access to this counter.

D. SCSI Control Interface

3.44 The control interface of the SCSI HA provides intelligent control necessary to process commands from the 3B20D computer/CU and manage the two SCSI busses. The control interface (Figure 10) contains the following components:

- CPU
- SRAM
- EPROM
- Microbus
- Status register
- Write protect register
- Timers.



Legend:

COMP – Completion
CPU – Central Processing Unit
DMAC – Direct Memory Access Controller
EPROM – Erasable Programmable Read Only Memory
HA – Host Adapter
HASR – Host Adapter Status Register
PAR – Parity
SPC – SCSI Protocol Controller
SRAM – Static Random Access Memory
WPR – Write Protect Register

Figure 10. SCSI Control Interface

Host Adapter Central Processing Unit

3.45 The HA CPU does the following functions on the microbus:

- Memory read
- Memory write
- Read and write to the DMAC, MFP, SPC internal registers, and registers on both the UN294 and TN2116 circuit packs
- Microbus arbitration
- Fault handling

- Interrupt handling
- Reset for the UN294 and TN2116 circuit packs.

Host Adaptor Static RAM

3.46 The HA has one megabyte of SRAM.

3.47 The SRAM provides:

- Byte, half-word, double-word, and quad-word transfers. The block fetch is supported for the double-word and quad-word transfers. A wait state is required on the second, third, and fourth word fetch of a block fetch transfer.
- Zero wait state HA CPU and DMAC read and write
- Write protection of two specified ranges of the memory
- Parity bit generation for each byte on the memory write
- Memory read parity check
- Forcing bad parity on individual bytes.

EPROM

3.48 The HA has 256 kbytes of erasable programmable read only memory (EPROM) arranged in four 64-K X 8-bit EPROMs. EPROM supports the following:

- Byte, half-word, and word read
- Overlap the SRAM when the overlap inactive bit is cleared in the host adapter status register (HASR).

Host Adapter Status Register

3.49 The HASR is a 32-bit register. The HA CPU can read this register a byte at a time and write to each bit individually with each bit having an address. Table H shows the layout of the HASR.

Table H. Host Adapter Status Register

Bit	Description	Read Address	Write Address
00	Sanity Failure	03000503	03000503
01	Write Protect Violation	03000503	03000507
02	Parity Error on SRAM	03000503	0300050B
03	BIC Access Error	03000503	0300050F
04	Force Bad Parity Byte 0	03000503	03000513
05	Force Bad Parity Byte 1	03000503	03000517
06	Force Bad Parity Byte 2	03000503	0300051B
07	Force Bad Parity Byte 3	03000503	0300051F
08	Diagnostics in Progress	03000523	03000523
09	Spare	03000523	03000527
10	Fault Caused by Diagnostics	03000523	0300052B
11	Diagnostics Passed	03000523	0300052F
12	32104 Channel 1 High Priority	03000523	03000533
13	Mask (inhibit) interrupt level 13	03000523	03000537
14	Mask (inhibit) interrupt level 11	03000523	0300053B
15	Address Overlap Inactive	03000523	0300053F
16	SCSI Bus 0 Send Bad Parity	03000543	03000543
17	SCSI Bus 0 Receive Bad Parity	03000543	03000547
18	Enable SCSI Bus 0 Disconnect	03000543	0300054B
19	32104 Channel 0 Flush	03000543	0300054F
20	SCSI Bus 1 Send Bad Parity	03000543	03000553
21	SCSI Bus 1 Receive Bad Parity	03000543	03000557
22	Enable SCSI Bus 1	03000543	0300055B
23	32104 Channel 1 Flush	03000543	0300055F

Table H. Host Adapter Status Register (Cont)

Bit	Description	Read Address	Write Address
24	Mask (inhibit) interrupt level 10	03000563	03000563
25	Mask (inhibit) interrupt level 9	03000563	03000567
26	Over temperature SCSI Bus 0	03000563	0300056B
27	Over temperature SCSI Bus 1	03000563	0300056F
28	Power Disconnect SCSI bus 0	03000563	03000573
29	Power Disconnect SCSI bus 1	03000563	03000577
30	3B20D computer DMA transfer in progress	03000563	0300057B
31	Power On Reset	03000563	0300057F

Host Adapter Interrupts

3.50 The HA CPU can field 15 levels of maskable interrupts and a nonmaskable interrupt (NMI).

Maskable Interrupts

3.51 The HA uses the Auto Vector Interrupt scheme to interrupt the HA CPU. A 16 to 4 priority encoder generates interrupt signals for the HA CPU. The interrupt map (in decreasing priority) is shown in Table I.

Table I. HA CPU Interrupts

IPL0-3 3 2 1 0	Priority Level	PSW/PC Address	Detail
0 0 0 0	15	0x504	Parity Error, Write Protect Error, FIFO Overflow/Underflow
0 0 0 1	14	0x4FC	IDM (UART)
0 0 1 0	13	0x4F4	DSCH Error (BIC Error)
0 0 1 1	12	0x4EC	Software Timer 1
0 1 0 0	11	0x4E4	Information Present in BIC Command Register
0 1 0 1	10	0x4DC	SCSI Bus Controller 0
0 1 1 0	9	0x4D4	SCSI BUS Controller 1
0 1 1 1	8	0x4CC	Software Timer 2
1 0 0 0	7	0x4C4	3B20D computer read/write complete
1 0 0 1	6	0x4BC	32104 (HA DMAC)
1 0 1 0	5	0x4B4	Sanity 3/4 point time out

3.52 In the above table, level 15 has the highest priority. All these interrupts are auto vectored. As a result, the HA CPU does not look for the external value and does the interrupt acknowledge without memory acknowledge or bus exception. This saves CPU time required to fetch the external value for the interrupt vector from the interrupting device.

3.53 The microprocessor provides the interrupt vector by treating the inverted INTOPO input concatenated with the interrupt priority level input (IPLO- IPL3), as a vector number.

3.54 Interrupt level 7 (3B20D computer read/write complete) and level 11 (information present in BIC command register) can be individually masked by setting bits 13 or 14 in the HASR, respectively.

Nonmaskable Interrupts

3.55 The NMI is generated as a result of a fatal error on the HA circuit pack. When the CPU fails to reset the sanity timer before it times out, NMI is generated to the HA CPU. The HA CPU reponds to this interrupt by sending an interrupt acknowledge and executing the NMI subroutine. The NMI input is negated when the NMI acknowledge is received.

Address Overlap

3.56 The memory map for the HA is shown in Table J.

Table J. Memory Map for the SCSI HA

Address	Overlap Active	SCRAM		EPROM
		Read	Write	Read
00000000-000FFFFF *	No	Yes	Yes	No
00000000-000FFFFF *	Yes	No	No	Yes
01000000-0103FFFF	No	No	No	Yes
01000000-0103FFFF	Yes	No	No	Yes
04000000-040FFFFF *	No	Yes	Yes	No
04000000-040FFFFF *	Yes	Yes	Yes	No

* The physical address 00000000-000FFFFF and 04000000- 040FFFFF represents the same physical memory, that is, a write to the address 00000000 when the address overlap is inactive is same as writing to address 04000000.

3.57 The overlap scheme for the HA is:

- When bit 15 in the HASR is zero, address overlap is active
- On power up, reset, or when interrupt level 15, or NMI occurs, address overlap is made active
- When address overlap is active, the lower address is responded to by the EPROM as shown in the table
- Write protection is provided for the SRAM, not confined to any address spectrum.

Write Protect Register

3.58 Write protection is provided for the HA SRAM by the 16-bit write protect register (WPR). The WPR provides two values that are compared to the upper eight address bits of SRAM. The upper eight bits of the WPR provides the upper limit, and the lower eight bits provides the lower limit of write protected memory.

3.59 The upper eight bits of the SRAM address are compared with the upper limit and the lower limit values, stored in the WPR. When the address is between the upper limit and the lower limit, the write operation is completed without any error condition. The lower limit can go from address 00000000 - 000FFFFF, similarly the upper limit can go from 000FFFFF - 00000000. When two limits overlap, the whole memory is write protected.

3.60 When a memory write occurs in the protected memory area, bit 1 in the HASR is set and a level 15 interrupt is generated to the HA CPU.

3.61 On the RESET, the SRAM is not write protected. The CPU can read or write to the WPR.

Sanity Timer

3.62 The 16-bit sanity timer monitors sanity errors. The HA CPU has read/write access to this timer, that provides a CPU programmable interval. Normally, a total interval of 500 milliseconds is specified. When it reaches zero the second time without being reset by the HA CPU, it times out.

3.63 When a sanity error occurs (that is, when the sanity timer times out, a nonmaskable interrupt is sent to the HA CPU). A sanity failure also automatically sets the sanity error and the HA fatal error summary bits in the BSR and the sanity failure bit in the HASR.

3.64 When the sanity timer counts down to zero the first time, an interrupt is sent to the HA CPU after programmable interval. To prevent the sanity error, the interrupt routine must clear the timer before it counts down to zero a second time without being reset by the HA CPU.

Software Timers

3.65 Two 16-bit timers (software timer 1 & software timer 2) on the SCSI HA are controlled exclusively by the HA firmware/pumpcode. These timers provide the timed intervals needed during program execution.

3.66 These timers count down and each causes a maskable interrupt to be sent to the HA CPU when the count of all zero is reached. They can be loaded into any initial value under software control, and the accumulated count can be read by the HA CPU.

E. SCSI Bus Interface

3.67 The SCSI bus interface is shown in Figure 11.

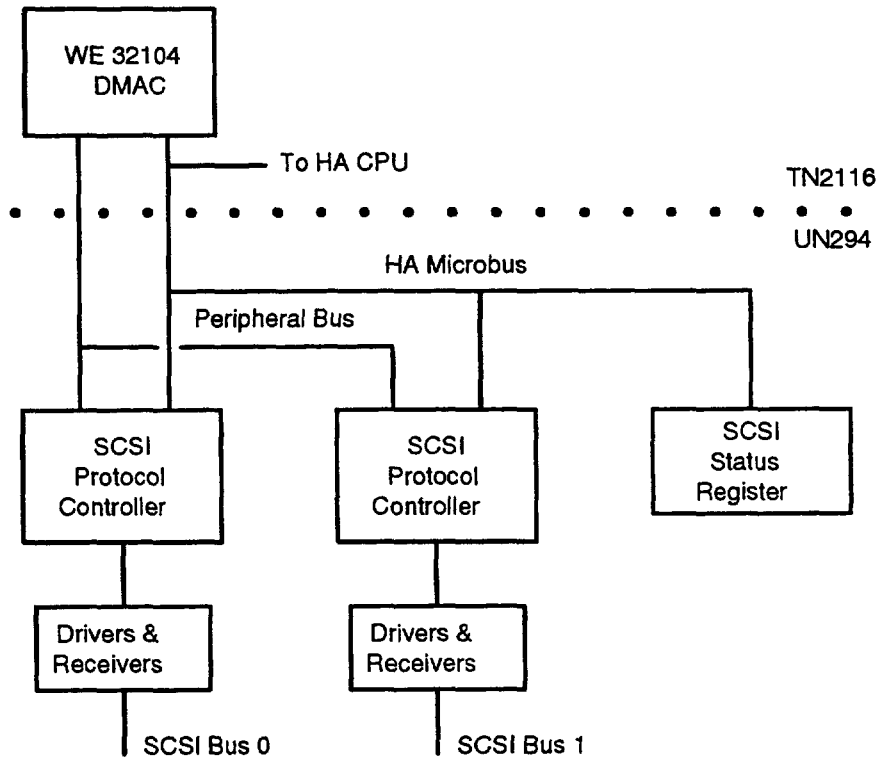


Figure 11. SCSI Bus Interface

SCSI Buses 0 and 1

3.68 The HA contains two independent differential SCSI buses, internally labeled bus 0 and bus 1, that conform to the ANSI and AT&T SCSI specifications.

SCSI Protocol Converters 0 and 1

3.69 Each SCSI bus is controlled by an SCSI protocol controller (SPC). With help from the HA CPU, this device provides all data and control signals needed to execute the SCSI bus protocol. It provides a data port to be used by the HA CPU to program SCSI bus operations by accessing internal registers. It also provides a high-speed port for block transfers.

3.70 The functions provided by the SPCs are:

- Either an initiator or target synchronous mode transfer with programmable offset (up to 8 bytes)
- Synchronous data transfer rate programmable at four rates

- 4-megabyte/second maximum synchronous data rate
- 8-byte data buffer
- 24-bit byte transfer counter
- Independent data transfer bus.

3.71 Two SPCs (0 and 1) are used on the HA. SPC 0 controls SCSI Bus 0 and SPC 1 controls SCSI Bus 1. They can operate completely independently.

3.72 Each SPC provides three data ports that are used as follows:

(a) **CPU Data Bus:** The SCSI data bus is connected to the HA microbus. It allows the HA CPU to access the internal SPC registers to program SCSI operations. Short data transfers can also be made through this bus using manual transfer mode.

(b) **DMA Data Bus:** The DMA data bus is connected to the DMAC peripheral data bus. High-speed data transfers are made on this bus under control of the DMAC. SPC 0 is controlled by DMAC Channel 0 and SPC 1 by DMAC Channel 1.

(c) **SCSI Bus:** The SCSI bus is connected to differential bus transceivers. These signals interface directly to the SCSI bus.

3.73 The SPCs are clocked at 8 MHz. This allows four synchronous data transfer rates of 4.00, 2.67, 2.00, and 1.60 megabytes/second to be selected under firmware control. Asynchronous data transfer is also supported on both buses.

3.74 The SPC registers and their addresses are listed in Table K. Each SPC has an independent set of registers, and all registers are 8 bits.

Direct Memory Access Controller

3.75 The HA direct memory access controller (DMAC) is a WE32104 microprocessor that provides high-speed data transfers between the SCSI buses and the HA RAM or the BIC FIFOs. The HA DMAC functions are:

- SCSI bus data transfers without CPU intervention
- High-speed transfers to and from RAM or FIFOs and using quad-word reads and writes
- Data packing - assembling bytes from a disk drive into quad-word operands for RAM or FIFOs and disassembling quad-words into bytes for a disk drive for reduced microbus occupancy.

3.76 The HA DMAC's control, and 32-bit address and data buses are connected to the HA microbus. This allows the HA CPU to access the DMAC's internal registers, and allows the HA DMAC to address the HA RAM and the BIC FIFOs with the same addresses used by the HA CPU. The HA DMAC's 8-bit peripheral bus is connected to the DMA data ports of both SPCs.

Table K. SPC 0 Register Address Map

Address	Register Name	Abbr.	Access Type
03000903	Bus Device ID	BDID	R/W
03000907	SPC Control	SCTL	R/W
0300090B	Command	SCMD	R/W
0300090F	Transfer Mode	TMOD	R/W
03000913	Interrupt Sense	INTS	R
03000913	Reset Interrupt	INTS	W
03000917	SPC Diagnostic Control	SDGC	W
0300091B	SPC Status	SSTS	R
0300091F	SPC Error Status	SERR	R
03000923	Phase Control	PCTL	R/W
03000927	Modified Byte Counter	MBC	R
0300092B	Data Register	DREG	R/W
0300092F	Temporary Register	TEMP	R/W
03000933	Transfer Counter High	TCH	R/W
03000937	Transfer Counter Middle	TCM	R/W
0300093B	Transfer Counter Low	TCL	R/W
0300093F	External Buffer (not implemented)	EXBF	

Note:
SPC 1 has an identical set of registers. To access corresponding registers in SPC 1, add 100 (hex) to the above addresses.

HA DMAC - CPU Operations

3.77 The HA CPU must access the DMAC's internal registers to program HA DMAC operations. The HA DMAC registers and their addresses are listed in Table L. Note that HA CPU access to the peripheral bus is not supported and should not be used.

Disk Write Read

3.78 The HA DMAC treats a CPU access to a register as a word transfer. If a register smaller than 32 bits is read, the lower bits of the data bus contain the register value, and the upper bits contain zeros. When such a register is written, the lower bits are used and the upper bits are ignored.

3.79 If any HA DMAC channel has an interrupt pending and enabled, the HA DMAC will interrupt the HA CPU at interrupt level 6. These interrupts can be individually masked via the DMAC channel mode registers. The channel interrupt vector registers must be initialized before an interrupt is enabled.

HA DMAC - Peripheral Operations

3.80 The HA DMAC peripheral bus is used to transfer bytes of data between the HA DMAC and the DMA data ports of the SPCs. SPC 0 is controlled by HA DMAC channel 0, and SPC1 by HA DMA channel 1. All four channels can also be used for memory copy and fill operations. Because each SPC has only one DMA port, the peripheral address bus is not used. Peripheral bus transfers must use synchronous burst mode and two wait states. These considerations require that two HA DMAC registers be programmed with the following values:

- Channel 0 device control register - 2500
- Channel 1 device control register - 6500.

HA DMAC Mask 4 Limitations

3.81 The SCSI HA uses mask 4 of the HA DMAC, that has the following limitations:

- Should do all peripheral-to-memory (PTM) transfers using the chain mode
- Should begin all memory-to-peripheral (MTP) transfers word aligned
- Asserts the block access (BLKACS) signal for MTP transfers if the HA DMACs mode register is set for multiword accesses
- Should not use 0 wait state peripheral accesses when doing PTM transfers
- While doing quad-word PTM transfers in chain mode, all data blocks (except for the last block) may not end misaligned on the first byte of a word.

Table L. HA DMAC Register Address Map

Address (Hex)	Register Name	Size (Bits)
03001800 - 030019FF	Access to Peripheral Bus (not implemented)	
03001A00	Channel 0 Source Address	32
03001A04	Channel 0 Destination Address	32
03001A0C	Channel 0 Base Address	32
03001A10	Channel 0 Transfer Count	16
03001A18	Channel 0 Interrupt Vector	16
03001A20	Channel 0 Status and Control	16
03001A24	Channel 0 Mode	16
03001A28	Channel 0 Device Control	16
03001A80	Channel 1 Source Address	32
03001A84	Channel 1 Destination Address	32
03001A8C	Channel 1 Base Address	32
03001A90	Channel 1 Transfer Count	16
03001A98	Channel 1 Interrupt Vector	16
03001AA0	Channel 1 Status and Control	16
03001AA4	Channel 1 Mode	16
03001AA8	Channel 1 Device Control	16
03001B00	Channel 2 Source Address	32
03001B04	Channel 2 Destination Address	32
03001B0C	Channel 2 Base Address	32
03001B10	Channel 2 Transfer Count	16
03001B18	Channel 2 Interrupt Vector	16
03001B20	Channel 2 Status and Control	16
03001B24	Channel 2 Mode	16
03001B28	Channel 2 Device Control	16
03001B80	Channel 3 Source Address	32
03001B84	Channel 3 Destination Address	32
03001B8C	Channel 3 Base Address	32
03001B90	Channel 3 Transfer Count	16
03001B98	Channel 3 Interrupt Vector	16
03001BA0	Channel 3 Status and Control	16
03001BA4	Channel 3 Mode	16
03001BA8	Channel 3 Device Control	16
03001C10	Mask	8
03001E00	Channel 0 Memory Fill Data	32
03001E80	Channel 1 Memory Fill Data	32
03001F00	Channel 2 Memory Fill Data	32
03001F80	Channel 3 Memory Fill Data	32

SCSI DFC Error Handling

A. Command or Data Transfer errors

3.82 One of the five response signals from the BIC to the DDSBS is the error signal ER. This signal signifies to the 3B20D computer CU whether an error has occurred during a command or data transfer. ER is sampled by the DDSBS after the BIC has sent the SYNC response signal to signify that the requested operation has been performed. The following errors assert the ER signal:

- Parity errors on data and command transfers between the BIC and DDSBS (INF parity errors)
- Parity errors on reads of the BIC FIFO by the HA CPU or DMAC (BIC FIFO parity errors)
- End of data error
- 3B20D computer DMA setup overwrite
- BIC command register overflow/underflow
- BIC FIFO overflow/underflow
- Sanity failure
- Error conditions signified by the HA CPU through the HA fatal error summary bit in the BIC status register.

B. Errors That Generate Interrupts

3.83 Sanity failure generates a nonmaskable interrupt to the HA CPU. This error also sets the sanity failure bit in the HASR and the sanity error and HA fatal error summary bits in the BIC status register.

3.84 Four maskable interrupts are triggered by errors. SRAM parity errors, SRAM write protect errors and BIC FIFO overflow/underflow generate a priority level 15 interrupt. SRAM parity errors occur when even parity is detected on reads of the HA SRAM. SRAM parity errors set bit 2 in the HASR. SRAM write protect errors occur when the HA CPU/DMAC writes to a protected area of SRAM. SRAM write protect errors set bit 1 in the HASR. FIFO overflow/underflow occurs when the HA CPU/DMAC or 3B20D computer attempts to write the BIC FIFO when it is full or read it when it is empty.

3.85 The following BIC errors generate a priority level 13 interrupt:

- BIC access error
- INF parity errors
- BIC FIFO parity errors
- 3B20D computer DMA setup overwrite

- End of data error
- BIC command register overflow/underflow.

3.86 Except for BIC access error, the above are registered in the BSR. BIC access error occurs if the HA CPU/DMAC attempts to read the BIC FIFO when the BIC - HA CPU interface is disabled. This error is registered as bit 3 in the HASR.

3.87 The following SCSI bus errors generate a level 10 interrupt if the errors occur on bus 0 and a level 9 interrupt if the errors occur on bus 1:

- SCSI bus parity errors
- Selection timeout errors
- Bus phase error.

3.88 These errors are detected by the SPCs and the SPCs can mask these interrupts.

C. Parity Checking and Generation

BIC DDSBS Transfers

3.89 Parity is checked over each byte of the 32 INF leads on writes of the BIC command register and BIC control register, and on reads and writes of the BIC FIFOs. The results of these parity checks are saved as bits 5 - 8 of the BSR. These bits are set when a parity error occurs.

3.90 Parity is not checked on reads of the BSR.

3.91 The DDSBS can write data with bad parity to the BIC to check the parity checkers.

SRAM and FIFO Parity

3.92 Parity is checked over each byte when the HA CPU or DMAC reads the HA SRAM or the BIC FIFOs. Parity is generated for each byte when the HA CPU or DMAC writes the SRAM or FIFOs.

3.93 A parity error on the HA SRAM sets bit 2 in the HASR.

3.94 Parity errors on the BIC FIFOs set bits 12 and 13 of the BSR. Bit 12 signifies a parity error on the low half-word and bit 13 signifies an error on the high half-word.

3.95 The HA CPU can disable the BIC FIFO parity checks by setting bit 7 of the PIC control pulse points.

SCSI Bus Transfers

3.96 Parity is always generated by the SPCs when data is sent to the SCSI buses. Parity over data received from the SCSI buses is checked by the SPCs if parity checking is enabled. Parity checking is controlled by a bit in the SPC's SCTL register.

3.97 SCSI bus parity errors can be caused by the HA CPU to assist diagnostics. Inverted parity is sent to a SCSI bus when the SCSI bus send bad parity bit is set in the HASR. Inverted parity is received from a SCSI bus when the SCSI bus receive bad parity bit is set in the HASR.

4. Theory Of Operation

General

4.01 Data transmission between the 3B20D computer DSCH, and the DDSBS is via dual serial data streams with dedicated timing pulses. This interface is bidirectional with each DSCH serial data stream capable of handling 16 data and 2 parity bits (2 bytes) and a start code. Odd parity is observed for each byte. This transmission occurs over a 5-twisted-pair cable that is duplicated for each CU.

4.02 All actions within the SCSI DFC are controlled by the WE32100 microprocessor in the HA CPU that has direct access to the BIC via the HA microbus. The BIC interfaces the HA with the 3B20D computer CU via the DDSBS. Status and information transfers between the BIC and DDSBS occur under control of the 3B20D computer CU/DMAC via the PBI (Table B). The first four bits of each serial data stream (high and low data) contain a code that, when decoded (Figure 12), determines the DDSBS mode of operation. The first bit is always a 1 with a 1-out-of-3 code following the leading 1. Table M lists the commands transmitted (start code) by the CU and responses (return code) generated by the DDSBS.

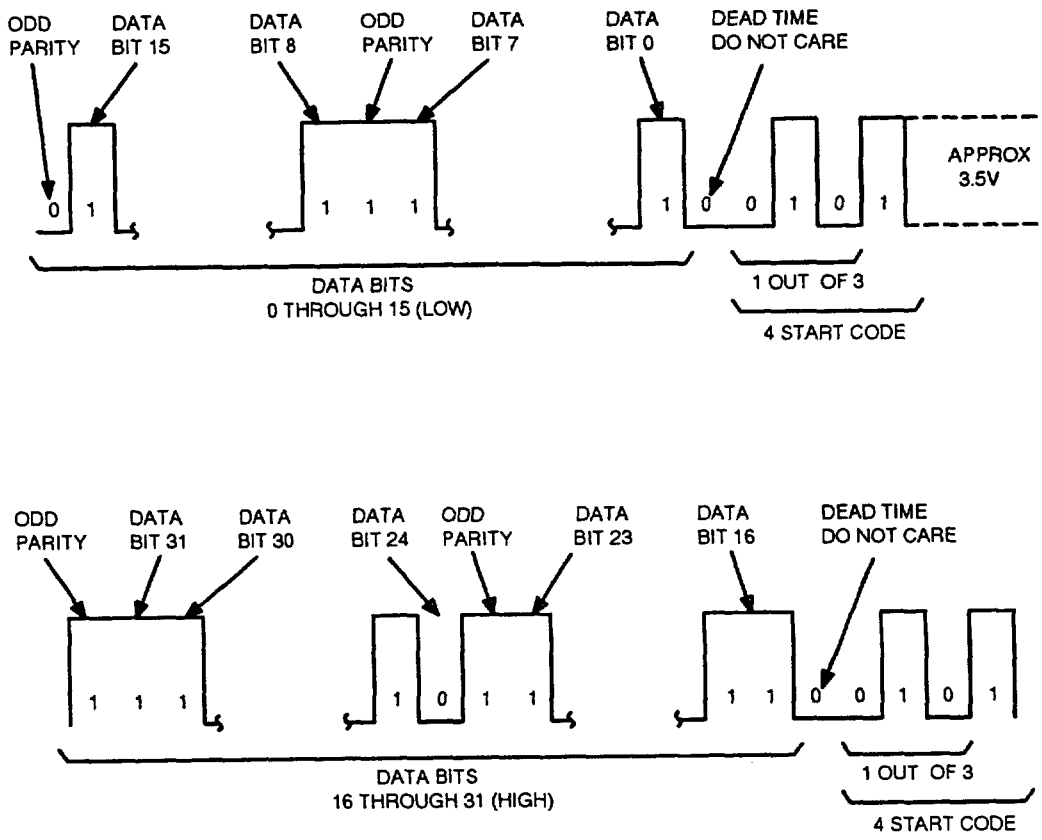


Figure 12. Direct Memory Access Controller Message Format

Table M. Dual Serial Channel Start and Return Codes

Type of Code	Nibble Position		Response
	High	Low	
Start code	0011	0011	Write data (word mode)
	0011	0101	Send device command
	0011	1001	Write data (block mode)
	0101	0011	Read data (word mode)
	0101	1001	Read data (block mode)
	0101	0101	Sense status
	1001	0011	End of transfer
Return code	0011	0011	All seems well (ASW)
	0011	0101	Device reported error
	0101	0011	Illegal computer command
	0101	0101	Illegal start code received

4.03 The HA CPU informs the 3B20D computer CU that service is required through three request mechanisms started by the HA writing bits in the BIC controller. The three request mechanisms are as follows.

(a) **DMA Setup Request:** A DMA setup request informs the 3B20D computer DMAC that the SCSI DFC wants to transfer control information to the 3B20D computer DMAC. This control information contains, among other things, the main store memory starting address for the data transfers that start when the SCSI DFC sends a transfer request, and the amount of data to be transferred.

(b) **DMA Transfer Request:** A DMA transfer request informs the 3B20D computer DMAC that the SCSI DFC wants to transfer one word at a time or a block of sixteen 32-bit words to and from main store memory. When the 3B20D computer DMAC services this request, it commands the DSCH to transfer the contents of the BIC FIFO memory to the DSCH via the serial data link between the DDSBS and DSCH.

(c) **Interrupt Request:** An interrupt request informs the CU that the SCSI DFC wants to communicate with the software disk driver.

4.04 The HA communicates with disk drives via two SCSI buses. Each SCSI bus will support up to four SCSI disk drives. The SCSI disk drives are controlled by a SCSI protocol converter (SPC) within the SCSI bus interface. The HA CPU together with

the SPC provide all control and data signals needed to execute the SCSI bus protocol. Each SCSI bus has a cable and each SCSI disk drive connects to the SCSI bus cable via a stub.

Disk Write/Disk Read

4.05 Each disk write or read operation that the 3B20D computer system wants the DFC to do is described to the DFC as a job request containing the following details:

- Device number (bus and disk drive)
- Operation (read or write)
- Starting main store (virtual) address
- Starting disk block address
- Number of data blocks to transfer (data block = 512 bytes)
- Job identification code.

4.06 The decoding of the disk block number into **cyl, head, sec** numbers is done entirely by the target controller of the disk drive.

4.07 The disk driver process (running on the 3B20D computer CU) places the appropriate disk command in a queue in the main store memory. If the SCSI DFC is not actively processing jobs, the disk driver program writes a "wakeup" command to the BIC command register to signify that there is work to do.

4.08 The SCSI DFC requests the 3B20D computer DMAC to send it the job queue from main store memory. To request a 3B20D computer DMAC transfer, the SCSI DFC places two words of DMAC set up information in the BIC FIFO, then asserts the DMAC setup request signal for each word. The 3B20D computer DMAC then reads the setup information from the FIFO.

4.09 The job queue data is transferred to the BIC FIFO when the HA CPU asserts a transfer request.

4.10 The 3B20D computer DMAC transfers the job queue to the BIC FIFO, and the HA DMAC transfers the queue from FIFO to SRAM.

4.11 The HA firmware/pumpcode (FW/PC) picks a job to process, and sends an SCSI command to one SPC. The SPC sends the command over the SCSI bus to the disk drive being read or written.

4.12 The disk drive disconnects from the bus and starts its seek.

4.13 If reading the disk, when the seek is complete and data has been read, the disk drive reconnects itself to the SPC and begins to transfer the data into the FIFO.

4.14 The HA FW/PC requests the 3B20D computer DMAC (using the steps described above) to transfer the disk data to or from the main store memory.

4.15 If writing the disk, the data is now transferred from the FIFO to the disk over the SCSI bus.

4.16 When the data transfer is complete, the SCSI DFC puts a job response in the FIFO and uses the 3B20D computer DMAC to send it to the response queue in the main store memory.

4.17 The HA FW/PC asserts the 3B20D computer interrupt request to signify to the disk driver program that it has completed the disk job.

5. SCSI Disk Power System

5.01 Power for the SCSI DFC is provided by the following elements.

- Power supply (410AB circuit pack)
- Power switch (TN6B circuit pack).

5.02 The two power supplies are provided to the multilayer backplane serving the MAS, I/O, and DFC unit. Current programming provides backplane protection.

5.03 The power switch contains a monitor circuit for checking the power supply. If the power supply fails, a major alarm occurs and the SCSI DFC is shut down.

Power

5.04 The SCSI DFC requires +5 V DC for operation. The +5 V DC is supplied by a power converter (–48 V DC to ±5 V DC and ±12 V DC) located adjacent to and in the same backplane unit as the DFC. Backplane protection is provided by current programming instead of fuses. With current programming, each circuit pack in the SCSI DFC has a resistor on it whose value is related to the amount of current drawn by that circuit pack under normal conditions. The current programming resistors of all the SCSI DFC circuit packs supplied by the power converter are paralleled together to signify to the power converter how much current should be supplied. If a high-current fault occurs assocaited with either the circuit pack or backplane, the power converter will shut down and an alarm signal will be generated.

5.05 The power control circuit controls the application of a +5 V DC power to the host adapter circuit packs and the DDSBS. The power control circuit also provides power status and alarm information to system software through a scanner/distributor interface. The power control interface is provided by manual switches and indicator light-emitting diodes (LEDs) located on the faceplate of the power control circuit (Figure 13).

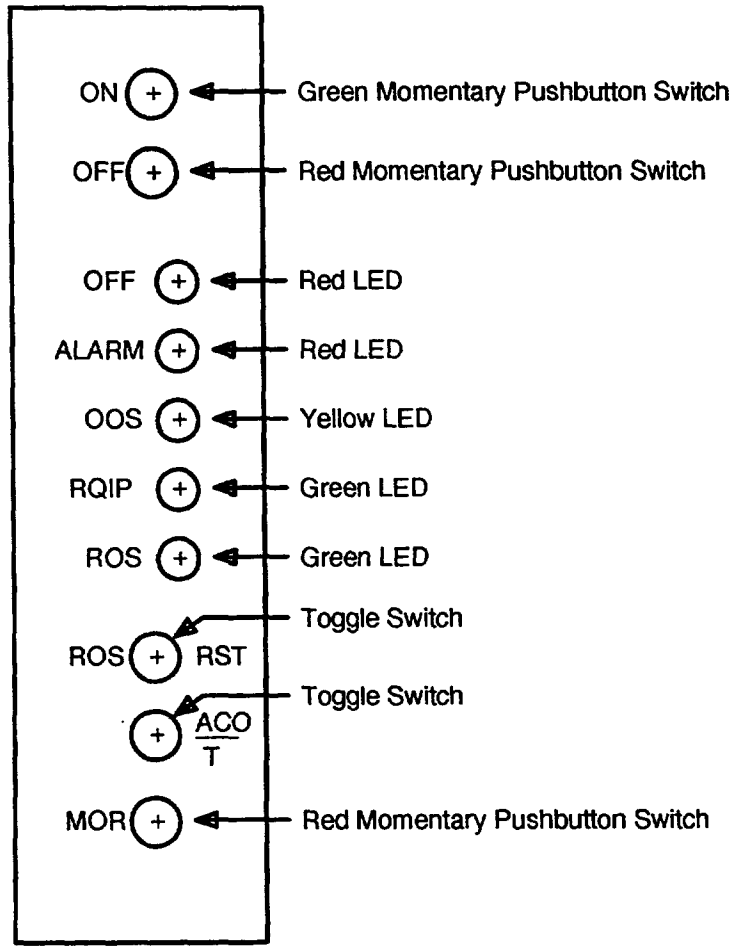


Figure 13. Disk File Controller Power Control Circuit Faceplate

A. Power Switches

5.06 The power switches provide control (application and removal) for the SCSI DFC power. The 3-phased start signals are provided by the power control circuit to control the application sequence of logic power and I/O bus power. The following functions may be performed by the maintenance personnel.

(a) Apply or remove power

(b) Start a system request to remove from service or restore to service the associated unit

(c) Test indicator lights on the power switch

(d) Retire a major alarm generated at the associated unit.

5.07 Five switches provide power control. These switches are located on the front power panel of the power control circuit and are labeled ON, OFF, ROS/RST (request out of service/restore), ACO/T (alarm cutoff/test), and MOR (manual override). The ON, OFF, and MOR switches are momentary pushbutton switches, and the ROS/RST and ACO/T switches are 2-position latching switches. Input voltage requirements are –48 V DC from the office supply and +5 V DC from the power converter controlled by the power control circuit.

5.08 The power control circuit switches are described as follows.

(a) **ON:** Momentarily pressing the ON switch when the ACO/T switch is not in its alarm cutoff state starts the power-up sequence. Pressing the ON switch when the ACO/T switch is in its alarm cutoff state or when frame power is up causes no change in the state of the power control circuit.

(b) **OFF:** Momentarily pressing the OFF switch when the unit is in its out-of-service state starts the power-down sequence. Pressing the OFF switch when the unit is in service or when power is off causes no change in the state of the power control circuit.

(c) **ROS/RST:** Pressing the ROS/RST switch to the ROS position requests that the unit be taken out of service via the scan point SCX and lights the ROS LED. Pressing the ROS/RST switch to the RST position requests that the unit be restored to service.

(d) **ACO/T:** Operating the ACO/T switch to the ACO position tests all lamps on the power control circuit, silences the office major alarm originated at the power control circuit, and permits the ALM LED to extinguish (when the ACO/T switch is returned to its normal position).

(e) **MOR:** Simultaneously pressing the OFF and MOR switches defeats the interlock between the OFF switch and unit out-of-service state and starts the power-down sequence.

B. Power Control Indicators

5.09 Five indicator lights on the front of the power control circuit signify the state of the unit being controlled. These lights are OFF, ALM (alarm), OOS (out of service), RQIP (request in progress), and ROS (request out of service). The five indicators, described as follows, are 549-type LEDs.

(a) **OFF:** A red LED labeled OFF is lighted when the unit is in its power-off state and is extinguished when the unit is in its power-on state.

(b) **ALM:** A red LED labeled ALM is lighted to signify the presence of power-related faults.

(c) **OOS:** A yellow LED labeled OOS is system activated via the OOS signal distributor point when the unit is marked out of service.

(d) **RQIP:** A green LED labeled RQIP is lighted to signify that the system has received a request to take the unit out of service or to restore it to service. This lamp, is system-activated via the RQIP signal distributor point and flashes to signify that the request has been denied.

(e) **ROS:** A green LED labeled ROS is lighted when the ROS/RST switch is in its ROS state.

C. Scan, Alarm, and Signal Distributor Points

5.10 Two scan points (SCX and SCY), two alarm points (MJ and PA), and two signal distributor points (OOS and RQIP) are provided. Each scan and alarm point consists of an isolated metallic contact. The active one state is defined as a resistance of less than 200 megohms. The inactive zero state is defined as an open circuit. Each distributor point consists of an optoisolator input diode.

Scan and Alarm Points

5.11 The scan and alarm point states are summarized in Table N. For automatic power-off alarms, the MJ alarm contact closes and remains closed until the ACO/T switch is pressed. When power is left up in the presence of a major alarm fault, the MJ alarm point remains closed until either the fault is removed (PA alarm point also goes inactive) or the ACO/T switch is pressed (PA alarm point remains active).

Table N. DFC Power Control Scan and Alarm Point States

Condition	Scan Point		Alarm Point	
	SCX	SCY	MJ	PA
Normal in service	0	0	0	0
Request out of service	1	0	0	0
Manual power off	1	1	0	0
Automatic power off	1	1	1	0
Power up with major fault present	0	1	1	1
Power up with minor fault present	0	1	0	1

Signal Distributor Points

5.12 The active one state of the RQIP signal distributor point signifies a system software acknowledgment that a request for removal from service or restoral to service of the associated unit has been made. If the request is granted, the RQIP signal distributor point will become inactive (zero state). If it is denied, the RQIP signal distributor point will intermittently flash under system control. The OOS signal distributor point becomes active when the unit has been taken out of service. The RQIP and OOS LEDs provide a visual indication of the state of the RQIP and OOS signal distributor points, respectively. The signal distributor point states are summarized in Table O.

Table O. DFC Power Control Signal Distributor Point States

Condition	SD RQIP	Point OOS
Normal in service	0	0
Removal from service or restoral to service requested with disposition pending	1	0
Request denied	FLASH	0
Diagnostic failure after a restore-to-service request	FLASH	0
System grants out-of-service request	0	1

D. Power-Up Sequence

5.13 Power-up is started by momentarily pressing the ON switch. Control circuitry ensures that frame power is supplied in the proper sequence via three start signals and an initialization phase. In the power-off state, the initialization circuit, that starts the power-up sequence, is powered from a fused –48 V DC source through a normally open ON switch (momentary contact). Initialization signals enable +5 V DC frame converters that power TTL sequence circuitry and initialize power control and alarm circuitry. This allows the power control circuit to be inserted with –48 V DC present without enabling frame converters until the ON switch is depressed. The OFF LED is lighted in the power-off state and does not extinguish until the power-up sequence is complete.

E. Power-Down Sequence

Normal Power Down

5.14 To prevent the inadvertent removal of frame power, the OFF switch (momentary contact) is interlocked with a system-granted out-of-service signal. Pressing the OFF switch causes no change in state of the circuit pack unless the out-of-service signal distributor point is active. If that signal is active, case frame power is sequentially removed. The OFF LED remains extinguished until the power-down sequence is

complete.

Emergency Power Down

5.15 Simultaneously pressing the OFF and MOR switches sequentially removes frame power and provides an emergency manual power control if needed.

5.16 Power should be removed before replacing any circuit pack.

SCSI Bus Power Control

A. Bus Terminator Power

5.17 The HA provides 5 V DC power for bus termination on the TERMPWR signal on each SCSI bus. This is used by resistor networks that plug into each end of the SCSI buses. To protect the HA against electrical faults, the current drawn through the TERMPWR signal on each SCSI bus is limited. Once normal current draw returns, terminator power is restored.

B. Bus Isolation

5.18 Each SCSI bus can be independently isolated from the HA. Bus isolation requires two steps. First, the HA FW/PC stops issuing commands to the SCSI devices and waits for any pending commands to complete. Next, the HA FW/PC disables its SCSI bus drivers by clearing the SCSI bus enable bit in the HA status register.

6. Maintenance

6.01 Manual and routine maintenance is performed using 254-302-811 *AT&T 3B20D Computers Model 2 and Model 3 Common System Routine Tasks* to guide and direct step-by-step procedures.

7. Glossary Of Terms And Acronyms

7.01 A glossary of terms and acronyms is provided to aid in the understanding of this section.

Terms

Power Converter: Converts –48 V DC power to +5 V DC logic power for the SCSI DFC circuitry.

Buffer: A storage device used to compensate for a difference in the rate of flow of information or time of occurrence of events when transmitting from one device to another. This storage device is normally a register.

Bus: One or more conductors for transmitting from any of several sources to any of several destinations.

Bus Interface Circuit: Buffers data, commands, and status information between the DDSBS and the host adapter.

Central Control: Control section of the control unit. It consists of the microcontroller, data manipulation unit, special registers, store interface circuits, cache store unit, microstore, main store update, maintenance channel, microlevel test set interface, utility interface, and emergency action interface.

Control Unit: That part of a computer that is switched on-line or off-line as a unit. It consists of the CC, main store memory, DMA input/output channels, and associated power elements.

Direct Memory Access: This system function provides main store access control for peripheral devices without requiring direct control from the CC.

Direct Memory Access Controller: Control circuitry for the DMA.

Disk File Controller Power Control: Contains a monitor circuit for checking the power converter.

Dual Serial Channel: Provides a 16- or 32-bit AC interface to input-output devices and uses two serial signal paths in each direction.

Duplex Dual Serial Bus Selector: Provides interface between two DSCHs and an associated peripheral device.

Emergency Action Interface: System component that provides a manual emergency control interface to the computer.

Flag: Bit positions indicating that some task needs to be done.

Flip-Flop: A device capable of assuming two stable states (set or clear) thereby storing a bit of information. It remains in either state until a signal changes it to the other state.

Interrupt: A signal generated by a device to notify the CC that the device requires attention.

Mask: A bit pattern used to enable or disable specific bits.

Microbus: The bus that connects the HA CPU, HA DMAC, and memory on the HA. Also connects SPCs and BIC registers and FIFOs.

Microprocessor: A small, low-priced, special-purpose processor used to do a specific function; for example, a peripheral controller.

Off-Line: A computer is off-line when it is not in the active state and is not controlling the system. The off-line computer is the unit that is not in active control of system configuration and execution but may be actively (executing diagnostics, for example) doing off-line functions.

On-Line: A computer is on-line if it is in the active state and can execute code. More specifically, for a 3B20D Model computer, the on-line computer is in active control of system configuration and execution; its mate processor, the off-line processor, may be executing diagnostics but it is not in control.

Physical Address: Hardware memory address.

Peripheral Bus Interface: A group of leads that interconnect the DDSBS and associated peripheral devices.

Shift Register: A digital storage circuit that shifts information from one flip-flop of a chain to the adjacent flip-flop on application of each clock pulse.

Word: A CC word consists of 32 bits (plus 4 parity bits) that correspond to the width of the data paths within the CC and to the width of most registers within the CC. A word is divided into four 8-bit bytes with a parity bit associated with each byte.

Acronyms

7.02 The following acronyms are used within this section.

ACRONYMS	WORDS
ASW	All Seems Well
BIC	Bus Interface Circuit
BSR	BIC Status Register
CC	Central Control
CCIO	Central Control Input/Output
CU	Control Unit
DDSBS	Duplex Dual Serial Bus Selector
DFC	Disk File Controller
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DSCH	Dual Serial Channel
DUP	Disk Unit Package

EOT	End Of Transfer
EPROM	Erasable Programmable Read Only Memory
FIFO	First-In-First-Out (Buffer)
HA	Host Adapter
HASR	Host Adapter Status Register
IC	Integrated Circuit
LED	Light-Emitting Diode
MAS	Main Store
MTP	Memory-To-Peripheral
NMI	Nonmaskable Interrupt
OOS	Out-Of-Service
PBI	Peripheral Bus Interface
PIC	Peripheral Interface Controller
PIO	Programmed Input/Output
PROM	Programmable Read-Only Memory
PTM	Peripheral-To-Memory
RAM	Random-Access Memory
ROM	Read-Only Memory
ROS	Request Out Of Service
RQIP	Request In Progress
SCSI	Small Computer System Interface
SCSI DFC	SCSI Disk File Controller
SMD	Storage Module Drive
SPC	SCSI Protocol Controller
SRAM	Static Random Access Memory
SST	Sense Status
TTL	Transistor-Transistor Logic
WPR	Write Protect Register

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