A1 DIGITAL DATA TRANSMISSION SYSTEM USING FOUR-PHASE DATA SETS GENERAL DESCRIPTION

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1. GENERAL

1.01 This section describes the major components and over-all operation of the A1 Digital Data Transmission System equipped with Four-Phase Data Sets (A1 DDS-4PH). Initial Line-Up and Testing Procedures are covered in Section 314-550-305, Periodic Routine Testing in Section 314-500-305, and Over-all Tests and Trouble Location in Section 314-500-505. Many components and testing circuits of the four-phase system are identical with those of the original A1 system and are covered in detail in existing sections.

1.02 The A1 DDS-4PH system has been developed for use in the SAGE air defense system for transmission of data, at a 1300 bit-per-second rate, from the data generating equipment at radar sites or other locations to data processing equipment at computer centers, and to transmit processed data from these computer centers to other data using locations.

1.03 The system consists essentially of a data transmitter (DDT-4PH) connected over a data transmission line to a data receiver (DDR-4PH), and terminal loop facilities connecting the data generating equipment to the DDT-4PH and the DDR-4PH to the data using equipment. The system is so arranged that the data generating equipment and data using equipment may be in the same location or separated by several miles from the data transmitter and receiver to which they are connected.

1.04 Either single or dual transmitting systems may be used, depending on the operational importance of the particular link. A single system usually consists of a single transmitter connected to a single receiver. Where dual service is specified, two transmitters are used at the data source location, each connected over separate transmission lines (preferably on separate routes) to two receivers at the data using location. Data is supplied at the transmitting terminal to both transmitters at all times. Automatic trouble detection and automatic transfer features are provided at the receiving location between the regular and alternate service.

1.05 The system may be provided as a two-point service, a single transmitter location feeding a single receiver location. Bridging arrangements, such as one transmitter location feeding more than one receiver location, may be used where required. Other combinations of transmitters and receivers are also possible for special applications.

1.06 When access to the AUTOVON Switched Network is required, data sets will terminate as specially conditioned 4-wire subscriber lines.

1.07 These 4-wire subscriber lines will then route via a Dial Restoration Panel (DRP) or an Alternate Dial and Transfer Arrangement which has the capability to restore data facilities using suitable AUTOVON PBX access lines.

2. OVER-ALL OPERATION

2.01 The input data signal is fed from the data generating equipment to the data transmitter (DDT-4PH) over three balanced pairs called dipulse loops. These loops carry separately the three components of the signal; START, DATA, and TIMING information. Transmission and resistance considerations limit the length of these dipulse loops to about five miles.

2.02 The START signal consists of a single cycle of the 1300-cycle sine wave, called a dipulse, occurring once at the beginning of each data "word". In the SAGE system, the word may be either 52, 78, 92, or 326 bits long.

2.03 The DATA signal consists of a variable combination of marks and spaces. A mark consists of a single dipulse of the TIMING wave and is in phase with it. A space consists of a null or no signal condition for a time period of one cycle. In order to avoid possible interference between the START and DATA signals, only spaces are transmitted on the DATA loop during a five bit period centered around the mark signal on the START loop.

2.04 The TIMING signal is a continuous sine wave of 1300 cycles and an amplitude of 2.2 ± 0.1 volts peak-to-peak. Frequency accuracy is held to about ± .01 per cent.

2.05 The three signal components are fed to the data transmitter (DDT-4PH) which transforms the signal to a form suitable for transmission over the data line. The DDT-4PH set is so designed as to be a direct physical replacement for the older A1 DDT used on the SAGE system (the DDR-4PH is similarly a direct physical replacement for the older A1 receiver).

2.06 The transmitter, which has a serial capability of 2600 bits per second, is divided and operated as two parallel 1300 bps channels known as Channels A and B. Information from the START and DATA inputs are combined and transmitted alternately over the two channels. The TIMING signal is not transmitted over the data line.

2.07 The SAGE four-phase data sets use a form of phase shift modulation, in which dibits are transmitted by shifting the carrier phase a fixed amount with respect to the phase of the carrier transmitted for the previous dibit, rather than by comparison with a fixed or constant phase reference.

2.08 The dibits transmitted are formed by combining the information on the START and DATA inputs. Four types of dibit combinations are possible with a predetermined amount of phase shift for each type. Only three of these types are used in the SAGE system. By representing a dipulse (mark) on either START or DATA inputs by a "1" and the absence of the dibit (space) by a "0", the four possible types of line information may be described as follows:

00 — Condition of a space (absence of dipulse) on both START and DATA inputs. Will be read by the data receiver as a ***data space.***

01 — Condition of a space on the DATA input and a mark on the START input. Read by the data receiver as a ***start pulse.***

10 — Condition of a mark on the DATA input and a space on the START input. This will be read by the receiver as a ***data mark.***

11 — Condition of a mark on both DATA and START inputs. This condition should never occur, since start and data dipulses are never transmitted simultaneously.

2.09 The dibits are transmitted alternately over Channels A and B of the data transmitter (Paragraph 2.06). As the form of each successive dibit is recognized by the data transmitter logic circuit, the transmitter sets up the phase of the 1950-cycle carrier for the next dibit and prepares to transmit the succeeding dibit over the opposite channel. The amount of this phase shift is always the same for each dibit form and is always referred to the phase of the previously transmitted dibit. The amount of this phase shift used in the SAGE system is as follows:

11-type dibit = 45°
10-type dibit = 135°
00-type dibit = 225°
01-type dibit = 315°

As an example, if a group of data marks were transmitted within a word, each "10"-type dibit would be displaced 135° in carrier phase from the dibit immediately preceding it and transmitted alternately over the line from the two 1300 bps Channels A and B.

2.10 The composite data signal from the data transmitter (DDT-4PH) is fed over the data transmission line to the data receiver (DDR-

4PH). The transmitter carrier level output should be −2.0 ± 2.0 dbm measured at the DDT-4PH set output when terminated. This level is reduced to −10 dbm at the zero level point of the line facility. The input to the data receiver (DDR-4PH) is a nominal −18 dbm.

2.11 The data receiver (DDR-4PH) is a direct physical replacement for the older A1 DDR with one exception. The external Trouble Detector Circuit used with the original A1 system is no longer required and is replaced by trouble detection circuitry included internally in the DDR-4PH set. A minor wiring modification, consisting of a new lead from the internal trouble detector of the receiver to the A1 Transfer and Control Circuit, is required.

2.12 The data receiver detects the line signal and regenerates a composite data signal identical to that from the data generating equipment. The START, DATA, and TIMING components are fed over separate dipulse loops to the data using equipment. The 600-ohm balanced dipulse outputs of the receiver are adjusted to provide a nominal level of 0 dbm (2.2 volts peak-to-peak) into a 600-ohm resistive test termination. Where the data receiver is in the same location as the data using equipment, the level fed to the customer's equipment should be at least −1.0 dbm (2.0 volts peak-to-peak). Where the loss between the receiver and the data using equipment exceeds 1.0 db, the customer's equipment can be adjusted to receive a nominal level of −10 dbm (0.7 volts peak-to-peak), pads should be provided in the dipulse loops to build out the line loss to 10 db. In some cases, the data using equipment is only arranged for low-level input (−10 dbm) and pads will be required on all loops.

3. SYSTEM COMPONENTS AND TESTING CIRCUITS

3.01 The A1 system using four-phase data sets is essentially identical to the original A1 system except for the transmitting and receiving data sets, the form of line signal used, and the transmission requirements of the line facility. The system consists of certain basic line units, circuits connected permanently to the data circuit for line supervision, and certain testing circuits used for both "in service" and "out-of-service" testing.

3.02 ***Transmitter:*** The four-phase digital data transmitter receives the START, DATA, and TIMING components of the data signal from the customer's data generating equipment over three 600-ohm balanced input lines. The transmitter transforms these inputs into a composite line signal using a 1950-cycle carrier, as described in Part 2 of this section, and feeds this signal to the data line. In the dual circuit arrangement, two transmitters receive data in parallel thru bridging resistors from the three input loops and transmit to both the regular and alternate data lines simultaneously. A detailed description of the transmitter is covered in Section 314-501-105. Maintenance Tests are covered in Section 314-501-305 and Performance Requirements in Section AA643.013. Drawing SD-1G184-01 covers the circuit details.

3.03 ***Receiver:*** The four-phase digital data receiver accepts the signal from the data line, demodulates the signal, separates the START and DATA components, and originates a new TIMING component. These three components are fed over separate 600-ohm balanced loops to the data using equipment. Synchronization for the TIMING output is obtained from an internal oscillator in the receiver, the frequency of which is constantly corrected by crossing pulses generated by 0 to 1 or 1 to 0 transitions of the line signal. Trouble detection circuitry is included in the receiver to actuate the A1 Transfer and Control Circuit. Three types of trouble are detected and will cause operation of the Transfer and Control Circuit. These are:

(a) Loss of carrier or loss of continuity thru the plug-in card circuits of the receiver.

(b) Loss of crossing pulses. If proper START pulses are received, even though no message bits are transmitted, sufficient crossings will be received to prevent operation.

(c) Excess noise on the data line. If sufficient noise is received, the trouble detector will operate.

A detailed description of the receiver is contained in Section 314-502-105. Maintenance Tests are covered in Section 314-502-305 and Performance Requirements in Section AA643.014. Circuit details are covered by Drawing SD-1G185-01.

3.04 ***Transfer and Control Circuit:*** The transfer and control circuit receives the indication of trouble from the trouble detection circuitry in the data receiver and transfers the service to bring the alternate channel and DDR to the "in-use" condition and the regular channel to "stand-by". Associated lamps and trouble alarms are operated. If the trouble condition disappears from the regular channel, the transfer relays will not restore the service to normal until manually operated, unless trouble should be indicated on the alternate channel. A trouble indication on a channel in the stand-by condition will also give alarm indications but, of course, no transfer would be made. Operation of the circuit and the lamp indications for different circuit conditions are covered by Sections 314-500-100, 314-504-100, and Drawing SD-1G004-01.

3.05 ***Word Generator Circuit:*** The word generator (WG) is used in the testing of transmitters, receivers, and associated line equipment and is used as a source of SAGE-type data signals. The output of the word generator consists of the three basic signal components of TIMING sine wave, START dipulses, and DATA dipulses. The word length, that is, the number of pulses between start signals, may be varied from 16 to 256 bits per word. Either a 1300-cycle or 1600-cycle bit rate may be used. The 1300-cycle setting should be used with four-phase data sets. Operation of the circuit is covered by Section 314-505-100 and Drawing SD-1G005-01 or SD-1G097-01.

3.06 ***Matching and Error Counter Circuit (M and EC):*** The matching and error counter circuit is a test circuit used to determine differences between transmitted and received data over a data circuit equipped with a DDT and DDR at transmitting and receiving ends. It may also be used in the testing of the transmitters and receivers themselves by operating the two units back to back at the same location with no data line facilities between. In the usual case the matching and error counter circuit is used in conjunction with two word generators, one at the transmitting end and one at the receiving end of the data line. The two word generators are adjusted for the same bit rate (1300), word length, and data content of a word and the M and EC circuit is used to compare the signal received over the data line with that from the local word generator at the receiving location. The number of errors or differences in a given test period are recorded by counter tubes and a message register in the M and EC circuit. Operation of the circuit is covered by Section 314-506-100 and Drawing SD-1G006-01.

3.07 ***Parity Check Circuit:*** The parity check circuit is a testing or monitoring circuit used to estimate and record the number of errors transmitted over a working data line. The circuit may be used to terminate a line from the receiver under test but, as normally used, is bridged on a working line at or near the receiver location.

3.08 In normal operation the data transmitting terminal is preset to transmit data words of either even or odd parity, that is, each word is made up of an even or odd number of data bits. The parity check circuit is then set for the type parity being transmitted. When so operating, an omitted pulse or an added false pulse will reverse the correct parity of a received word and will be recorded as an error. Since the error detection depends on only an odd-to-even or even-to-odd reversal, only an odd number of bit errors per word will be recorded as word errors and, in those cases where word errors occur in closely spaced groups, the actual number of errors recorded may be considerably less than those actually occurring. The recorded total will, however, give an indication of the severity of the existing trouble. Details of the operation of the parity check circuits are covered by Section 314-507-100 and Drawing SD-1G007.

3.09 ***Jack and Connector Circuit:*** The jack and connector circuit provides terminations for the various units of the A1 system and is used for testing and adjusting of transmitters, receivers, and other components of the system. The circuit is installed in two forms known as the test relay jack and connector circuit and a simplified form, the test jack and connector circuit. In the test relay jack and connector circuit, relays are provided to switch units to be tested with spare test units. A spare transmitter and receiver for use in testing are usually supplied as part of the circuit.

In the simplified jack and connector circuit, the relays and spare transmitter and receiver units are omitted and jack terminations only are provided. Details of the jack and connector circuits are covered by Section 314-509-100 and Drawing SD-1G009-01.

3.10 ***Miscellaneous Test Circuit:*** This circuit provides an adjustable source of in-band noise for use in testing various components of the system. It is usually used in conjunction with jack and connector circuits in the testing of trouble detector circuits. Details of the miscellaneous test circuit are covered by Section 314-509-100 and Drawing SD-1G009-01.

4. SIGNAL REQUIREMENTS

4.01 The signal generated by the data source consists of three basic parts: the TIMING, START, and DATA components. The TIMING signal consists of a sine wave of a frequency equal to the bit rate, that is, a frequency of 1300 cycles. The START and DATA components consist of dipulses or single cycles of a sine wave of the same frequency. The presence of a dipulse in the signal corresponds to a "mark" condition and the absence of a dipulse to a "space" condition.

4.02 The required amplitude of the TIMING signal and of the START and DATA dipulses should be nominally 2.2 volts peak-to-peak (one milliwatt or 0 dbm into 600 ohms). (See Fig. 1.) This amplitude should not vary by more than ±10.0 per cent or approximately ±0.8 db over a long period. The maximum amplitude of any harmonic in the signal should not exceed 5.0 per cent.

4.03 The frequency of the signal should meet two different requirements. The permissible long time variation over a period of days or months should not exceed ±0.01 per cent. The signal may, however, have a short time variation from cycle-to-cycle or pulse-to-pulse. This variation in cycle-to-cycle frequency or phase shift is known as phase jitter. This jitter should not exceed ±2.0 per cent of the wave period at the crossover points. These requirements are illustrated in Fig. 1.

4.04 The ideal mark signal consists of one complete cycle of the sine wave, starting at the zero amplitude point and terminating again at zero with no carry-over or following transient. An ideal space signal would be a complete absence of signal. In a practical signal, there may be some variation in the gating time or the beginning and end of the mark pulse (Fig. 1). Also, some transients may occur immediately following a mark signal. The space signal may include some noise energy or may contain some transient energy from a preceding mark. The peak interference in a space signal should not exceed 5.0 per cent of the peak amplitude of the mark signal. However, since the signal will be sampled near its center, the interference during the first and last 10 per cent of the space signal may exceed the above 5.0 per cent limit provided the detection level of the mark signal is not exceeded at any time. This detection level may be assumed to be approximately a third of the peak mark level.

4.05 Since the timing, start, and data components of the signal usually will have a common source, there should be little phase displacement or independent phase jitter between the components. As measured at crossover points, this difference should not exceed ±1.0 per cent of one wave period.

4.06 The above signal components, when received from the customer equipment, are reduced in level by input pads to the transmitter, the usual level into the DDT-4PH being −10.0 dbm with a tolerance of ±0.5 db.

4.07 The level of the signal applied to the data line from the four-phase transmitter should be adjusted to be −10.0 dbm at the 0← TLP of the circuit (0.7 volts peak-to-peak in a← 600-ohm circuit).

4.08 The received line signal is separated by the receiver into the three basic components (the start signal, data signal, and the recreated timing signal) and transmitted to the customer over three 600-ohm lines.

4.09 The output level from the data receiver for all three components is adjusted at the receiver output to a level 2.2 volts peak-to-peak (0 dbm into the 600-ohm line). Where the

data using equipment and the receiver are in the same location, this should result in a minimum level of about 2.0 volts peak-to-peak (−1.0 dbm) at the data using equipment. In those cases where the customer's equipment is at a greater distance from the receiver (DDR-4PH), the data using equipment should be adjusted to accept a level of 0.7 volt peak-to-peak (−10 dbm). In this case, pads should be provided to give an over-all 10 db loss from the data receiver to the data using equipment. In some cases, only low-level type customer equipment is provided and pads may be used even when close to the DDR-4PH.

5. LINE REQUIREMENTS

5.01 In general, facilities suitable for Schedule 4A data service will be satisfactory for SAGE data circuits using the four-phase sets. The general over-all requirements for the point-to-point line facilities are covered below. Transmission requirements of 4-wire subscriber lines into AUTOVON are discussed in Sections AB27.401.3 and AB23.053.3.

5.02 The ***1000-cycle net loss*** of the over-all data channel (DDT to DDR) is usually engineered for an 8 ± 1.0 db loss between 600-ohm terminations. ***Seasonal variations*** should be no greater than ±4.0 db. ***Short time variations,*** that is, swings in line loss in about four seconds or less, should be no greater than ±3.0 db.

5.03 The maximum loss deviation with frequency of the over-all data channel from the actual measured 1000-cycle loss should not exceed the following limits:

300- to 1000-cycle band	−2 to +6 db
1001- to 2400-cycle band	−1 to +3 db
2401- to 2700-cycle band	−2 to +6 db

If equalization is required to meet the aboye limits, the 1000-cycle loss of the equalizer should be included in the 8 db limit of Paragraph 5.02.

5.04 The ***envelope delay characteristic*** of the over-all channel between data sets should be such that the difference in delay of any two frequencies between 1000 and 2400 cycles should not be more than 1000 microseconds. When 200-type, or equivalent, equalizers are used to meet this limit, it is not desirable to use more equalizer sections than necessary to meet this limit. Overequalization may result in ripples in the delay characteristic in the middle of the frequency band. Computations of the expected residual delay distortion or delay measurements over the above band should be made.

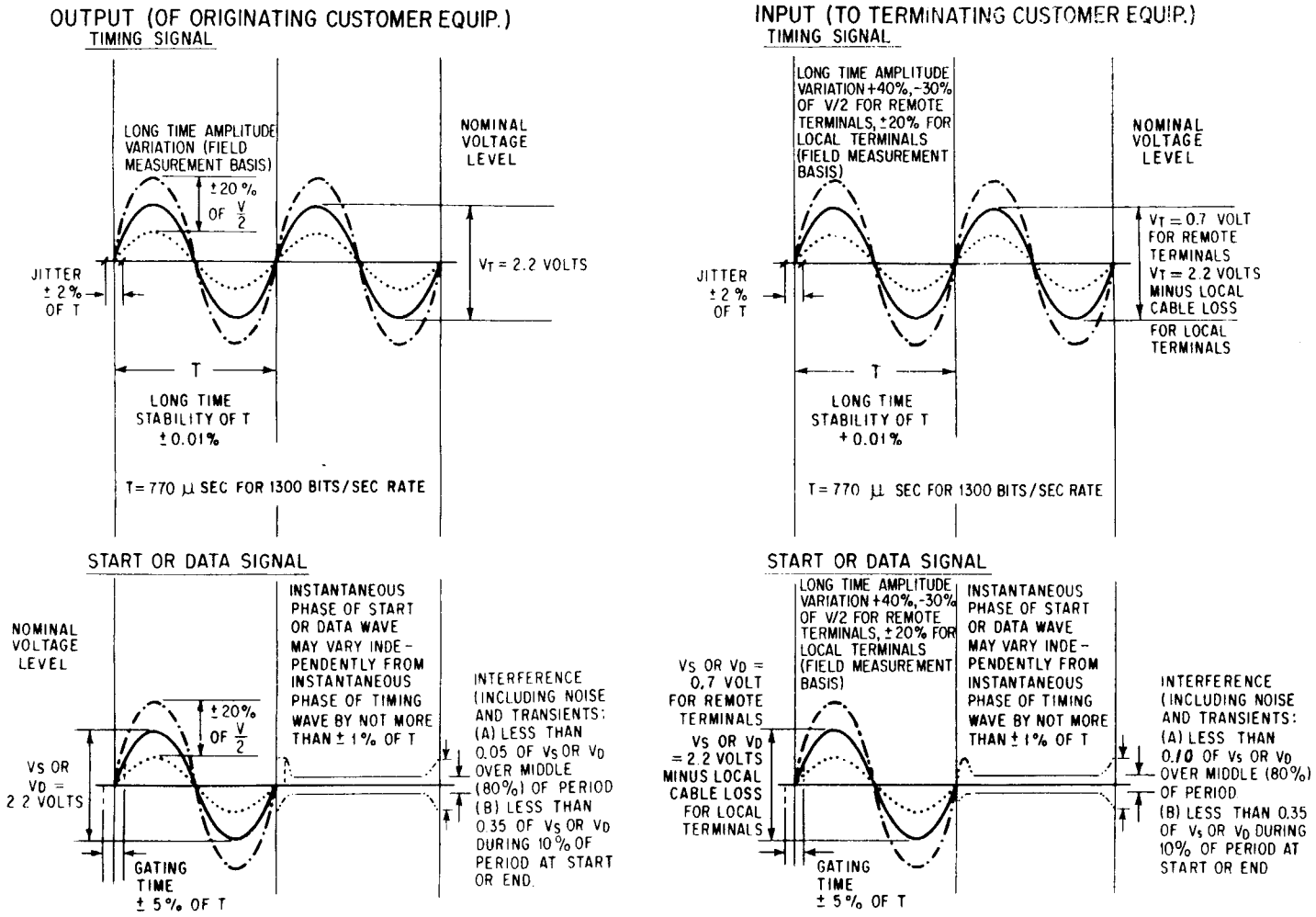
5.05 The maximum permissible noise on four-phase data channels is essentially the same as that for other Schedule 4A data services. When N, ON, or O carrier facilities are used, compandored channel units should be employed whenever possible, to give the best possible signal-to-noise condition. Test limits for both steady and impulse noise are covered in Sections 314-550-305 and 314-500-305.

6. REFERENCE SECTIONS

AA330.001	Signaling Equipment Units and Associated Equipment for Receiving and Transmitting Digital Data Signals
AA330.002	A1 Digital Data Patching and Testboard Equipment
AA643.013- and .014	Performance Requirements for Four-Phase DDT and DDR
AB27.400.5	Estimate of Impulse Noise on N1 and ON1 Carrier Channels
AB27.400.6	Estimate of Static Noise on Open-Wire Circuits
→AB27.400.7	Dial Restoration Panel for SAGE — Transmission Engineering Considerations
AB27.401.1	Data Circuits — Delay Equalization
AB27.401.20	Absolute Delay Equalization for Ground/Air Data Links
AB27.401.3	A1 DDS — Four-Phase Sets — Genl. Eng. Considerations
314-500-305	Periodic Tests

314-505-501	Word Generator Circuit
314-506-501	Matching and Error Counting Circuit
314-507-501	Parity Check Circuit
314-550-305	Initial Testing and Line-up of SAGE Data Circuits
314-500-505	Over-all Tests and Trouble Location
314-850-500	Testing of Pairs for Data Circuits
100-658-100	KS-16305 Oscilloscope
100-656-100	Type 535 Tektronix Oscilloscope
103-111-100 (E40.673.1)	Delay Measuring System — KS-15877 (Transmitter), KS-15878 (Receiver)
314-410-500	Private Line Data — Over-all Test Circuits and Requirements
314-500-105	SAGE Data Systems — General Considerations and Description
314-551-100 314-552-100 314-553-100	Radar, Ground-Ground, Ground-Air Data Systems
314-504-100	Description of Transfer and Control Circuit
314-508-100	Description of Jack and Connector Circuit
314-510-100	Description of Data Testboard and Associated Circuits
314-501-105	Description of Four-Phase DDT
314-501-305	Maintenance Tests for Four-Phase DDT
314-502-105	Description of Four-Phase DDR
314-502-305	Maintenance Tests for Four-Phase DDR
103-620-100	6A Impulse Counter
103-611-100	3A Noise Measuring Set

DATA SYSTEM SIGNALS



NOMINAL VOLTAGE LEVELS ARE FOR REFERENCE CONDITION WHERE MEASUREMENT IS MADE INTO 600-OHM BALANCED RESISTIVE TERMINATION. WHERE VOLTAGES OF THREE SIGNALS ARE NOT SEPARATELY ADJUSTABLE, SPECIFIED LEVEL APPLIES TO LOWEST. ALLOWANCES FOR LONG TIME AMPLITUDE VARIATION ARE SPECIFIED ON A FIELD MEASUREMENT BASIS AND INCLUDE A 10% ALLOWANCE FOR MEASUREMENT ERROR; MAXIMUM ALLOWABLE VOLTAGE EXCURSIONS, THEREFORE, ARE ± 10% FOR OUTPUT AND LOCAL TERMINAL INPUT SIGNAL, AND +30%, -20% FOR REMOTE TERMINAL INPUT SIGNAL. NOMINAL DATA SOURCE OUTPUT AND DATA USING EQUIPMENT INPUT IMPEDENCES OF 600 OHMS ±10% BALANCED RESISTIVE.

Fig. 1 – Input and Output Signals