A1 DIGITAL DATA TRANSMISSION SYSTEM
WORD GENERATOR CIRCUIT SD-1G005-01
ANALYSIS AND CLEARANCE OF TROUBLE

1. GENERAL

1.01 This section describes methods and procedures to be followed in the analysis and clearance of typical troubles which may be encountered in the word generator circuit.

1.02 This section is reissued to incorporate material from the addendum in its proper location. In this process marginal arrows have been omitted.

1.03 These trouble indications usually occur from failure to meet the test and adjustment requirements described in Section 314-505-502 covering out-of-service tests of the word generator. The suggested procedures for location of the troubles are classified in the same order as the requirements listed in Section 314-505-502 under the following headings.

A. Adjustments

B. Dipulse Output

C. Synchronization

Under the following heading, Tables A through R are found. These tables may be used to locate a defective varistor.

D. Varistor Tables

1.04 Care should be used to prevent damage to varistors by avoiding the direct application of the heat of a soldering iron.

1.05 Reference to schematic SD-1G005-01 drawings J1G000L-90 and ED-16018-90 will be helpful in applying the procedures of this section.

2. APPARATUS

2.01 Waterman Systems Rakscope (S-12-C) KS-16305

2.02 No. 262B plug (600 ohms)

3. TROUBLE CONDITIONS

A. Adjustments

3.01 When a square wave cannot be obtained at the BCA1 test point by adjusting the TMG potentiometer to meet the requirements of Test A, Step 19, of Section 314-505-502, it is probably due to one of the following reasons.

(a) No sine wave at the OSC test point, which may be due to:

(1) Defective tuning fork

(2) Faulty V2 electron tube in timing (TMG) circuit

(3) Faulty V2 electron tube in start (ST) circuit

(b) No square wave at terminal 1 of the BCA1 counter. This may be due to a faulty V1 electron tube in the timing circuit.

(c) No square wave at terminal 3 of the BCA1 counter may be caused by:

(1) Faulty V1, V2, or V3 electron tube in BCA1 counter.

(2) Shorted CR1 varistor in BCA1 counter (see Table L).

3.02 When a rectangular pulse cannot be obtained at the ST test point by adjusting the ST-SL potentiometer to meet the requirements of Test A, Step 22 of Section 314-505-502, it is probably due to one of the following reasons.

(a) A BCA counter may be faulty if a square wave is not obtained at each of the BCA test points. Starting at lowest counter, no square wave at terminal 1 of the counter would indicate the next lower numbered counter is faulty. This condition may be due to:

(1) Faulty V1, V2, or V3 electron tube in BCA counter.

(2) Shorted CR1 varistor in BCA counter (see Table L).

(b) No square pulse at terminal 1 of the ST-OUT, DIP MOD may be due to an open CR55 varistor.

(c) No square pulse at terminal 3 of the ST-OUT, DIP MOD may be due to a faulty V1 or V2 electron tube in the ST-OUT, DIP MOD circuit.

3.03 If a square pulse cannot be obtained at the DAT test point by adjusting the DAT-SL potentiometer to meet the requirements of Test A, Step 24, of Section 314-505-502, it is probably due to one of the following reasons.

(a) A square pulse on terminal 1, and not on terminal 9, of the word matrix (W MTX) may be due to a faulty V1 electron tube in the W MTX.

(b) If a square pulse appears on terminal 9 of the W MTX, and not on terminal 1 of the D OUT circuit, refer to Tables G and H.

(c) A square pulse at terminal 1 and not at terminal 7 of the D OUT circuit may be due to a faulty V1 or V2 electron tube in the D OUT circuit.

3.04 Inability to remove two of the pulses when switch S14 is operated to position 32, as stated in Test A, Step 27 of Section Section 314-505-502, is probably due to one of the following reasons.

(a) No square wave at the BCB1 test point is probably due to:

(1) Faulty V1 or V2 electron tube in BCB1 counter.

(2) Shorted CR1 varistor in BCB1 counter.

(b) If a square wave appears at the BCB1 test point and circuit is still not functioning properly, it may be due to an open CR37 varistor.

3.05 Inability to remove pulses when switch S14 is operated to other positions as stated in Test A, Steps 29 to 33 inclusive, of 314-505-502, is probably due to one of the following reasons.

(a) No square wave at the BCB test point associated with its particular counter. This condition may be due to:

(1) Faulty V1 or V2 electron tube in BCB counter not producing square wave.

(2) Shorted CR1 varistor in the above mentioned counter.

(b) When a square wave is obtained at the BCB test point, and the circuit is still not functioning properly, the trouble may be due to an open varistor CR36, CR35, or CR34, corresponding to counters BCB2, BCB3, or BCB4, respectively.

3.06 When the requirements of Test A, Step 34, of Section 314-505-502 cannot be met (that is, the start pulse does not double in width, or more than doubles, when switch S15 is operated), the trouble is probably due to a faulty varistor. (Refer to Table K.)

B. Dipulse Output

3.07 When dipulses cannot be made to meet the requirements of Test B, Step 20, of Section 314-505-502 by adjusting the LEVEL potentiometer, it is probably due to one of the following reasons.

(a) If a dipulse does not appear at the data output jack, or if the one-half-inch peak-to-peak deflection cannot be met, it may be caused by a faulty V3 electron tube in the ST-OUT, DIP MOD circuit, or a faulty varistor. (See Tables C through J.)

(b) If the dipulse is misshapen and the replacing of V3 electron tube of the ST-OUT, DIP MOD circuit does not remove the trouble, refer to Tables M, O, Q, or R.

3.08 When the requirements of Test B, Steps 22 through 29c of Section 314-505-502 cannot be met because more than one (or no) dipulse appears corresponding to each operated switch, it may be due to a faulty varistor in the word forming network. Locate by referring to Tables C through J.

3.09 When the requirements of Test B, Step 31 of Section 314-505-502 cannot be met, it may be due to more than one (or no) start dipulse appearing. This is probably caused by a faulty varistor. (Refer to Tables A and B.) If the start pulse is misshapen, refer to Tables N and P.

3.10 If the sine wave described in Test B, Step 33, of Section 314-505-502 cannot be obtained, or the one-half-inch peak-to-peak amplitude cannot be achieved by adjusting the RATIO potentiometer, it is probably due to:

(a) Faulty V2 electron tube in ST circuit.

(b) Shorted CR1 or CR2 varistor in ST circuit.

(c) Faulty V3 electron tube in DIP MOD circuit.

C. Synchronization

3.11 If the matching and error counter counts errors, failing to meet the requirements of Test C, Step 21, of Section 314-505-502, it is because word generators 1 and 2 are not in synchronism. This condition may be due to:

(a) Faulty V1 or V2 electron tube in ST circuit of word generator 2.

(b) Faulty V3 electron tube in W MTX circuit of word generator 2 if supplied with a start pulse gate.

(c) Open CR1 or CR2 varistor in W MTX circuit of word generator 2 if supplied with a start pulse gate.

D. Varistor Tables

3.12 The following tables provide the necessary information to locate an open or shorted varistor in the word generator.

3.13 The following oscilloscope adjustments are to be made before tables are used. Connect oscilloscope SYNC input to word generator SYNC test point, set SYNC-SEL switch to TRIG EXT HI, insert oscilloscope probe into BCA2 test point, and adjust sweep to obtain four cycles of square wave. (Fig. 1.)

3.14 Switch S-14 of the word generator should be on position 16.

3.15 The data output jack or start output jack referred to in this heading are located in the jack and connector circuit.

3.16 All observations will be made at the data output jack, unless otherwise specified.

3.17 While using tables, oscilloscope is to be terminated in 600 ohms.

3.18 In reference to the Bits Appear column of tables, the diagram below will show the position of bits on oscilloscope.

Pos

ST B 1 2 3 4 5 6 7 8 9 10 11 12 13 B'

(That is, see Fig. 2 which shows bits in positions [Pos] 1 and 13.)

3.19 To clarify the use of the tables, take the following case as an example. Observations are being made at the data output jack. Switch 1 is operated and bits appear in positions 1, 2, 5, and 6. Next look at the start output jack. It is found that the start pulse is not normal; bits appear in positions ST, B, 1, 2, 3, 4, 5, and 6. Turn to Tables A and B and under the Switches Operated column it is noticed that no switches are to be operated. Therefore, restore switch 1 to its off position. It is noticed that bits still appear in positions ST, B, 1, 2, 3, 4, 5, and 6. Since the above combination of bits does not appear in the Bits Appear column of Table A or B, go on to Table C. To use Table C, observations are to be made at the data output jack with no switches operated. Looking at the data output jack with no switches operated, it is found that no bits appear; therefore Table C cannot be used. Table D requires the start pulse to be normal, therefore Table D is of no help. Since the operation of switch 1 produced the trouble condition, looking down the Switch Operated column of Table E, it is noticed that switch 1 appears twice. The first row it appears in, it is noted that bits appear in positions ST and 1; the second row where switch 1 appears, bits appear in positions 1 and 2. Therefore Table E cannot be used because it was originally determined that the operation of switch 1 produced bits in positions 1, 2, 5, and 6. Table F has switches 1 and 3 operated in all rows, therefore operate switches 1 and 3. Doing this produces bits in positions 1, 2, 3, 4, 5, and 6. Looking down the Bits Appear column for this combination it appears in the row where varistor CR38 is shorted; therefore the trouble has been located.

TABLE A

Switches Operated	Bits Appear	This Varistor Open
None	Pos ST,7	CR38
None	Pos ST,3	CR39
None	Pos ST,1	CR40
None	Pos ST,B	CR41

Note 1: Observations are to be made at the start output jack.

Note 2: If any one of the varistors CR38 to CR41 are open, any observation at the data output jack while using Table A will appear normal.

TABLE B

Switches Operated	Bits Appear	This Varistor Shorted
None	Pos ST,3,7,11	CR48
None	Pos ST,1,7,9	CR49
None	Pos ST,1,3,5	CR50
None	Pos ST,1,3,5,7,9,11,13	CR51
None	Pos ST,1,3,5,7,9,11,13	CR52
None	Pos ST,1,3,5,7,9,11,13	CR53
None	Pos ST,1,3,5,7,9,11,13	CR54

Note 1: Observations are to be made at the start output jack.

Note 2: In Table B, with no switches operated, CR51 to CR54 being shorted produce the same symptoms.

TABLE C

Switches Operated	Bits Appear	This Varistor Shorted	Remarks
None	Pos ST,B,3, 4,7,8,11,12	CR24 or CR25	To determine which varistor is shorted, observe dipulse at start output jack. If double start pulse appears, CR24 is shorted.
None	Pos 1,2,5, 6,9,10,13, B'	CR22 or CR23	
None	Pos ST,1,3, 5,7,9,11,13	CR20 or CR21	To determine which varistor is shorted, observe dipulse at start output jack. If a start pulse, a blank, and another start pulse appear, CR20 is shorted.
None	Pos B,2,4, 6,8,10,12, B'	CR18 or CR19	

TABLE D

Switch Operated	Bits Appear	This Varistor Open	or This Varistor Shorted
1	Pos 1,9	CR32	CR28
2	Pos 2,10		
1	Pos 1,5	CR28	CR32
2	Pos 2,6		
3	Pos 3,11		
4	Pos 4,12	CR33	CR26
5	Pos 5,13		
6	Pos 6,B'		
3	Pos ST,3		
4	Pos B,4	CR26	CR33
5	Pos 1,5		
6	Pos 2,6		
7	Pos ST,7		
8	Pos B,8	CR30	CR29
9	Pos 1,9		
10	Pos 2,10		
7	Pos 7,11		
8	Pos 8,12	CR29	CR30
9	Pos 9,13		
10	Pos 10,B'		
11	Pos 3,11		
12	Pos 4,12	CR31	CR27
13	Pos 5,13		
11	Pos 7,11		
12	Pos 8,12	CR27	CR31
13	Pos 9,13		

Note: Start dipulse must be normal to use Table D.

TABLE E

Switch Operated	Bits Appear	This Varistor Open
1	Pos ST,1	
5	Pos 3,5	CR22
9	Pos 7,9	
13	Pos 11,13	
1	Pos 1,2	
5	Pos 5,6	CR21
9	Pos 9,10	
13	Pos 13,B'	
2	Pos B,2	
6	Pos 4,6	CR23
10	Pos 8,10	
2	Pos 1,2	
6	Pos 5,6	CR19
10	Pos 9,10	
3	Pos 3,5	
7	Pos 7,9	CR24
11	Pos 11,13	
3	Pos 3,4	
7	Pos 7,8	CR20
11	Pos 11,12	
4	Pos 4,6	
8	Pos 8,10	CR25
12	Pos 12,B'	
4	Pos 3,4	
8	Pos 7,8	CR18
12	Pos 11,12	

TABLE F

All switches in a group must be operated.

Switches Operated	Bits Appear	This Varistor Shorted
1,3	Pos 1,2,3,4,5,6	CR38
1,3	Pos 1,2,3,9,10	CR39
1,3	Pos 1,3,4,11,12	CR40
1,3	Pos 1,3,5,9,11,13	CR41

TABLE G

All switches in a group must be operated.

Switches Operated	Bits Appear	This Varistor Open
1,5	Pos 5	CR1
	Pos 1	CR5
9,13	Pos 13	CR9
	Pos 9	CR13
2,6,10	Pos 6,10	CR2
	Pos 2,10	CR6
	Pos 2,6	CR10
3,7,11	Pos 3,7	CR11
	Pos 7,11	CR3
	Pos 3,11	CR7
4,8,12	Pos 4,8	CR12
	Pos 8,12	CR4
	Pos 4,12	CR8

Note: Start dipulse must be normal to use Table G.

TABLE H

All switches in a group must be operated.

Switches Operated	Bits Appear	This Varistor Open
1,5,9,13	None	CR16
		Provided a bit appears only in position 2 when S2 is operated
2,6,10	None	CR17
		Provided a bit appears only in position 1 when S1 is operated
4,8,12	None	CR15
		Provided a bit appears only in position 1 when S1 is operated
3,7,11	None	CR14
		Provided a bit appears only in position 1 when S1 is operated

TABLE I

All switches in a group must be operated.

Switches Operated	Bits Appear	This Varistor Shorted
1,2,5,9,13	Pos 1,2,5,6,9,10, 13,B'	CR1
1,2,6,10	Pos 1,2,5,6,9,10	CR2
3,4,7,11	Pos 3,4,7,8,11,12	CR3
3,4,8,12	Pos 3,4,7,8,11,12	CR4
1,4,5,9,13	Pos B,1,4,5,8,9, 12,13	CR5
2,5,6,10	Pos 1,2,5,6,9,10	CR6
3,7,8,11	Pos 3,4,7,8,11,12	CR7
4,7,8,12	Pos 3,4,7,8,11,12	CR8
1,5,8,9,13	Pos B,1,4,5,8,9, 12,13	CR9
2,6,9,10	Pos 1,2,5,6,9,10	CR10
3,7,11,12	Pos 3,4,7,8,11,12	CR11
4,8,11,12	Pos 3,4,7,8,11,12	CR12
1,5,9,12,13	Pos B,1,4,5,8,9, 12,13	CR13

TABLE J

Switches Operated	Bits Appear	This Varistor Shorted
1 to 13	Pos 1,5,9,13	CR16
1 to 13	Pos 2,6,10	CR17
1 to 13	Pos 4,8,12	CR15
1 to 13	Pos 3,7,11	CR14

TABLE K

Switch Operated	Bits Appear	This Varistor Open
S15	ST, and three dipulses for double start B, 1, 2	CR48
S15	ST, and three dipulses for double start B, 3, 4	CR49
S15	ST, and three dipulses for double start B, 7, 8	CR50

Note 1: Observations are to be made at start output jack.

Note 2: CR51 to CR54 varistor being open show no obvious symptom of trouble. The double start repetition rate changes but it cannot be noticed unless timed or measured.

TABLE L

All switches in a group must be operated.

Switches Operated	Bits Appear	This Varistor Shorted
2,6,7,10,12	Pos B,2,4,5,8,10, 12,13	CR1 IN BCA1
2,6,7,10,12	Pos B,2,4,8,10, 12	CR1 IN BCA2
2,6,7,10,12	Pos 2,4,10,12	CR1 IN BCA3
2,6,7,10,12	Pos ST,2,4,7,10, 12	CR1 IN BCA4

TABLE M

Switches Operated	Bits Appear	This Varistor Shorted
None	Positive half of all bits appear. (See Fig. 3.)	CR42
None	Negative half of all bits appear. (See Fig. 4.)	CR43

TABLE N

Switches Operated	Bits Appear	This Varistor Shorted
None	Start dipulse and positive half of all other bits appear. (See Fig. 5.)	CR44
None	Start dipulse and negative half of all other bits appear. (See Fig. 6.)	CR46

Note: Observations are to be made at start output jack.

TABLE O

Switch Operated	Bits Appear	This Varistor Open
1	Position 1, but it appears as a positive going square wave with a dipulse superimposed on it. (See Fig. 7.)	CR42
1	Position 1, but it appears as a negative going square wave with a dipulse superimposed on it. (See Fig. 8.)	CR43

TABLE P

Switches Operated	Bits Appear	This Varistor Open
None	Start pulse appears as a positive going square wave with a dipulse superimposed on it. (See Fig. 9.)	CR44
None	Start pulse appears as a negative going square wave with a dipulse superimposed on it. (See Fig. 10.)	CR46

Note: Observations are to be made at start output jack.

TABLE Q

Switch Operated	Bits Appear	This Varistor Open
1	Position 1, but the dipulse appears unbalanced. (See Fig. 11.)	CR45
1	Position 1, but the dipulse appears unbalanced. (See Fig. 12.)	CR47

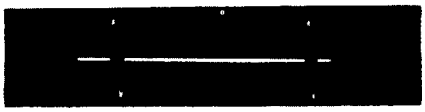
TABLE R

Switch Operated	Bits Appear	This Varistor Shorted
1	Position 1, but positive half of dipulse is larger than negative half. (See Fig. 13.)	CR47
1	Position 1, but negative half of dipulse is larger than positive half. (See Fig. 14.)	CR45

TYPICAL NORMAL OSCILLOSCOPE PATTERNS

FIG. 1

FIG. 2



TYPICAL TROUBLE OSCILLOSCOPE PATTERNS

FIG. 3

FIG. 4

FIG. 5

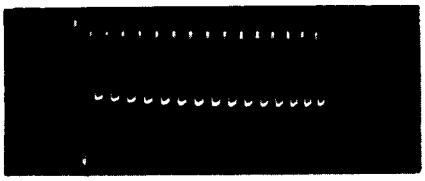


FIG. 6

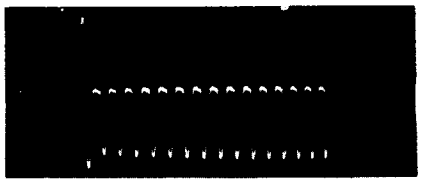


FIG. 7

FIG. 8

FIG. 9

FIG. 10

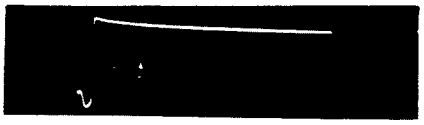


FIG. 11

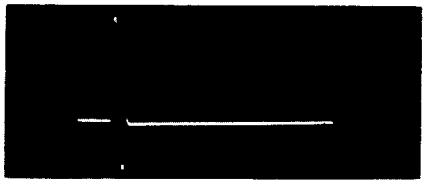


FIG. 12

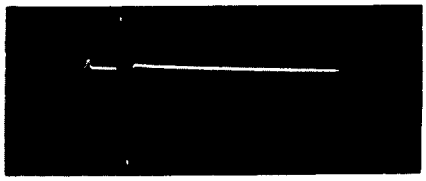


FIG. 13

FIG. 14