A1 DIGITAL DATA TRANSMISSION SYSTEM
DESCRIPTION — PARITY CHECK CIRCUIT

1. GENERAL

1.01 The parity check circuit is part of the A1 digital data system and provides a means of detecting and counting errors in the received data without removing the data line from service.

1.02 This section is reissued to cover a change in the parity check circuit to improve performance and increase sensitivity.

1.03 The data supplied at the sending end of the data line is usually preset to transmit data of either even or odd parity, that is, all data words to have either an even or odd number of bits. The received data is fed from the receiver to the parity check circuit which is preset for the type parity being transmitted. The parity check circuit then recognizes any departure of any word to the opposite parity and any odd number of omitted or added bits is recorded as an error. A count of the number of such errors is made on a counter tube and a message register.

2. OPERATION

2.01 The parity check circuit is arranged to either terminate a data line in a 600-ohm termination or it may be connected as a high impedance bridge to monitor a working circuit.

2.02 As indicated in the block diagram (Fig. 1) START and DATA signals are applied to the circuit input from the corresponding output loops of the data receiver. The DATA input is sliced and differentiated by the data slicer to produce positive spikes used to key the flip-flop circuit. At the end of each word, the start pulse, sliced and differentiated by the start slicer, tests the final condition of the flip-flop for parity.

2.03 The flip-flop circuit controls the AND gate circuit in the following manner. If at the end of a word V3B (Fig. 2) is cut off, it will prevent the start pulse from passing through the AND circuit. If at the end of a word V3B is conducting, a pulse is passed through to the multivibrator (Monostable Multivibrator) and an error is recorded.

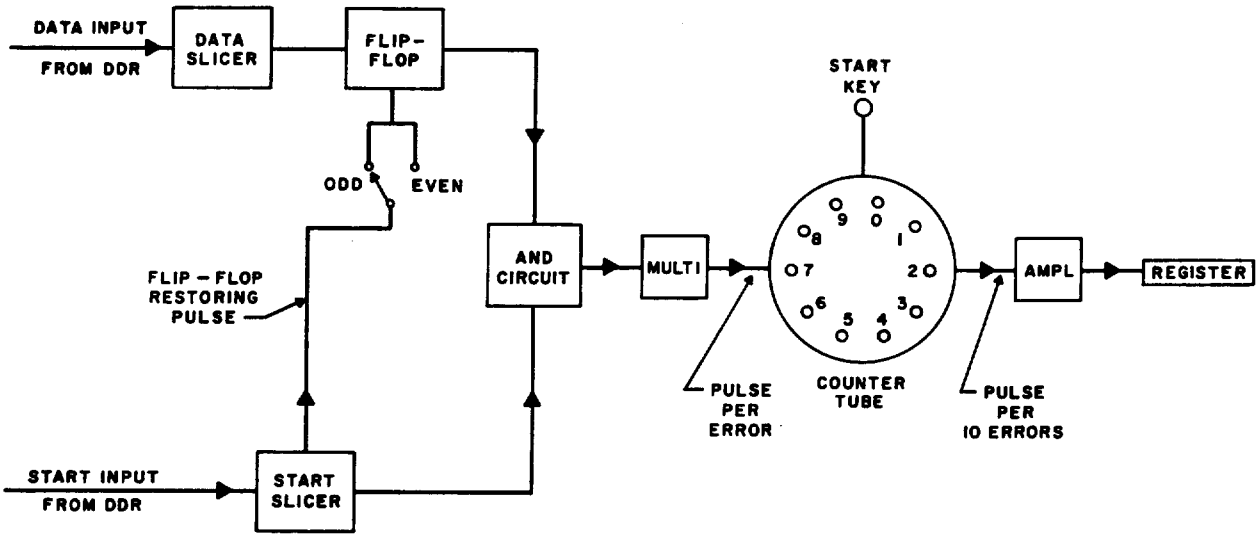

Fig. 1 – A1 Digital Data Transmission System Parity Checker-Block Diagram

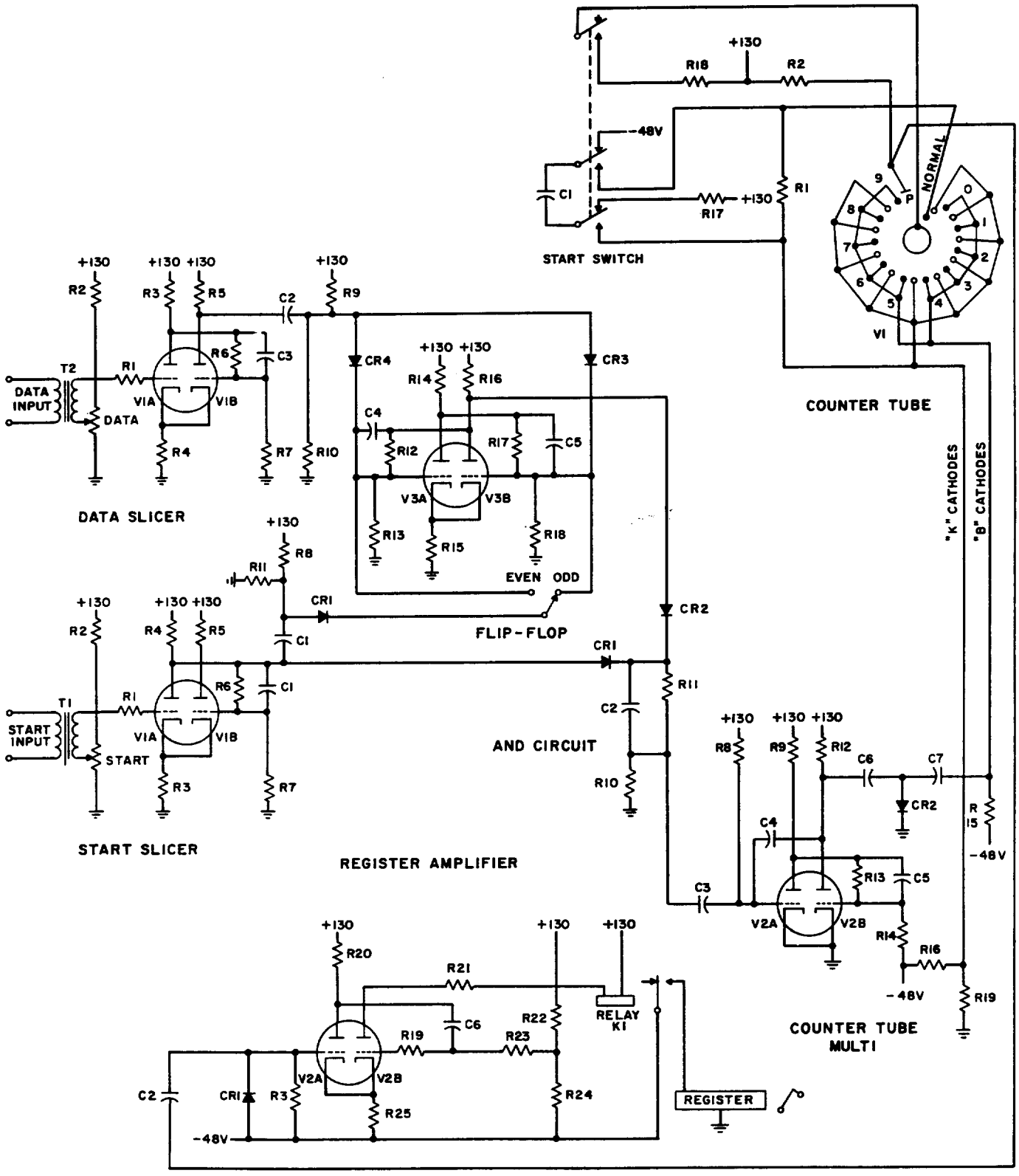

Fig. 2 – A1 Digital Data Transmission System Parity Checker — Schematic

2.04 The ODD-EVEN switch determines which side of the flip-flop is conducting at the start of a word. For odd parity V3B will be conducting prior to receipt of data and for even parity V3B will be cut off.

2.05 When set for odd parity, if the word contains an odd number of pulses, as it should, V3B will be cut off at the end of the word and will prevent the start pulse from passing through the gate circuit. The start pulse will then reset the flip-flop for the next word.

2.06 When set for even parity V3A (Fig. 2) will be conducting initially and V3B cut off. At the end of a correct word V3B is still cut off and no error will be recorded. An odd number of pulses, however, will leave V3B conducting at the word end, sending a pulse to the AND circuit to match the start pulse and a pulse will be passed to the multivibrator. The start pulse will again reset the flip-flop.

2.07 When a parity error is present it is passed by the multivibrator to the counter tube. The counter tube is a glow discharge tube containing ten glow discharge cathodes numbered from 0 to 9. Operating the START switch resets the tube and lights the '0' cathode. Each pulse received causes the glow to shift to the next higher numbered cathode. When the tenth error is received the tube starts a second revolution and a pulse is passed through an amplifier to the message register indicating ten errors received. The message register can be reset by a mechanical reset lever.

3. CIRCUIT DETAILS

3.01 Referring to Fig. 2, the DATA signal from the receiver is fed through the transformer T2 to the data slicer. This circuit transforms the received di-pulses to square-wave form. The slicing level is controlled by the DATA potentiometer which determines the magnitude of the blocking voltage on the grid of V1A and therefore the slicing level. The square-wave output of V1 is differentiated by the capacitor C2 and the resultant pulses applied to the varistors CR3 and CR4. The positive pulses pass through the varistors and are applied to the flip-flop stage V3.

3.02 When the EVEN-ODD switch is set for EVEN parity, positive pulses through CR1 will have tripped the flip-flop so that V3A is conducting and V3B is cut off. The positive data pulses through CR3 and CR4 will alternately reverse the conducting condition of the flip-flop; that is, the first pulse will cause V3A to be cut off and the second pulse will restore the original condition with V3B cut off. With an even number of pulses received, V3B remains cut off at the word end and no pulse is transmitted from V3B to the varistor CR2.

3.03 When the switch is set to ODD parity the start pulse through CR1 would have reset the flip-flop stage with V3A cut off and V3B conducting. If in this condition at the start of a word, an odd number of bits is recorded, reversals are such that V3B is again cut off. As in 3.02 with V3B cut off, no pulse is passed to CR2 and no error is indicated.

3.04 The START signal is fed to the start slicer circuit through transformer T1, and is sliced to square-wave form by the start slicer. With no START pulse V1A is cut off and the high plate voltage from R4 is applied to CR1 of the AND gate circuit. Current flow through CR1, R10, and R11 prevents the counter tube multivibrator from being activated when the flip-flop operates. When a START pulse is received it will activate the multivibrator unless V3B of the flip-flop circuit is cut off. In this case the high plate voltage of the cut off V3B through CR2, R10, and R11 will prevent the multivibrator from operating.

3.05 From the above as long as either V3B (flip-flop) or V1A (start slicer) is cut off a pulse to the AND gate will not be transferred to the multivibrator. When a parity error occurs, both of these tubes will be conducting during the START pulse interval and a negative pulse will be applied to the grid of V2A.

3.06 At the end of each word the flip-flop must be reset to its original condition. The restoring pulse is obtained from the trailing edge of the START pulse, differentiated through C1 and varistor CR1 of the start slicer circuit and applied through the EVEN-ODD switch to the grid of either side of the flip-flop V3, depending on the switch setting. This will reset the flip-flop circuit as described in 3.02 and 3.03.

3.07 The negative pulse across R10, R11 of the AND gate circuit, which represents an error, triggers the counter tube multivibrator which applies a negative pulse to the counter tube.

3.08 The counter tube is a cold cathode glow tube containing a circle of ten counting cathodes or pins numbered 0 to 9 and ten transfer cathodes located between the counting cathodes. The counting cathodes, known as 'K' cathodes, are tied together in a common ring and the intermediate or 'B' cathodes are connected together in a second ring circuit. In addition, the tube contains another cathode referred to as the NORMAL cathode, used as a starting point in the counting sequence. The tube also contains a ring anode and a small pulse anode (P).

3.09 The glow discharge in the counter tube is started by operating the START switch. The capacitor C1 in the START switch circuit has been charged to ±178 volts and, when the switch is operated, discharges in series with the counter tube plate potential and places a high enough potential between the anode and the NORMAL cathode to cause the tube to fire. As soon as the tube fires, the 'K' cathode adjacent to the NORMAL cathode starts to conduct and assumes the gap current, causing a continuous glow at that point.

3.10 The tube construction is such that when a negative pulse is received on the 'B' cathodes from the counter tube amplifier, conduction is transferred clockwise from the conducting 'K' cathode to the next adjacent 'B' cathode. When this occurs the 'B' potential drops and conduction is again transferred clockwise to the next 'K' cathode. In this way each pulse, representing a received error, will step the flow point clockwise around the ring of 'K' cathodes.

3.11 The above sequence continues until nine errors are recorded. When the tenth error is received the tube steps over to glow on the zero 'K' cathode. As this happens and conduction passes the P anode this anode momentarily draws current producing a negative pulse across resistor R2.

3.12 This pulse is differentiated by capacitor C2 of the register amplifier to obtain a positive pulse to apply to the grid of V2A. This tube is held cut off by the −48 volts on the grid except during the positive pulse interval when the tube conducts and the drop in its plate current passes a pulse along to V2B.

3.13 Tube V2B of the register amplifier is normally conducting and its plate current holds the K1 relay operated. When the pulse from V2A is received, V2B cuts off, allowing the relay to release and operate the register. The time constant of this circuit is long enough to allow adequate time for the relay to release before the normal plate current of V2B causes the relay to be again held operated.

3.14 Some difficulty has been experienced with counter tubes of early manufacture. An improved 439A tube is supplied in all parity check circuits shipped after June 15, 1957. The circuits shipped prior to this date should be checked to determine if they contain the improved type tube. The new tube may be identified by date of manufacture or a yellow dot next to the date marked in yellow on the tube. Tubes not so marked should be replaced with one of the improved type.