B S M # 7783

SAGE DATA TRANSMISSION SYSTEMS

DESCRIPTION — LINCOLN DIGITAL DATA TRANSMISSION SYSTEM

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1. GENERAL

1.01 The Lincoln Digital Data Transmission System was originally designed to provide a data transmission system to interconnect all the data processing units of the SAGE System. It was developed at the Lincoln Laboratories of the Massachusetts Institute of Technology. The original field of use of this system has been modified to restrict its application to the early trials of the SAGE System and to some of the early gap filler circuits.

1.02 This data system has the usual three main system components, that is, a transmitting and receiving data terminal connected by a transmission path. Since it was designed specifically for use with the SAGE System, however, the data terminals are either constructed as actual integral parts of the data processing units, or, if separate, must operate in close proximity to them. Consequently where this system is used the data terminals will be customer-owned and maintained. Bell System responsibility will be confined to the provision and maintenance of the connecting transmission path. The main interest herein will, therefore, lie in this portion of the data system, particularly its general transmission characteristics and the line signal it generates. To provide background information, however, brief descriptions of the input and output signals as well as the transmitting and receiving terminal apparatus are also included.

2. OVER-ALL FEATURES OF THE SYSTEM

2.01 The Lincoln data system is designed to transmit information in digital form at a rate of either 1300 or 1600 bits per second. This information is composed of the usual three components, namely, the start or synchronizing component, the data or information component and the timing component. This last is transmitted continuously. (An explanation of the functions of these signal components will be found in other sections of the Practices.) All three components are fed separately to the transmitting data terminal, combined, and then modulated on a carrier for line transmission. This data transmission system is designed for use on voice bandwidth circuits and line transmission is via a vestigial sideband system. At the receiving data terminal the three original components are recovered from the incoming line signal by demodulation and amplitude separation. They are then fed separately to the data processing apparatus.

3. INPUT SIGNALS

3.01 The signals fed to the input of the data transmitting terminal (modulator) are shown in Fig. 1. All three inputs are binary signals with marks indicated by rectangular voltage pulses of 30 volts amplitude. As indicated the spacing voltage is -30v and the marking voltage is 0. The time duration of the pulses may be either 625 or 770 microseconds. In 1600 bits per second data systems the pulses are of 625 microseconds duration; in 1300 bits per second systems the pulses are 770 microseconds duration. All three inputs are unbalanced to ground. The repetition rate of marks on the start or sync input will be constant and quite close to 25 per second. The occurrence of marks on the data input will be more frequent but they will occur in more or less random combinations depending on the information to be transmitted. The rate of occurrence of marks on the timing input will be constant and quite close to 800 per second for a 1600-bit system and 650 per second for a 1300-bit data system. There is a fixed relation between the occurrence of marks on the three inputs. Marks on the start and data inputs will always occur in exactly the same time slot as either a mark or space on the timing input.

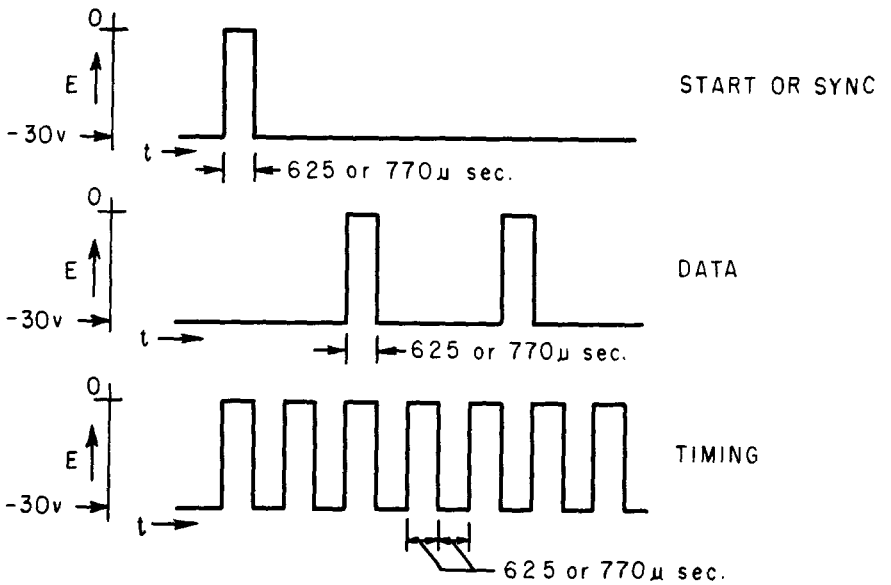

Fig. 1

4. THE TRANSMITTING DATA TERMINAL

4.01 A block diagram of the transmitting data terminal is shown in the upper portion of Fig. 2. The three input signals are first fed to a resistive network which not only combines them but adjusts their amplitudes. The result of this process is that in the combined signal the sync pulses have the largest amplitude and the timing pulses the smallest amplitude. The data pulses are adjusted to an intermediate value between these two extremes. The combined signal is coupled to a varistor modulator through the cathode follower stage. The carrier generation is discussed in some detail in the following paragraphs. In Fig. 2 the carrier generator is connected to the timing to indicate that both are derived from a common source. After modulation the signal is amplified and shaped. The purpose of this shaping is to confine the signal energy to a part of the passband of the line facilities where the envelope delay distortion is fairly small. The net result of this shaping is that most of the signal energy on the line lies between 700 and 2000 cycles. After shaping the signal is amplified and fed to the line through an output transformer. This data terminal is capable of feeding a signal voltage equal to 2.2 volts peak-to-peak into a 600-ohm line.

4.02 It should be pointed out here that in this data system the bit rates, either 1300 or 1600, are of the same order of magnitude as the carrier which is 2000 cycles per second. Thus the time interval of a marking bit, in a 1600-bit system, for example, will only contain a cycle and a fraction of carrier after modulation. The early experimental work on this system indicated that a noise advantage was realized if the bit intervals and the carrier frequency had a fixed time relationship. This was achieved by deriving both from a common source. Fig. 3 illustrates this process for a 1600-bit system. The fundamental source is a stable 1600-cycle sine wave oscillator. The output of this oscillator is shown at "A." This is clipped and shaped to form the rectangular pulses shown at "B." The repetition rate of these pulses is the same as the frequency of the source - 1600 pulses per second. These are fed to a flip-flop circuit. A flip-flop circuit is a vacuum tube circuit that has two and only two stable operating points or states. Regardless of which state the circuit happens to be in it changes rapidly to the other state when a pulse is applied to its input circuit. These circuits can also be designed so that they change states only on pulses of a given polarity.

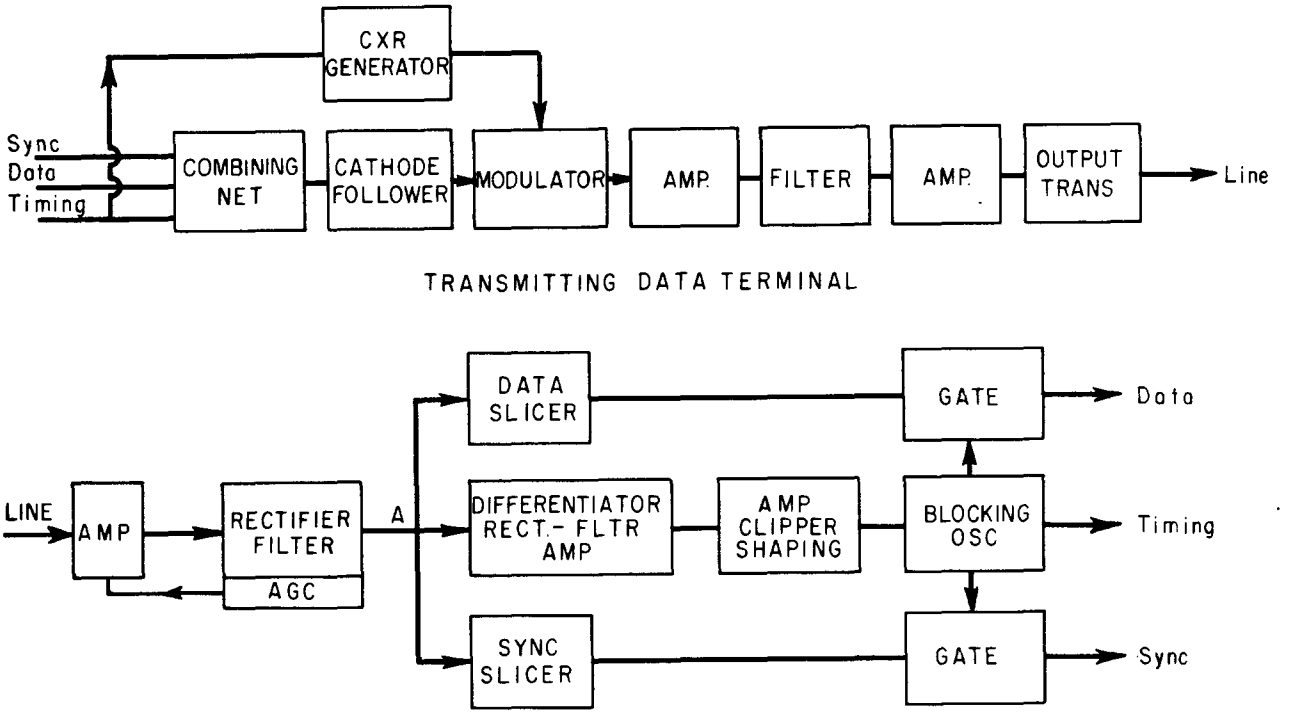
CXR GENERATOR
Sync
Data
Timing
COMBINING NET
CATHODE FOLLOWER
MODULATOR
AMP.
FILTER
AMP.
OUTPUT TRANS
Line
TRANSMITTING DATA TERMINAL
LINE
AMP
RECTIFIER FILTER
AGC
A
DATA SLICER
DIFFERENTIATOR RECT.- FLTR AMP
AMP CLIPPER SHAPING
BLOCKING OSC
SYNC SLICER
GATE
GATE
Data
Timing
Sync

Fig. 2

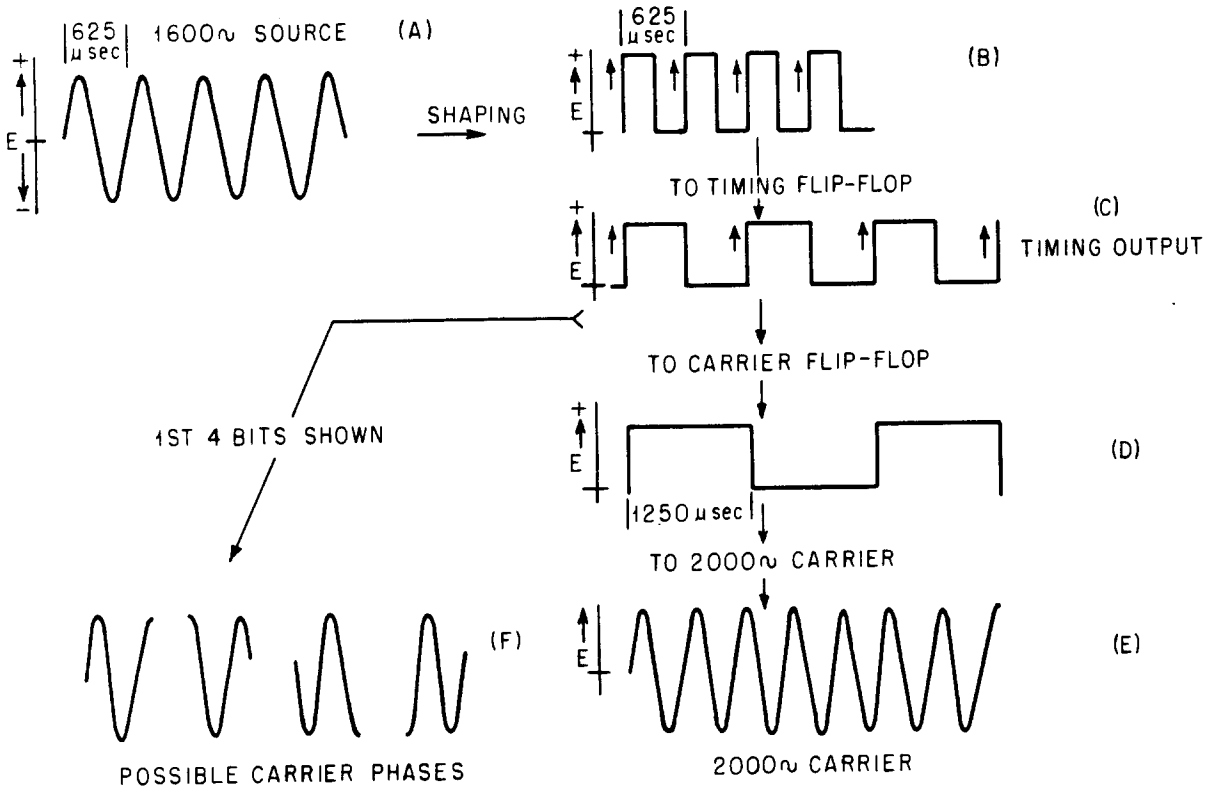
625 μsec
1600∿ SOURCE
(A)
SHAPING
625 μsec
(B)
TO TIMING FLIP-FLOP
(C)
TIMING OUTPUT
TO CARRIER FLIP-FLOP
1ST 4 BITS SHOWN
(D)
1250 μsec
TO 2000∿ CARRIER
(F)
(E)
POSSIBLE CARRIER PHASES
2000∿ CARRIER

Fig. 3

4.03 The pulses of "B" are applied to a flip-flop circuit of this latter type arranged, for example, to change states only on the positive going pulse voltages - or the leading edges of successive pulses. These are indicated by arrows. This results in the wave shape shown at "C" where the pulses occur at the rate of 800 per second. This waveshape is used as the timing and is also bridged to a second flip-flop circuit of the same type as above.

4.04 The output of this second flip-flop is the waveshape shown at "D." The pulse rate is 400 per second since this flip-flop also changes states only on the leading edges of the timing pulses (arrows in "C"). This wave is fed to a filter that picks off the fifth harmonic, 2000 cycles, which is used as the carrier. This method of deriving the timing and carrier insures that they will always be in a fixed time relationship. The result of this is that only a limited number of carrier phases can occur in a marking bit. These are illustrated at "F," which shows the carrier phases for the first four bits of the timing ("C"). Only four carrier phases are possible, regardless of the time position of the marking bit. Data systems where the bit intervals (timing) and the carrier frequency have a fixed time relation like this are called synchronous systems.

4.05 The 1300-bit systems operate in the same manner and hence are also synchronous systems. In this case, however, the frequency source is a 1300-cycle sine wave. The timing is derived from a flip-flop circuit as before; the result is a 650-cycle square wave. This is also applied to a filter which picks off the third harmonic, 1950 cycles, and this is used as the carrier. In this system there is exactly a cycle and a half of carrier in each marking bit interval and only two carrier phases result regardless of the position of the marking bit.

5. THE LINE SIGNAL

5.01 The combined input signal before modulation in the transmitting data terminal is shown in idealized form in the top part of Fig. 4. A 1300-bit/second signal has been assumed - each bit is 770 microseconds long. As drawn, this signal consists of a sync pulse, (S), four data pulses, (D), and the continuous timing wave, (T). It should be noted that as a result of the direct combination of the three input signals there are actually four marking amplitudes. The highest is that of the sync and the lowest the marking amplitude of the timing. Since data marks can be superimposed on either marks or spaces of the timing they may have either of two additional marking amplitudes.

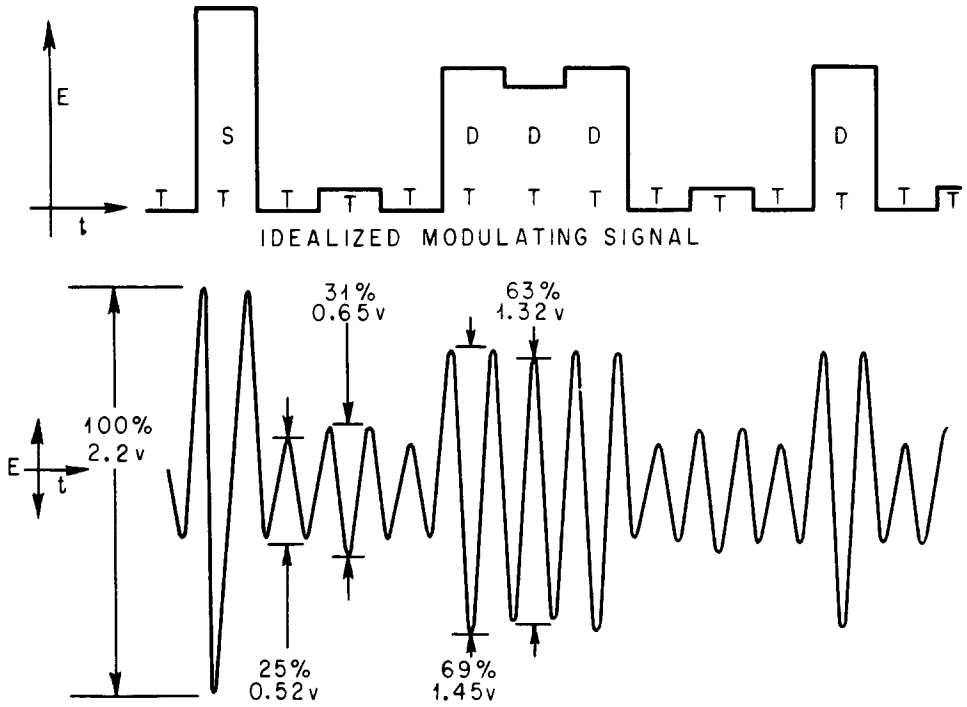

Fig. 4

5.02 After modulation the line signal at the output of the transmitting data terminal appears as shown in the lower portion of Fig. 4. The largest carrier amplitude corresponds to the sync pulse; this is a carrier voltage of 2.1 volts peak-to-peak. The minimum carrier amplitude is 0.52 volt peak-to-peak which corresponds to the timing spaces. (Thus the terminal will transmit 25% carrier under "no modulation" conditions.) Timing marks are only slightly greater, 0.65 volt. Data marks are either 1.45 or 1.32 volts depending on whether they are superimposed on a timing mark or space.

5.03 For circuit line-up purposes the output of the transmitting data terminal may be considered to be a zero level point. This data system is designed to work through an over-all 1000-cycle loss of 20 db from the output of the transmitting data terminal to the input of the receiving data terminal. The net loss of the line facilities between these points, however, has been limited to 12 db or less, if possible, due to noise considerations. The desired 20 db net loss is provided by padding out the facility loss at the receiving data terminal.

6. THE RECEIVING DATA TERMINAL

6.01 A block diagram of the receiving data terminal is shown in the lower portion of Fig. 2. (This is somewhat simplified; the terminal actually contains some fourteen vacuum tube stages.) The modulated signal at the input is first filtered to remove any incoming components above 5 kc. Following this it passes through the automatic gain control (AGC) section of the terminal which stabilizes the signal level. This tends to minimize the effect of circuit variations, etc. The signal is then rectified and filtered. The filter effectively removes components above 1000 cycles and the output is the detected envelope of the carrier. At this point the signal is fed to three different paths, each of which recovers one component of the signal, either sync, data or timing.

6.02 The timing path is shown in the center of the diagram. In this path the signal is first differentiated or, effectively, passed through a high pass filter which gives a wave of 800 cycles of varying amplitude. This is rectified and fed to a 1600-cycle filter. The output of this filter is amplified and shaped to form narrow pulses which trigger a blocking oscillator. This oscillator, whenever a pulse is applied to its grid, generates a single steep pulse such as shown in Fig. 5. The output of this oscillator is fed to three paths, one of which is the timing output, the other two feed gating circuits in the sync and data paths.

6.03 The output of the low pass filter (point A), is also fed to both the sync and data paths. The function of the slicers is to select and pass mark indications in the appropriate path. This selection is made on an amplitude basis. For example, any voltage above some maximum is read as a sync pulse and any voltage above some lower value is read as a data mark. Additional circuitry is also provided so that the sync pulses, which also appear in the data slicer output, are suppressed before they reach the data gate. The outputs of the slicers are substantially square waves of either 625 or 770 microseconds duration depending on the bit rate of the data system. These pulses are applied to the gates so that when a data mark occurs, for example, the data gate is open for nearly the whole bit interval. This allows the timing pulse, which occurs in the center of every bit interval to pass through the gate and out to the data path. Under spacing conditions, of course, the gate is closed and no pulses get through. This same action occurs in the sync path.

7. OUTPUT SIGNALS

7.01 The three components of the signal at the output of the receiving data terminal are shown in Fig. 5. It should be noted that all three components have a different waveshape from that of the input signals at the other end of the data system. Thus, the timing output is a series of 0.1 microsecond pulses of approximately 20 volts amplitude; a pulse occurs in the center of every bit interval - 1300 or 1600 times per second depending on the data system. The input timing signal on the other hand had alternate bit intervals marking and these marking pulses existed throughout the bit interval; this was an 800- or 650-cycle square wave, again depending on the data system. The essential timing information is present in both waveshapes, however. The same general scheme holds for the sync and data signals. Marks on these paths are also indicated by 0.1 microsecond pulses in the center of the bit intervals. The pulses on all three paths have the same shape since all come from the timing oscillator.

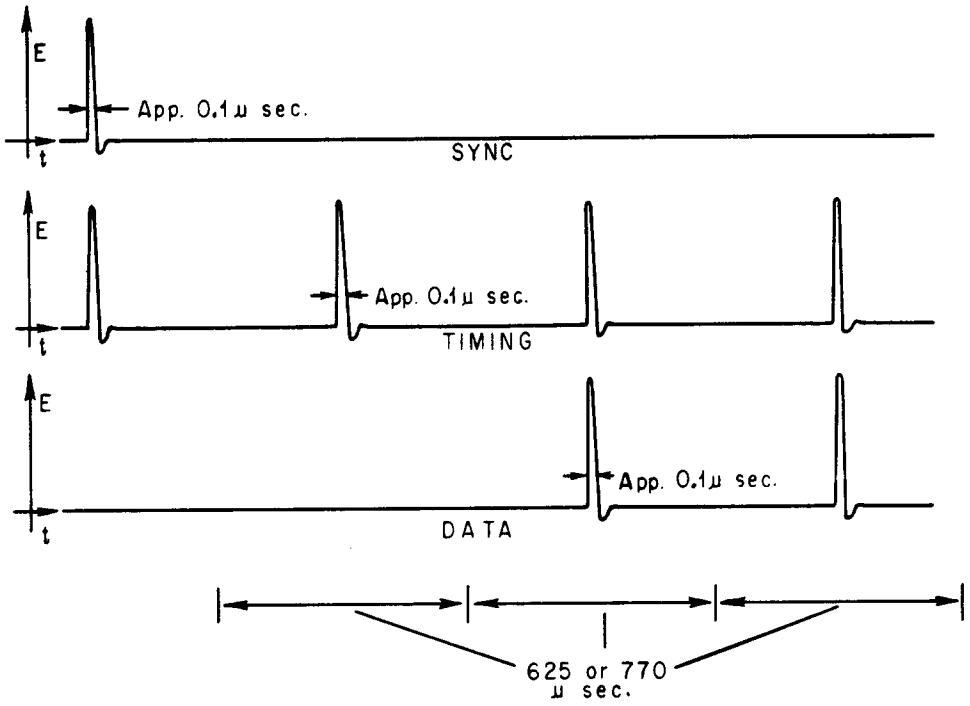
E
App. 0.1 μ sec.
t
SYNC
E
App. 0.1 μ sec.
t
TIMING
E
App. 0.1 μ sec.
t
DATA
625 or 770
μ sec.

Fig. 5