CLOCK DISTRIBUTION UNIT
DESCRIPTION AND OPERATION

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1. BACKGROUND INFORMATION

A. GENERAL

1.01 This practice provides the general description and procedures for the operation of the J98726Z-1 Clock Distribution Unit (CDU). Broad schematic coverage is given in application schematic SD-7C389-02. The plug-in equipment is coded AHG1, AHG4, AHG16, AHG25, AHG26, and AHG27.

1.02 This practice is being reissued to reflect design and operational improvements. The major changes are as follows:

- The AHG26 TD allows the CDU to provide a 2.048 MHz sine wave. This output has selectable levels of -20 dBm or -35 dBm into 75 ohm coaxial cable.
- The AHG27 TI allows the CDU to provide synchronization from a high quality DS-1 input signal having either a D4 or extended superframe (ESF) formats. The TI may also be used in concentrated timing configurations by supporting up to two auxiliary panels.

Since this is a general revision, revision arrows are not used.

1.03 It is the objective of the CDU to provide the highest quality timing with maximum reliability. The CDU is a distributor of synchronization from a high quality DS-1 input or the Stratum II system clocks of either the 4ESS or DACS machines. The CDU provides a variety of synchronized signals including all ones DS-1, 512 kHz, 64 kHz, or 2.048 MHz sine waves.

1.04 The system architecture of the CDU consists of separate A and B sides which derive their timing separately from the A and B timing inputs (fig. 4). There is no switching between these inputs. One half of the total outputs are derived from input A and the other half from input B (fig. 3). If there is a failure of one of the inputs, then all outputs derived from that input will be inhibited. The outputs of the CDU's A and B outputs are fed into switching and distribution machines. These machines perform phase build-out necessary for hitless switches between the A and B sides of the CDU.

1.05 The CDU's output signals are made available at the SDE A and SDE B terminal blocks above the shelf assembly. The Side A and Side B timing signals are divided between the SDE( ) terminal blocks. ***The first ten output taps on SDE A and SDE B terminal blocks provide outputs from Side A (TD-1 and TD-3 respectively). The second ten output taps on the SDE A and SDE B terminal blocks provide outputs from Side B (TD-2 and TD-4 respectively).***

B. CABLING

1.06 Careful placement of the CDU is needed to achieve high reliability timing. The input signal level and transmission characteristics require that a few simple guidelines be observed when installing the CDU. The CDU should be isolated from areas of high electrical noise. Care should also be taken when running power and signal cables so that the input signal cables are kept away from output cables. Good frame ground connections should be checked to ensure optimum shielding from external electrical noise. Finally, all cables connecting to the CDU should be connected such that unshielded lengths and pig-tails are kept as short as possible. Shield connections between the CDU to equipment located within a switching area should be made in accordance with AT&T Practice 805-500-410.

1.07 The input signal cabling type is essential for optimum performance. The 2.048 MHz and DS-1 inputs should be cabled with 22BF or equivalent cable only. The shield should be connected at the DACS end (hard ground) and at the CDU end of the shield designation (capacitive ground). The 16.384 MHz CTS input should be cabled with 728A or equivalent coaxial cable only. The cable should be connected so that the cable's tip and shield are connected to the tip and ring designations on the CDU. In addition, the coaxial cable's shield should be connected to the shield designation on the CDU (capacitive ground).

C. PHYSICAL DESCRIPTION

1.08 The CDU is assembled in a D4 channel bank type shelf. A front view of the panel is shown in fig. 1 for the J98726Z-1, L1,2. The L1,2 consists of the shelf assembly, side mounting brackets, and a pre-wired cross-connect output signal strip. The L1,2 panel mounts in a standard 23-inch duct type bay framework and requires about 10 inches of vertical space.

1.09 The rear of the CDU panel is shown in fig. 2. All input timing signals are connected to TS-2. Power connections are made to TS-1. Alarm closure connections are made to "E" terminals. Output signals are accessible at the SDE A and SDE B terminal blocks (Fig. 5).

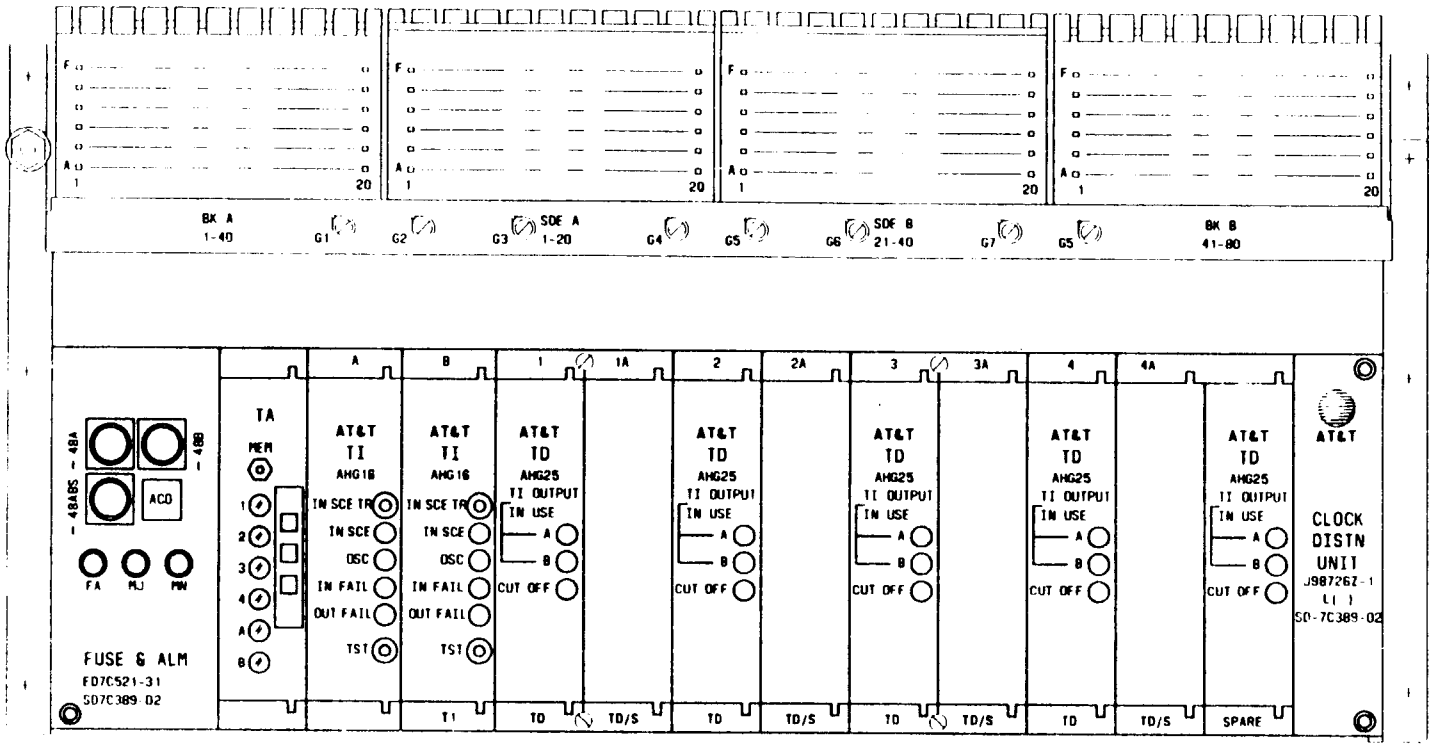


Fig. 1 - Front View of Clock Distribution Unit (J98726Z-1)

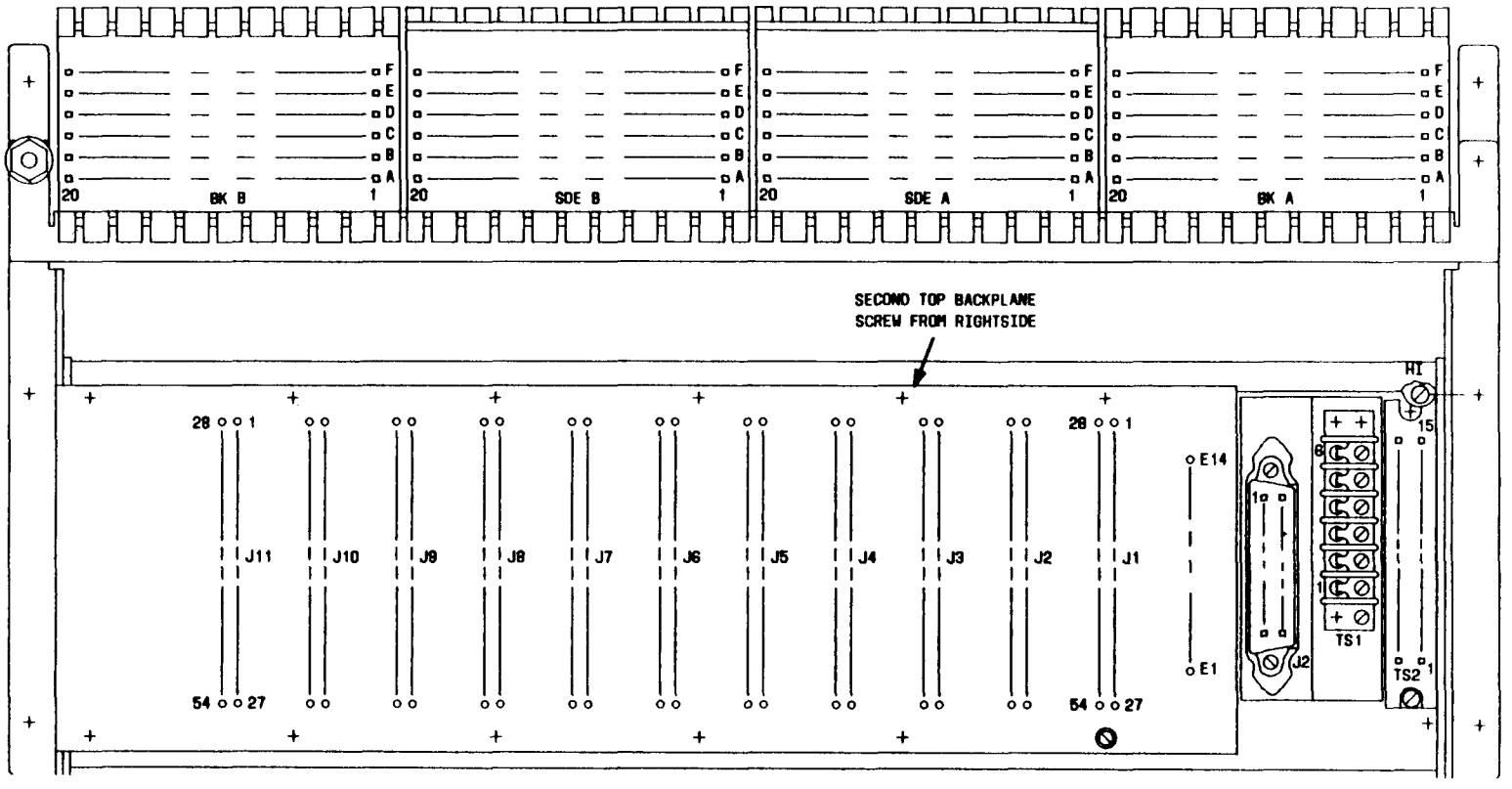


Fig. 2 - Rear View of Clock Distribution Unit (J98726Z-1)

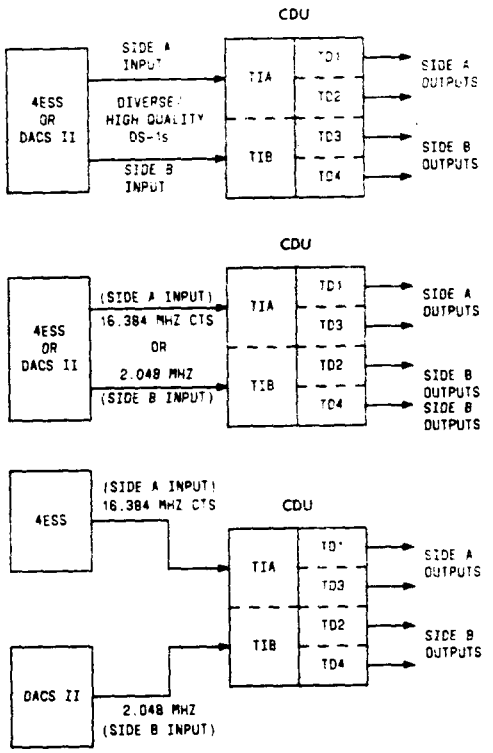


Fig. 3 - Typical Clock Distribution Unit Applications

1.10 The CDU is attached to the equipment bay using the brackets on either side of the shelf. These brackets are reversible and allow both front and rear mounting without additional hardware.

1.11 The CDU functional circuitry is contained in plug-in assemblies, which include the following:

- TA (Timing Alarm)--One per CDU
- TI (Timing Interface)--Two of the same type per CDU
- TD (Timing Distributor)--One to four per CDU.

1.12 Some components, such as fuses, alarm-status lamps, diodes, relays, and the input and output signal terminal blocks, are attached to screw mounted plates or brackets.

2. DESCRIPTION OF OPERATION

A. GENERAL

2.01 The CDU may operate any of the following input/output arrangements:

- Using a pair of 16.384 MHz CTS inputs
- Using a pair of 2.048 MHz inputs
- Using one 16.384 MHz CTS and one 2.048 MHz input
- Using a pair of DS-1 inputs
- Supplying up to 30 DS-1 framed outputs and one 512 kHz, one 64 kHz, or one 2.048 MHz sine wave output per panel
- Supplying up to 40 DS-1 framed outputs per panel

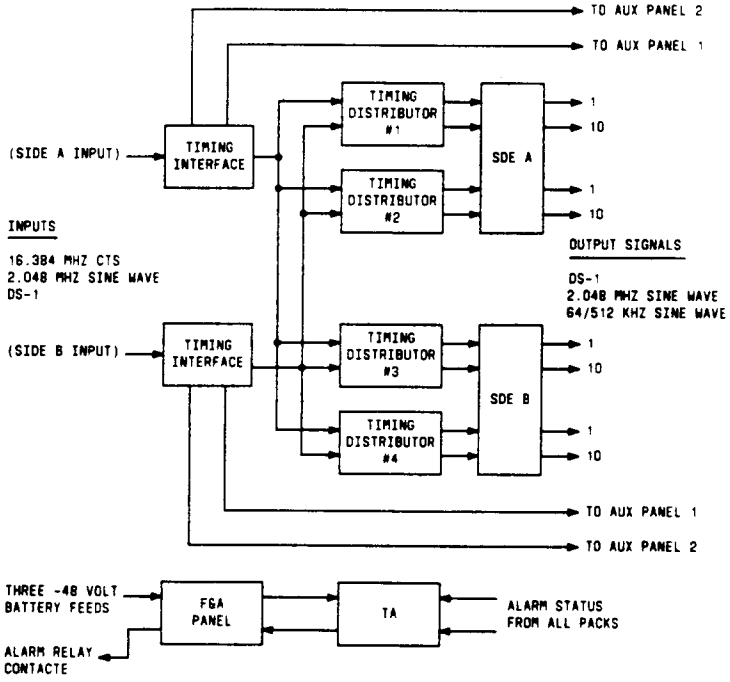


Fig. 4 - Block Diagram of Clock Distribution Unit

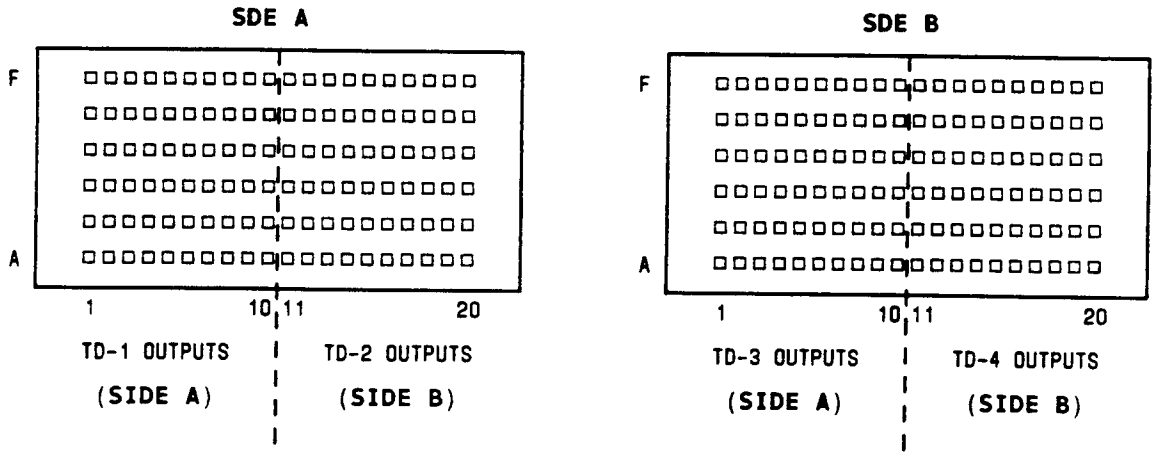


Fig. 5 - SDE( ) Terminal Block Assignments for DS-1 Outputs

- Supplying up to 80 DS-1 framed outputs using a single auxiliary panel
- Supplying up to 120 DS-1 framed outputs using two auxiliary panels.

2.02 The CDU is able to recover timing information from either the clock signal from the 4ESS (16.384 MHz CTS), the clock signal from the DACS (2.048 MHz), or a high quality DS-1 input. The CDU provides frequency and phase coherent DS-1 outputs in an all ones format with either D4 or ESF framing. The CDU also provides a 512 kHz, 64 kHz, or 2.048 MHz sine wave output for synchronizing a Primary Frequency Supply (J68857AC or J68857M).

2.03 The CDU is physically compatible with 23 inch rack mount bays and uses -48 volt office battery. The modular structure of the CDU consists of three types of circuit packs. The timing interface (TI) circuit pack interfaces directly with the input timing signals and extracts the necessary timing information. The timing distributor (TD) circuit pack recovers timing information and supplies either DS-1, 64 kHz, or 512 kHz output signals. The timing alarm (TA) circuit pack monitors alarms generated by the TI and TD circuit packs and activates dry contact relay closures for remote reporting of alarm events. These circuit packs are arranged so that a minimum complement of one TA, two TIs and two TDs are required for normal operation. A maximum of four TDs may operate in the CDU at one time.

3. TIMING INTERFACE

3.01 The input recovery circuitry for the CDU is contained on the TI circuit pack. Two TIs of the same code must be used in the same CDU panel.

3.02 The input recovery circuitry allows the phase alignment between the input signal and the output timing signal (output from the TD) to be phase coherent within 50 ns over a +/ 10 degree C temperature shift (typically less than 10 ns). The TI is also capable of inhibiting the output timing signal if the input signal becomes corrupted (loss of input signal or inability to lock to the input signal). Two TI circuit packs will be used in the CDU and be designated TI A and TI B. Each TI will recover its timing inputs independently of the other without any redundancy. This prevents output phase hits caused by input switching.

3.03 Each TI supplies input timing signals to only two TD positions via backplane connections. These signals are dual-rail unipolar composite clock format as shown in fig. 6. The TI A supplies output signals to TD positions 1 and 3; TI B will supply output signals to TD positions 2 and 4. This TD arrangement is referred to as a duplex configuration. The duplex configuration is used to create two separate timing sources (an A and B side) from the CDU. The A and B timing sources are not guaranteed to be in phase but each will be guaranteed to not change in relative phase more than 50 ns over a +/- 10 degrees C temperature shift provided the inputs remain valid. The duplex mode of operation is indicated by the green DUPLEX LED on the TI's faceplate. When all TI alarms have been cleared, only the IN SCE and DUPLEX LED's shall be lit on each TI. Switching between the A and B sources is external to the CDU. External switching machines perform a phase build-out so that at the time of a switch an error of less than 10 ns may be realized. The IN SCE TR switch on the AHG16 TI's faceplate is non-functioning and will not cause input transfers.

A. AHG16 TI

3.04 A block diagram of the AHG16 TI is shown in fig. 7. The AHG16 TI is designed to recover either the 16.384 MHz composite timing signal (CTS) clock output by the 4ESS (fig. 8a) or the 2.048 MHz clock output by the DACS (fig. 8b). The 16.384 MHz CTS signal is a pulsed output with every 2048th pulse missing. The AHG16 performs a "smoothing" of this missing pulse by the use of a "high Q" digital phase locked loop. More specific information about the input signals is listed as follows:

Frequency = 16.384 MHz:
Vnom = 1.73 Vp-p
Vmin = 300 mv p-p @ 1500 ft (with 728A or equivalent coaxial cable)
Termination = 75 ohms unbalanced
Waveshape = pulsed
Format = composite timing signal (CTS)

Frequency = 2.048 MHz:
Vnom = 1.5 Vp-p

Vmin = 300 mv p-p @ 1500 ft (with 22BF or equivalent twisted shielded cable)
Termination = 75 ohms balanced
Waveshape = sinusoidal

3.05 The TI is capable of detecting input signal failures as well as TI output driver failures. These failures are classified as either input or output failures (IN FAIL, OUT FAIL) and are displayed by red LEDs on the faceplate of the TI.

3.06 Input signal failures are monitored by a two stage detector. The first stage monitors the presence of input signals. Because this detector directly examines the input, it can sense problems in the input signal level or continuity before the TI tries to use the input. The second stage monitors the relative phase alignment between the TI's input frequency and the recovered frequency. The TI uses a phase locked loop (PLL) to perform the frequency recovery with a center frequency of 4.096 MHz. If the input and recovered frequencies differ by more than two clock cycles then an input failure is registered. The PLL's output frequency, divided by 2 and resulting in a 2.048 MHz frequency, may be monitored at the TST faceplate jack on the TI.

3.07 When an input failure is registered, two stages of signal interruption occur. The first stage of interruption inhibits the outputs of the affected timing interface. This prevents any signals from

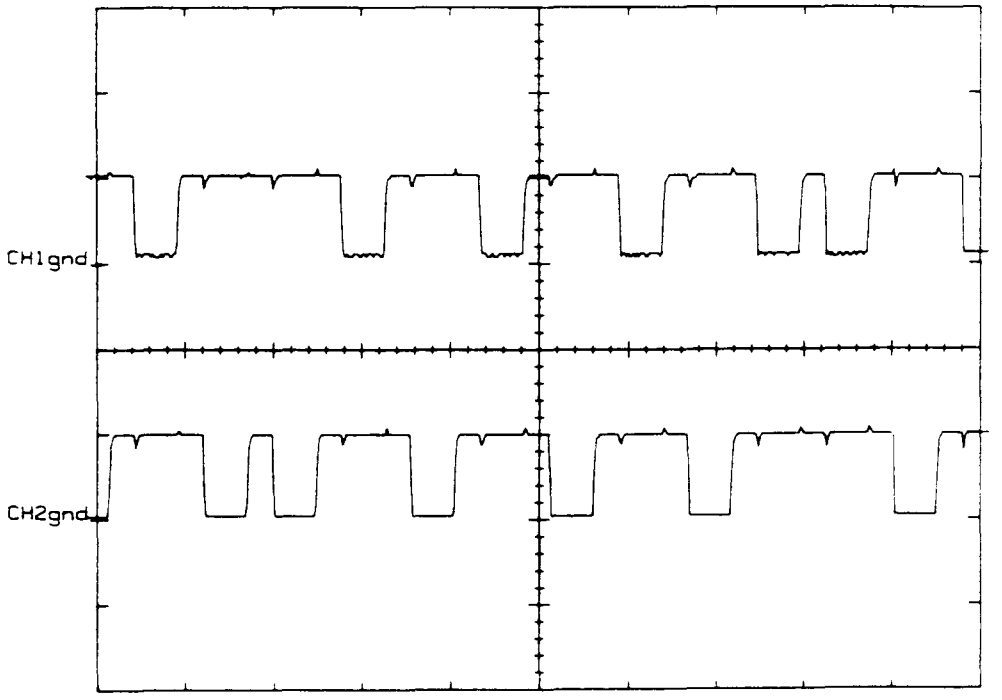


Fig. 6 - Dual-Rail Unipolar TI Output Waveforms

reaching the assigned TD packs. The second stage of interruption occurs at the timing distributor where a hard-wired "cut off" signal from the failed TI inhibits all outputs from the assigned TDs. This "cut off" condition is indicated on the affected TD circuit packs by the CUT OFF LED on the TD.

3.08 TI output driver failures are those failures that involve the timing signals from the TIs to the TDs. There are three individual signal pairs output by each TI. One of these signals pairs is for TD inputs located in the main CDU panel and the other two pairs are for those TDs in the optional auxiliary panels (see auxiliary panel expansion). If any of these outputs fail, the affected TI will issue an output failure indication. This indication is displayed by the IN FAIL LED on the TI's faceplate. The TI will also transmit a "cut off" command to the assigned TD circuit packs. This "cut off" will inhibit the signals output by the affected TDs.

B. AHG16 TI OPTIONS

3.09 The AHG16 TI has only two input option settings. The options are set by S1 on fig. 9 and labeled (2M) for the 2.048 MHz input and (16M) for the 16.384 MHz CTS input. These inputs redefine

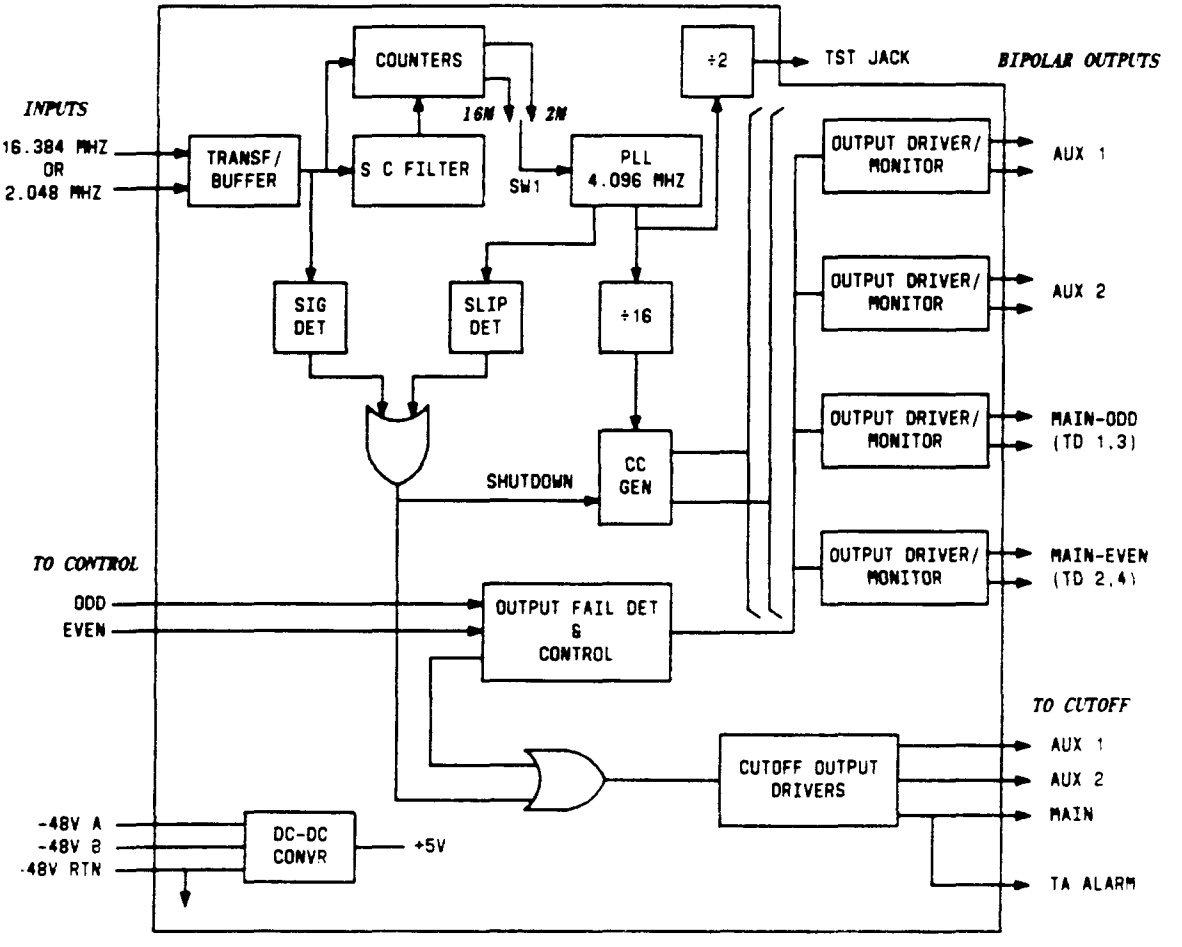


Fig. 7 - AHG16 Block Diagram

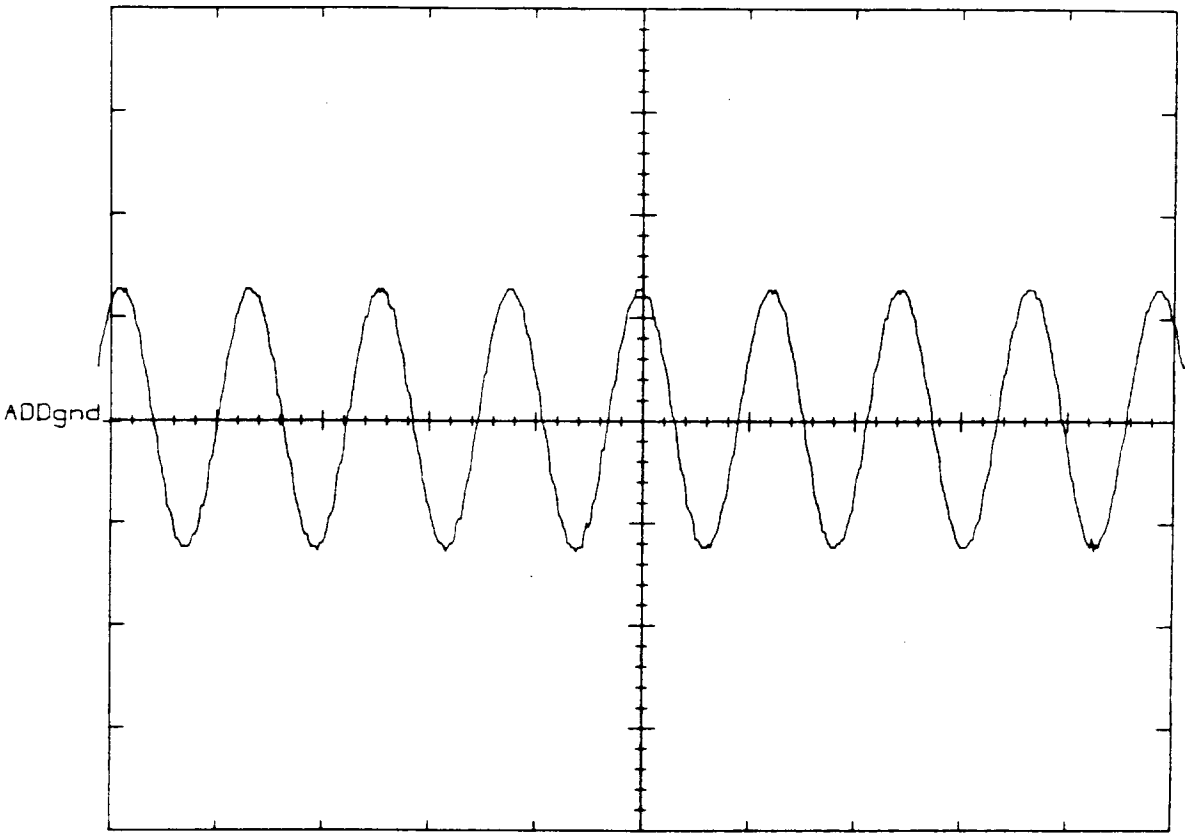


Fig. 8a - 16.384 MHz CTS Input Waveform

the input path input counters so that the same set of input punchings may be used for both inputs. If the wrong input option is selected, the TI will reject the input and report an input failure as indicated by the IN FAIL LED on the TI's faceplate.

C. AHG27 TI

3.10 The Timing Interface (TI) plug-in unit, AHG27 enables the CDU to provide synchronization from a high quality DS-1 input signal with either D4 or extended superframe (ESF) formats. The TI may also be used in a concentrated timing configuration (main-auxiliary timing arrangement). In the concentrated configuration, the main panel supports up to two auxiliary panels for a total of 120 DS-1 outputs at a single location. more specific information about the input DS-1 is listed as follows:

Frequency = 1.544 MHz:
Vnom = 6.0 Vp-p nominal level
Vnom = .6 Vp-p bridging level
Termination = 100 ohms balanced
Waveshape = standard DS-1 template (CB119)
Framing = D4 or ESF
Cable type: 22BF or equivalent

3.11 The TI's recovery circuitry (Fig. 10) allows the phase alignment between the input signal and the output timing signal (output from designated CDU

timing distributor circuit packs) to be phase coherent within 50 ns over a +/- 10 degree C temperature shift (typically less than 10 ns). The TI is also capable of inhibiting the output timing signal if the input signal becomes corrupted (loss of input signal or inability to lock to the input signal). Two TI circuit packs designated TI A and TI B are used in the CDU. Each TI recovers its timing inputs independently of the other without any redundancy.

3.12 Each TI supplies input timing signals to only two TD positions via backplane connections. These signals are dual-rail unipolar composite clock format. TI A supplies output signals to TD positions 1 and 3; TI B will supplies output signals to TD positions 2 and 4. This TD arrangement is referred to as a duplex configuration. The duplex configuration is used to create two separate timing sources (an A and B side) from the CDU. The A and B timing sources are not guaranteed to be in phase but each will be guaranteed to not change in

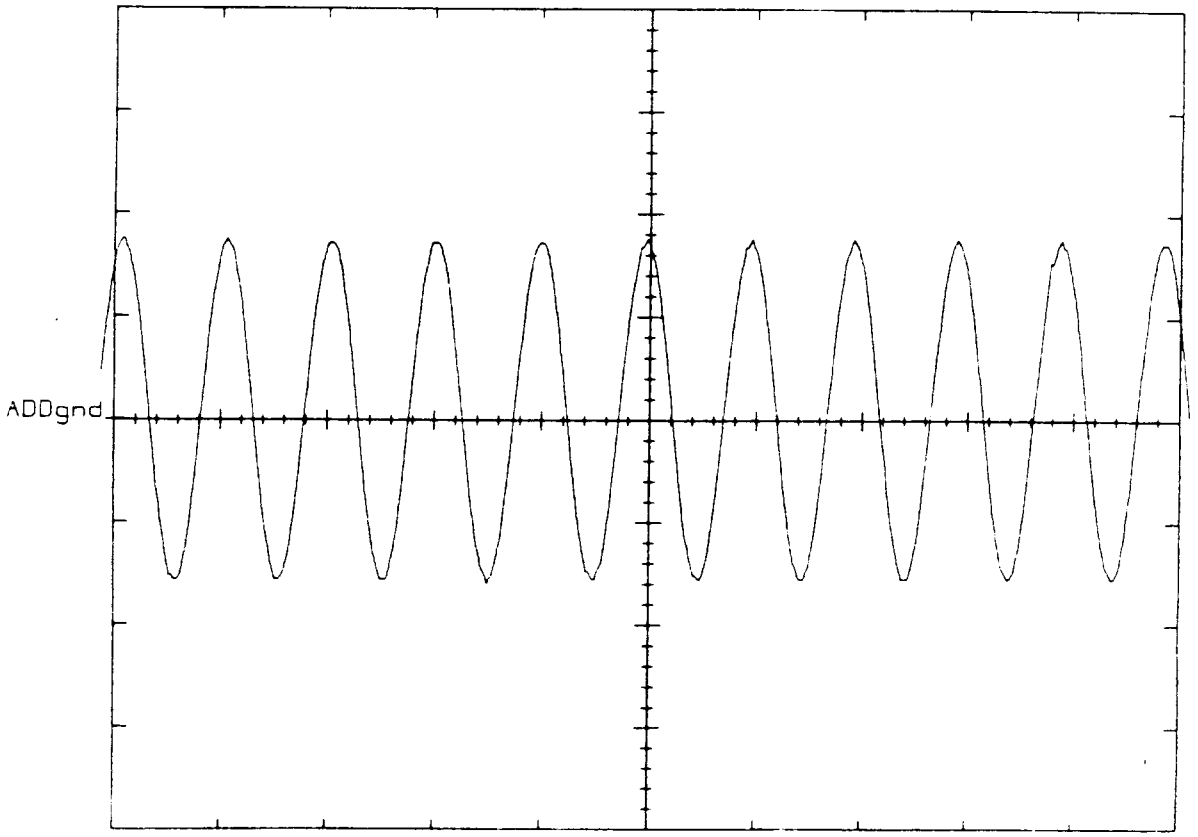


Fig. 8b - 2.048 MHz Input Waveform

relative phase more than 50 ns over a +/- 10 degrees C temperature shift provided the inputs remain valid. Switching between the A and B sources is external to the CDU. External switching machines perform a phase build-out so that at the time of a switch an error of less than 10 ns may be realized.

3.13 The TI is capable of detecting input signal failures as well as TI-output driver failures. These failures are classified as either input or output failures (IN FAIL, OUT FAIL) and are displayed by red LEDs on the faceplate of the TI.

3.14 Input signal failures are monitored by a two stage input detector. The first stage monitors the presence of input signals. Because this detector directly examines the input, it can sense problems in the input signal level continuity before the TI tries to use the input. The second stage monitors the relative phase alignment between the TI's input frequency and the recovered frequency. The TI uses a phase locked loop (PLL) to perform the frequency recovery with a center frequency of 4.096 MHz. The PLL uses an edge triggered phase detector to ensure phase coherent recovery. If the input and recovered frequencies differ by more than two clock cycles then an input failure is registered.

3.15 When an input failure is registered, two stages of signal interruption occur. The first stage of interruption inhibits the outputs of the affected timing interface. This prevents any signals from reaching the assigned TD packs. The second stage of interruption occurs at the timing distributor where a hard-wired "cut off" signal from the failed TI inhibits all outputs from the assigned TDs. This "cut off" condition is indicated on the affected TD circuit packs by the CUT OFF LED on the TD.

3.16 TI output driver failures are those failures that involve the timing signals from the TIs to the TDs. There are three individual signal pairs output by each TIs. One of these signals pairs is for TD inputs located in the main CDU panel and the other two pairs are for those TDs in the auxiliary panels (see auxiliary panel expansion). If any of these outputs fail, the affected TI will issue an output failure indication. This indication is displayed by the IN FAIL LED on the TI's faceplate. The TI will also transmit a "cut off" command to the assigned TD circuit packs. This cut off will cause the signals output by the affected TDs to be inhibited.

3.17 Because the CDU signal architecture provides for non-redundant A and B sides, the removal of an AHG27 will be service affecting. Therefore, the

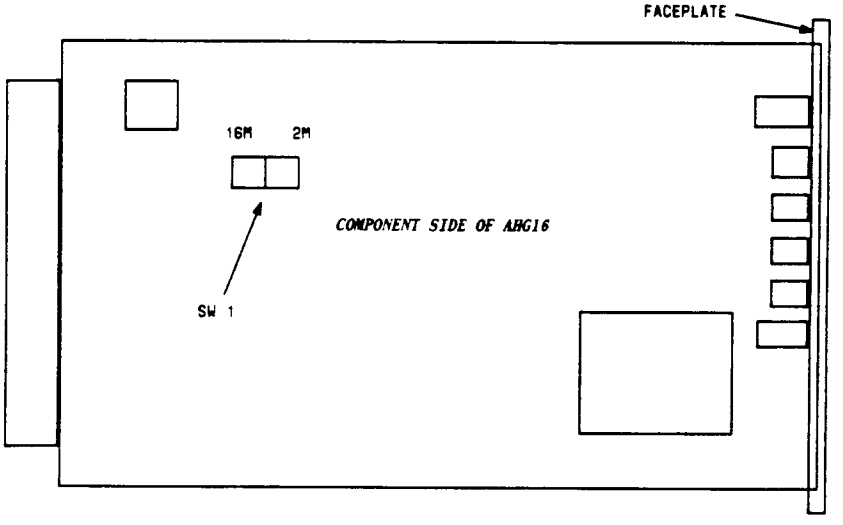


Fig. 9 - Location of Options on the AHG16 Timing Interface Circuit Pack

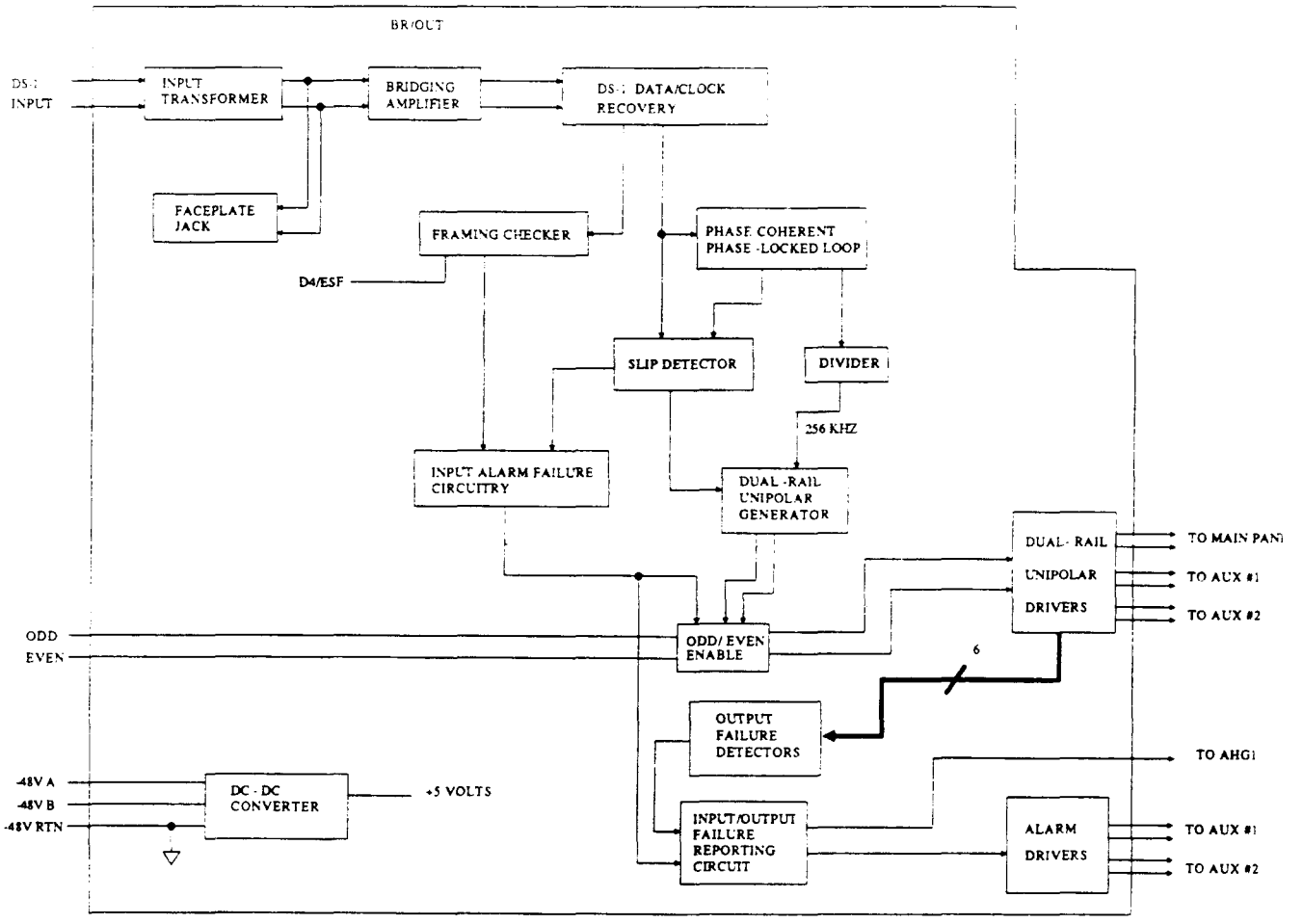


Fig. 10 - Block Diagram of AHG27 Timing Interface

removal should only be done in cases were the AHG27 is thought to be defective. Before starting the removal procedure, obtain a working AHG27 and option the pack for the intended application. The removal procedure is initiated by first pressing the ACO switch so that it lights. Next, remove the designated AHG27 and insert the new AHG27 in the same slot. The IN FAIL and OUT FAIL LEDs should stay lighted for approximately ten seconds. After the OUT FAIL LEDS extinguish, only the IN SCT and DUPLEX LEDs shall be lighted. Next, press the MEM switch on the AHG1 TA and lastly, press the ACO switch so that it is extinguished.

D. AHG27 TI OPTIONS

3.18 The location of the two sets of option switches is shown in fig. 11. The set of options located in the top center of the board is for selecting between the bridged (BR) and non-bridged (NORM) input level. The normal AHG27 DS-1 termination is 100 ohms (fig. 12). A working DS-1 line may only have a single 100 ohm termination. When it is desired to have AHG27 be this single termination, set SW1 (fig. 11) to the NORM position. If, however, timing

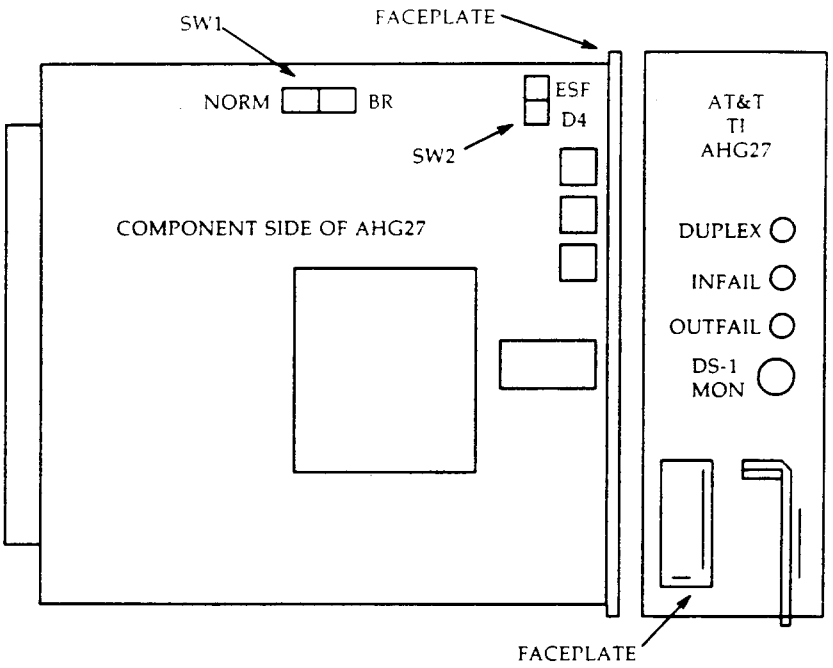


Fig. 11 - Location of Options on the AHG27 TI

information is to be extracted from a working, terminated DS-1 line, the input bridging option should be used. The bridging option allows the input impedance, presented by the AHG27 and bridging resistors, to be approximately 1000 ohms and allows the TI to accept the lower input signal level. The bridging option is used by setting SW1 to the BR position and using two external 432 ohm bridging resistors located at the DS-X.

3.19 The second set of options selects the input framing pattern for the frame detector. The selections are either D4 or extended superframe (ESF). The framing pattern may be selected the desired position of SW2.

4. TIMING DISTRIBUTOR

4.01 A maximum of four TDs may be plugged into a single CDU shelf assembly. The TDs are only inserted into the TD ( ) slots. The TD/S positions should not be used. They are reserved for future enhancements to the CDU.

4.02 Each TD receives its input signal from only one TI. The four TDs are assigned specific input TIs so that two TDs accept their inputs from TI A and the other two from TI B as shown in Table A. The TDs are numbered one to four as indicated by the frame designation strip. The odd numbered TDs (1 and 3) receive their input signals only from TI A. The even numbered TDs (2 and 4) receive their input signals only from TI B. It is by this fixed assignment of TI s and TDs that two separate timing sides may be created. Those two TDs that receive inputs from TI A create the "A" side and those that receive inputs from TI B create the "B" side.

4.03 The outputs from the CDU are determined by a selection of TD circuit packs (AHG4, AHG25, and AHG26). The types of outputs are DS-1 with ESF or D4 framing, 64-kHz, 512-kHz, or 2.048-mHz sine waves. The different outputs are selected by inserting a specific TD pack into any of the CDU's TD slots. The TD/S slots are not used at this time and are reserved for future enhancements.

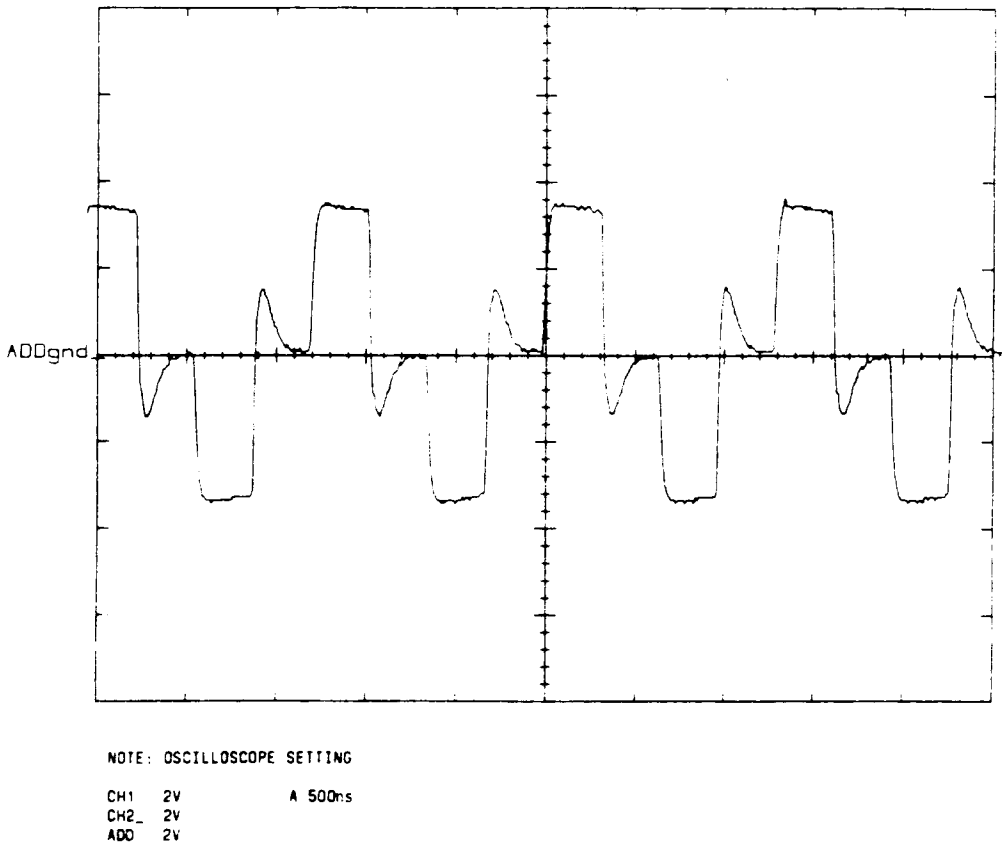


Fig. 12 - DS-1 Input Waveform (Terminated on 100-ohm)

The output signals are defined as follows:

(a) DS-1 (AHG25 TD)

Waveshape: Standard DS-1 template for new equipment

Amplitude: 3 volts peak nominal

Output Impedance: 100 ohms nominal

Output Range: 1140 feet max (655 + 85 + 400)

Framing: Extended super frame (ESF) or D4 selectable

(b) 64 kHz (AHG4 TD)

Waveshape: Sinusoidal

Amplitude: –23 dBm nominal with attenuator or +7 dBm nominal without attenuator

Output impedance: 130 ohms balanced

Output range: 1000 feet max with attenuator

(c) 512 kHz (AHG4 TD)

Waveshape: Sinusoidal

Amplitude: –54 dBm nominal with attenuator +10 dBm nominal without attenuator

Output Impedance: 130 ohms balanced

Output Range: 1000 feet max with attenuator

(d) 2.048 MHz (AHG26 TD)

Waveshape: Sinusoidal

Amplitude: –20 dBm or –30 dBm nominal with selectable attenuator

Output Impedance: 75 ohms unbalanced

Output Range: 1500 feet max with 728A or equivalent cable

TABLE A

ASSIGNED OPERATING STATES

TIMING SIDE	TI IN USE	ACTIVE TD
A	TI-A	TD-1
A	TI-A	TD-3
B	TI-B	TD-2
B	TI-B	TD-4

Note: The CDU does not make use of input or output transfer switching. Upon loss of either input or output sources, all outputs of the affected side will be inhibited.

A. AHG25 TD

4.04 The AHG25 timing distributor (TD) circuit pack provides DS-1 level signals for synchronizing network elements. The DS-1 signal is an all-ones format with a selectable framing pattern between D4 or ESF.

4.05 The input to the circuit pack is the standard dual-rail unipolar composite clock signal output by the respective timing interface (TI) circuit pack. The 64 kHz dual-rail signal enters the input selector/failure detector (Fig. 13) where one of the two input clocks is selected based upon pulse width and presence of the clock. If either the TI's input or outputs fail, then the output of the TD will "cut off" and a major alarm will be reported.

4.06 A delayed switching protocol is employed upon the restoration of one of the two bad inputs. The protocol checks to make sure that the input signal is good for at least one second before it is to be used as an input. The use of this delayed switch prevents disrupted outputs from the TD. The recovered input signal is then input to a digital phase locked where it is converted into a de-jittered clock at 3.088 MHz. The 3.088 MHz clock is next fed into the DS-1 framing generator where the pre-selected framing format is placed on the all ones DS-1 signal. The output of the framing generator is a unipolar DS-1 signal which is converted to a bipolar signal by the unipolar/dual-rail rate converter. The bipolar DS-1 signal is then fed into the output enable buffer where the DS-1 signal is fanned-out before it enters the output driver stage. The buffer also serves to inhibit the DS-1 signal while operating in the "cut off" mode. Each of the ten output drivers is separate and transformer coupled.

4.07 Each output is equalized to match the DS-1 template at the DS-X to 400 feet [Compatibility Bulletin No. 119 (CB119), Interconnection Specification for Digital Cross-Connects, Issue 3, October, 1979]. The maximum distance from the CDU through the DS-X to the far end terminating equipment is 1140 feet: 400 feet (distance to DS-X with proper signal amplitude) +85 feet (DS-X interconnection distance) +655 feet (maximum distance from the DS-X cross-connect to terminating equipment). All outputs are designed to work into a 100 ohm load over 761A twisted shielded cable or equivalent. All output signals should be accessed at the SDE A and SDE B terminal blocks directly to reduce the possibility of cross-talk and high frequency emissions. In addition, each unused DS-1 output should be terminated by a 100 ohm resistor (fig. 14). The 100 ohm resistors must be removed if the corresponding output is to be used.

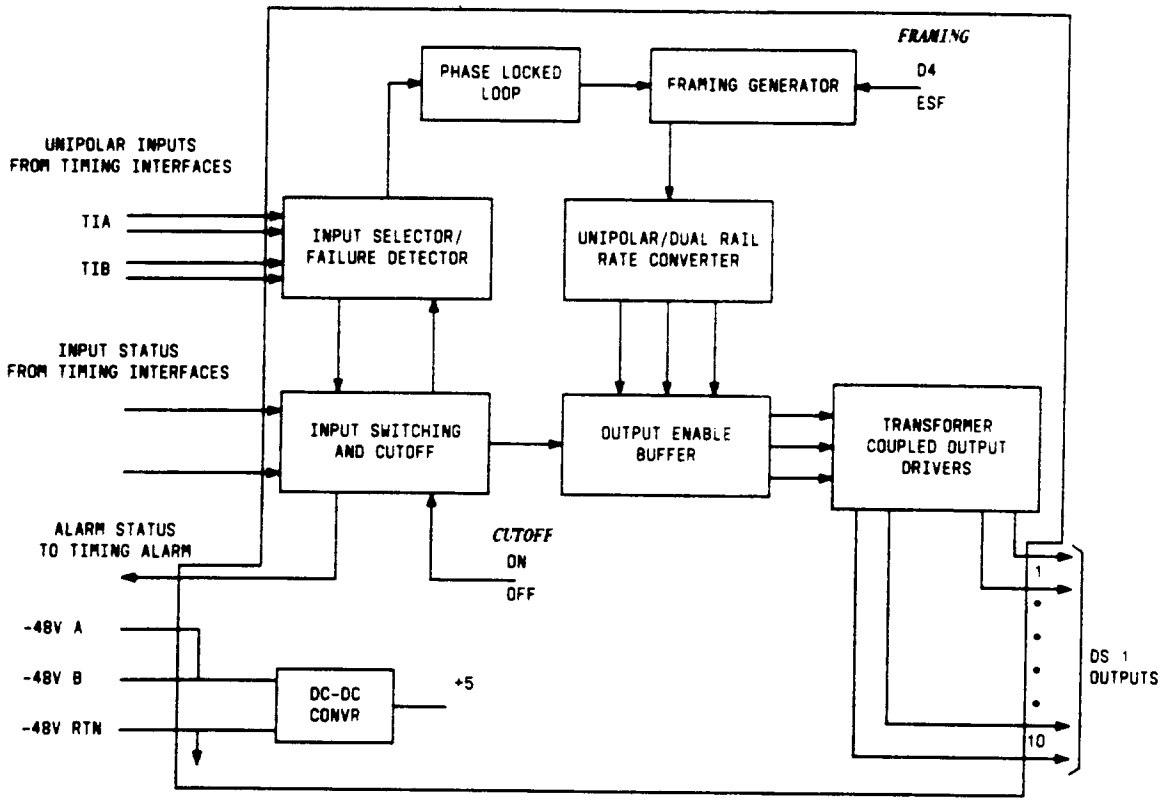
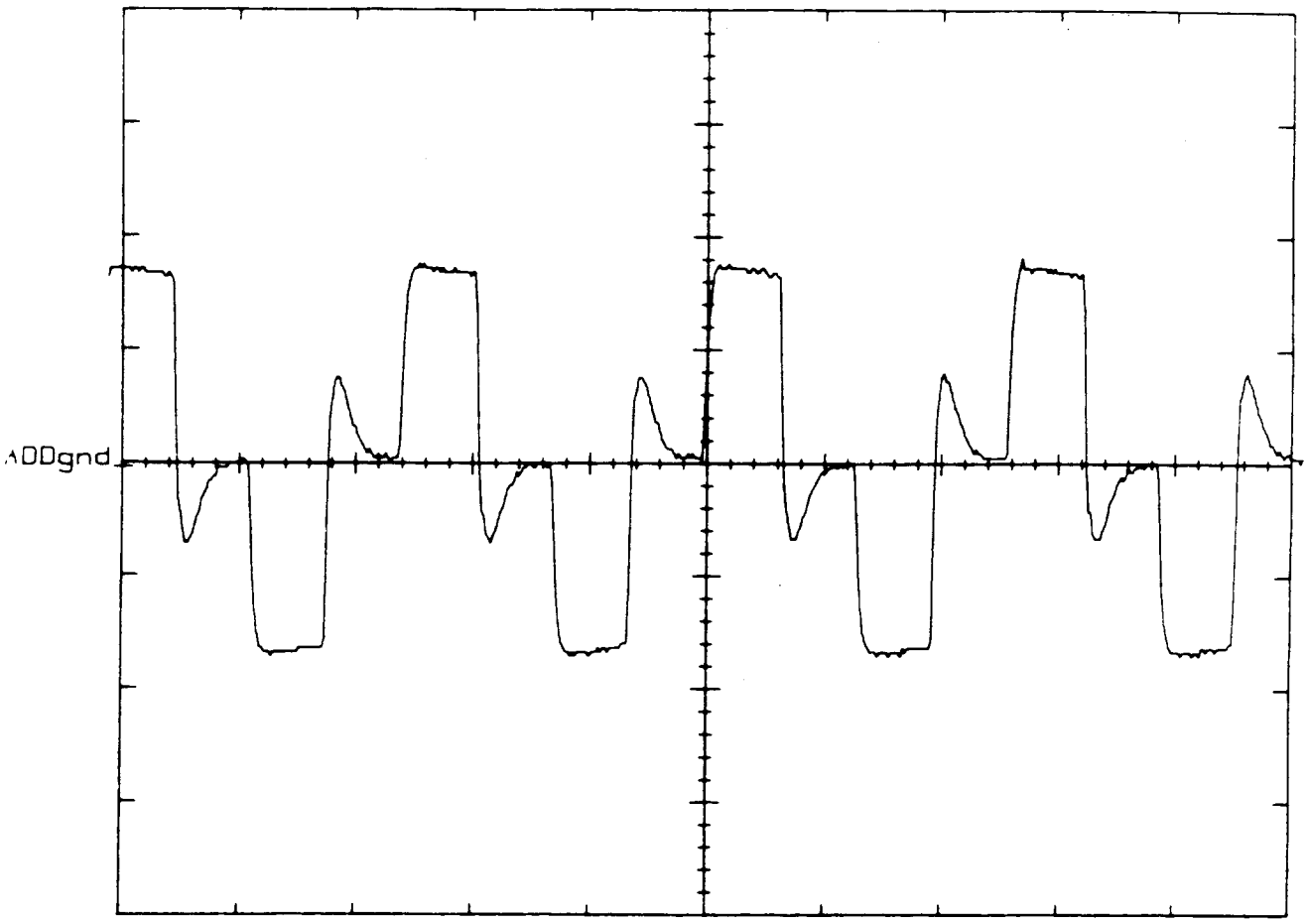


Fig. 13 - Block Diagram of the AHG25 Timing Distributor



NOTE: OSCILLOSCOPE SETTING

CH1 2V A 500ns
CH2_ 2V
ADD 2V

Fig. 14 - DS-1 AHG25 Output Waveform (Terminated on 100-Ohm)

B. AHG25 TD OPTIONS

4.08 There are two available options on the AHG25 circuit pack. The framing pattern option, mentioned previously, selects a D4 or ESF framing pattern. The framing pattern is chosen by selecting the proper section and position of switch SW 101 shown on fig. 15. The switch section labeled "1" selects the framing mode and the section labeled "2" selects the "cut off" option. Switch section 1 in the "D4" position selects the D4 framing format and in the "ESF" position the extended super frame (ESF) format is selected. **(The switch section 2 should always be set to the "in" position.)** This activates the "cut off" feature during CDU input failure conditions.

C. AHG4 TD

4.09 The AHG4 timing distributor circuit pack (fig. 16) receives dual-rail unipolar signals from the TIs and converts them to a single sine wave output (figs. 17a or 17b). This output is capable of synchronizing the PFS (Primary Frequency Supply). In addition, the AHG4 TD provides this synchronization at 512 kHz or 64 kHz frequencies

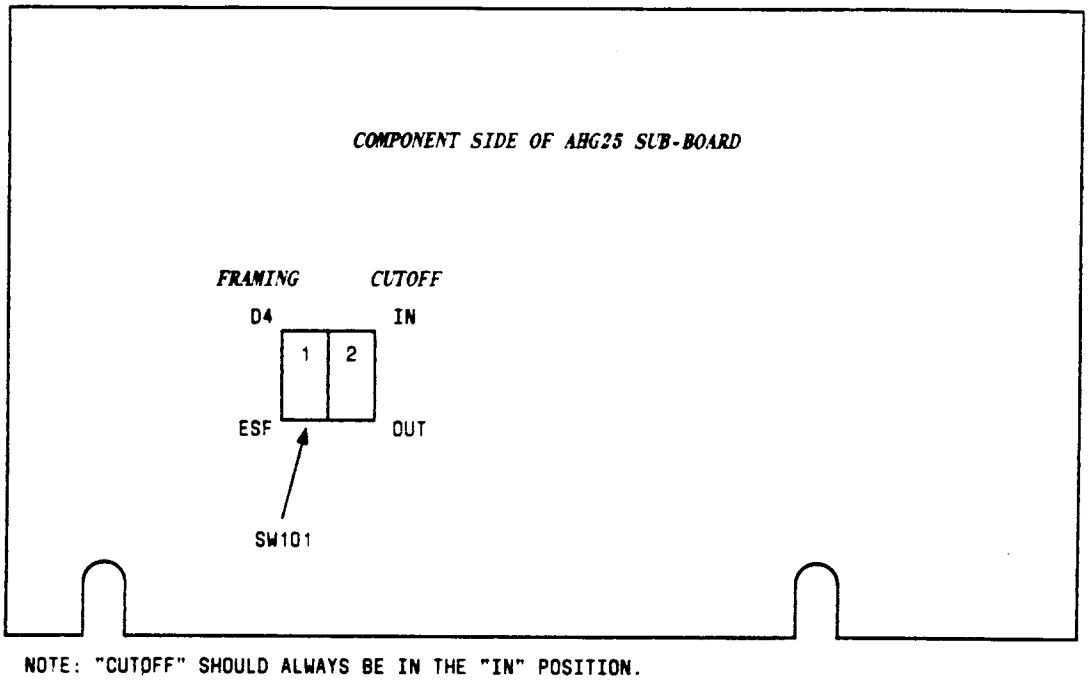


Fig. 15 - Location of Options on the AHG25 Timing Distributor

with output levels of either 10, -23, or -54 dBm. This TD is compatible with all the existing backplane connections on the J98726Z-1 panel. This TD circuit pack can be inserted into any TD card slot of the CDU. The TD/S slots are not intended to be used at this time and are reserved for future enhancements.

4.10 Under normal operating conditions, the AHG4 will supply an output timing signal that is proportional in frequency to the input of the CDU. If the CDU has an input reference failure, the outputs of the AHG4 will be disabled as indicated by the red "CUTOFF" LED on the faceplate of the AHG4. When the input reference to the CDU is restored, the output of the corresponding AHG4 is enabled. When the AHG4 is inserted onto the CDU panel, the red "CUTOFF" LED will light to indicate that the output is disabled until the circuitry can synchronize to the input timing signal. After 2 seconds, the "CUTOFF" LED will extinguish and the output will be enabled.

D. AHG4 TD OPTIONS

4.11 The AHG4 is provisioned by selecting the proper position of the plug and jack assembly labeled 64 kHz and 512 kHz (fig. 18). Provisioning the AHG4 for output level may be done in one of two ways: using the attenuated output or using the non-attenuated output.

4.12 In most cases the output signal from the AHG4 will come from the attenuated output. The attenuated output has two settings that can be selected by using the DIP switch. Positions 1 and 2 on the DIP switch need to be set to the ATTEN position. If the 64 kHz frequency is selected, the -54 dBm output level should be used. The -54 dBm level is selected by setting DIP switch positions 5 and 6 to the -54 dB position. If the 512 kHz frequency is selected, the -23 dBm output level should be used. The -23 dBm level is selected by

TABLE B (NOTES 1, AND 2)
AHG4 OUTPUT AND CONTROL WIRING

ATTENUATED-OUTPUT CONNECTIONS

FROM		TO		
CONNECTOR	TERMINALS	CONNECTOR	TERMINALS	TYPE
J4 (TD-1)	22	SDE A	D1	GRD
J4 (TD-1)	20	SDE A	E1	TIP
J4 (TD-1)	47	SDE A	F1	RING
J10 (TD-4)	22	SDE B	D20	GRD
J10 (TD-4)	20	SDE B	E20	TIP
J10 (TD-4)	47	SDE B	F20	RING

NONATTENUATED-OUTPUT CONNECTIONS

FROM		TO		
CONNECTOR (NOTE 3)	TERMINALS	CONNECTOR	TERMINALS	TYPE
J4 (TD-1)	22	SDE A	D1	GRD
J4 (TD-1)	21	SDE A	E1	TIP
J4 (TD-1)	48	SDE A	F1	RING
J10 (TD-4)	22	SDE B	D20	GRD
J10 (TD-4)	21	SDE B	E20	TIP
J10 (TD-4)	48	SDE B	F20	RING

*Note 1:*All tip, ring, and ground wires are 26-gauge twisted triples with three twists per inch and within one half at each end.

*Note 2:*All cabling from the SDE () terminal blocks to the PFS-2B (J68857AC) or PFS-2 (J68857M) will be 22BF-type cable (or equivalent) and should not exceed a length of 1000 feet.

setting DIP switch positions 5 and 6 to the -23 dB position. The attenuated output is accessed from TD backplane terminals 20 (tip), 47 (ring), and 22 (shield) as shown in Table B. Detailed wiring information showing input connections to the PFS-2B (J68857AC) may be found on SD-50802-1.

4.13 If the office environment is noisy and the low level signal cannot be transmitted from the CDU without interference, the non-attenuated output of the AHG4 may be used. The non-attenuated output provides an output signal at approximately 10 dBm level and may be selected by setting DIP switch positions 1 and 2 to the 10 dB setting. This signal may be accessed at TD slot 4 backplane terminals 21 (tip), 48 (ring), and 22 (shield). Cabling between the CDU and the PFS requires an external attenuator near the PFS to supply the proper input signal level.

E. AHG26 TD

4.14 The Timing Distributor (TD) plug-in unit, AHG26, is used in the CDU to provide a 2.048 MHz

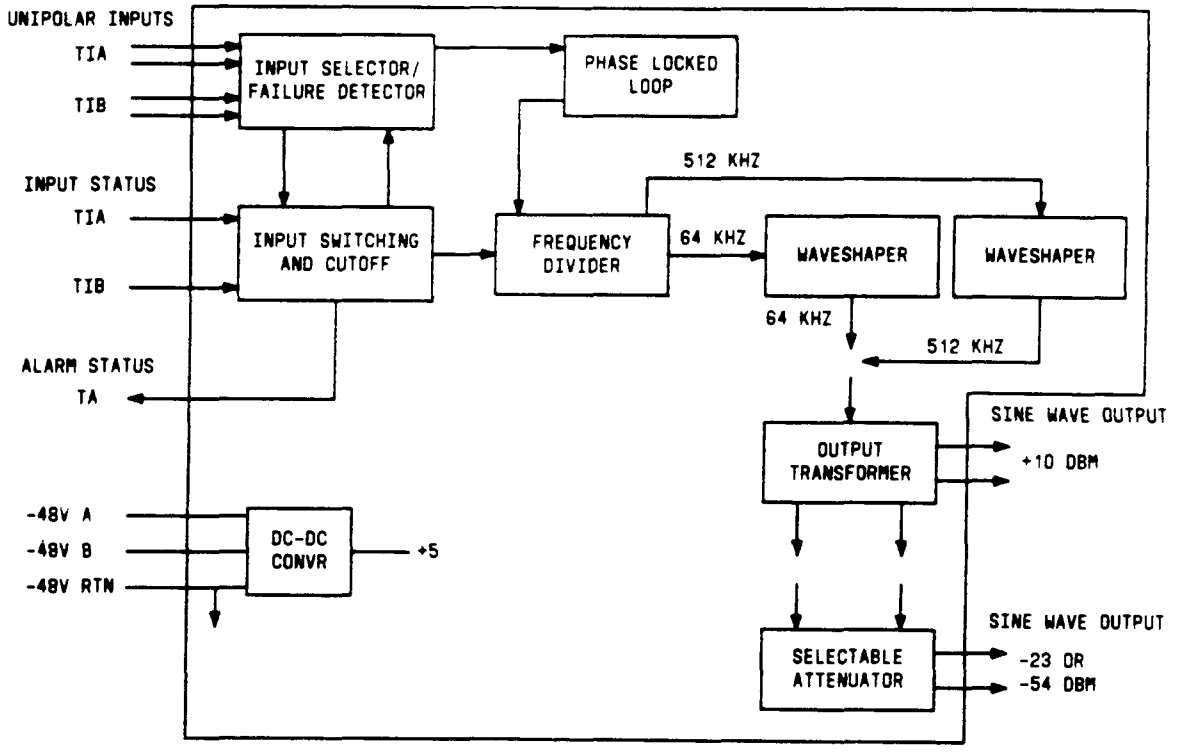


Fig. 16 - Block Diagram of Timing Distributor (AHG4)

sine wave output. The output provides a -20 dBm or -35 dBm level into 75 ohms to network elements (NE) requiring this input. The TD is intended to be used in the translation of synchronization from the Digital to Analog communications networks.

4.15 The input signal to the TD is a dual-rail unipolar composite clock signal received from the TI (timing interface) plug-in units. This signal is recovered and the signal quality is monitored by single-rail failure detectors (fig. 19). A 64 kHz square wave is derived from the input and then multiplied by a phase locked loop (PLL) to a frequency of 4.096 MHz. The PLL employees a phase coherent phase detector that aligns the edges of the input 64 kHz with the 4.096 MHz output. The PLL also incorporates a slip detector that monitors the phase error between the input and output frequencies of the phase detector. If this error is greater than three cycles of 4.096 MHz, a slip is registered.

4.16 The 4.096 MHz is divided by two to produce

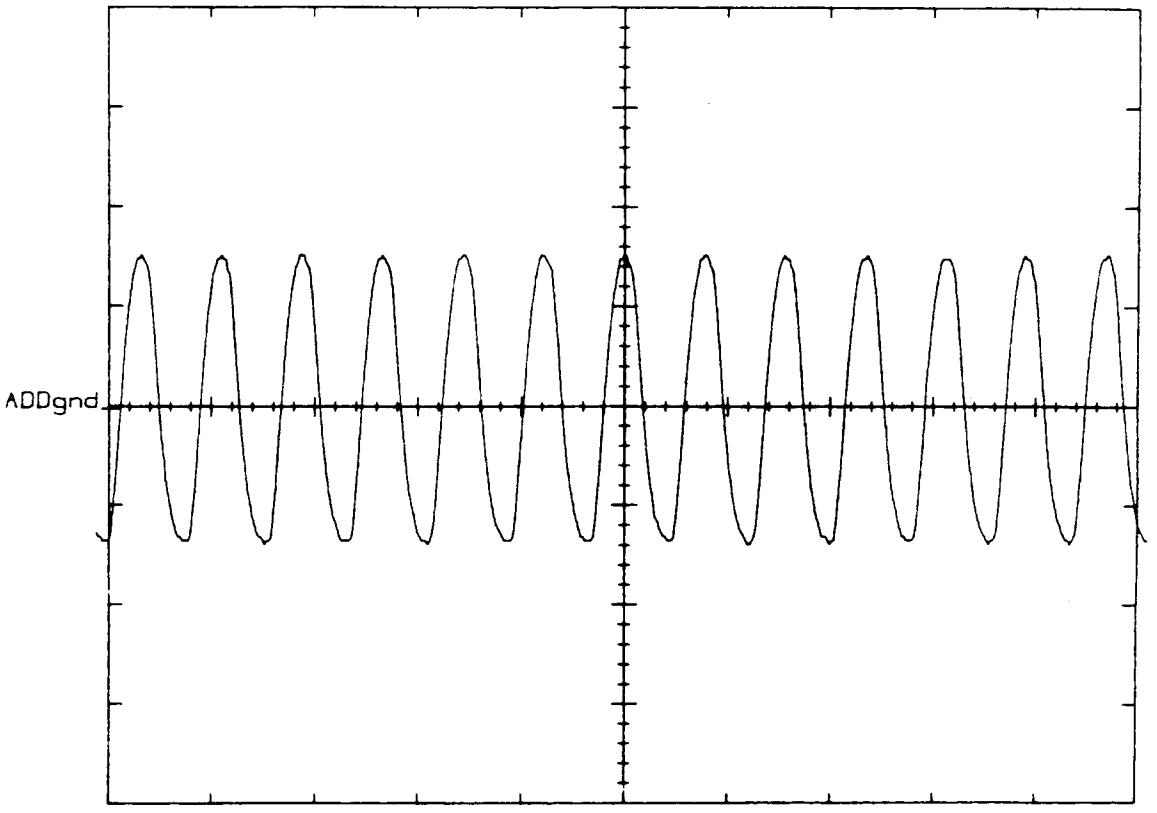


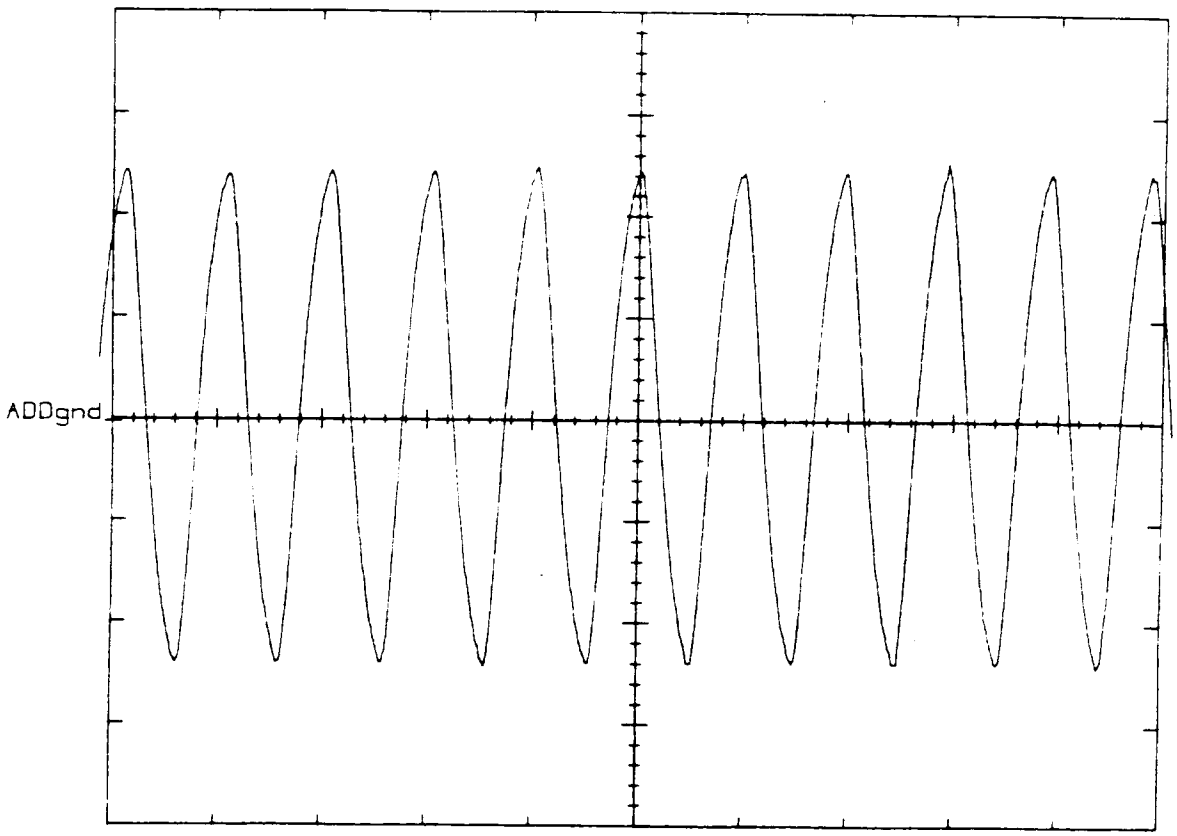
Fig. 17a - 64-kHz AHG4 Output Waveform

the 2.048 MHz base frequency. This frequency is next input to a Class A wave shaper/amplifier that produces the sine wave shape. This signal is fed into an unbalanced output transformer which is impedance matched for a 75 ohm load. Lastly the signal is input to a settable attenuator that allows either a -20 dBm or -35 dBm output level to be output from the TD.

4.17 A faceplate Bantam test jack provides an access port to evaluate the 2.048 MHz sine wave frequency (fig. 20). The test port is separate and buffered from the main output. The test port level is +10 dBm +/- 1 dBm into 75 ohms unbalanced.

4.18 The TD also employes an output "cut off" feature. In the event of a dual-TI input failure, the TD disables its outputs and allows the synchronized equipment to enter a holdover mode at its prescribed Stratum level.

4.19 There are three LED indicators on the TDs faceplate. Two of these indicators (TI OUTPUT IN USE) are green and are used to signify which input source is being used to derive timing (TI A or TI B). If there is a CUT OFF alarm, these LEDs are inhibited as this alarm state prevents any inputs from being used. The last of the LED indicators is the red CUT OFF LED which is used to signify the loss of input, loss of lock, or the external "cut off" command.



NOTE: OSCILLOSCOPE SETTING
CH1 500 mV A 2 us
CH2_ 500 mV
ADD 500 mV

Fig. 17b - 512-kHz AHG4 Output Waveform

F. AHG26 TD OPTIONS

4.20 The selection of the output level is the only TD option. The two output levels are -20 dBm or -35 dBm. The two levels are set by a slide switch located at the bottom left of the circuit pack (fig. 21).

4.21 The TD is intended to be used in non-redundant applications and need not be used in pairs. When used in the CDU, the TD is normally placed in slot TD1 (side A) or slot TD4 (side B). If, however, there are to be other non-redundant circuit packs used in the panel (ie. AHG4) then slots TD1, TD2, TD3, or TD4 may be used.

4.22 An output cable must be run between between the TD and the SDE terminal blocks. The cable will be a twisted pair with three twists per inch. The wiring assignments are given per TD slot assignment. Coaxial cable is used to cable from the SDE() terminal blocks to the designated NE. A 728A or equivalent coaxial cable is recommended.

G. AHG1 TA

4.23 When a plug-in unit in the CDU detects a signal failure, a fault indication is sent to the TA. The block diagram for the AHG1 TA is shown in fig. 22. The TA activates the fuse and alarm panel which provides relay contacts for activating audible

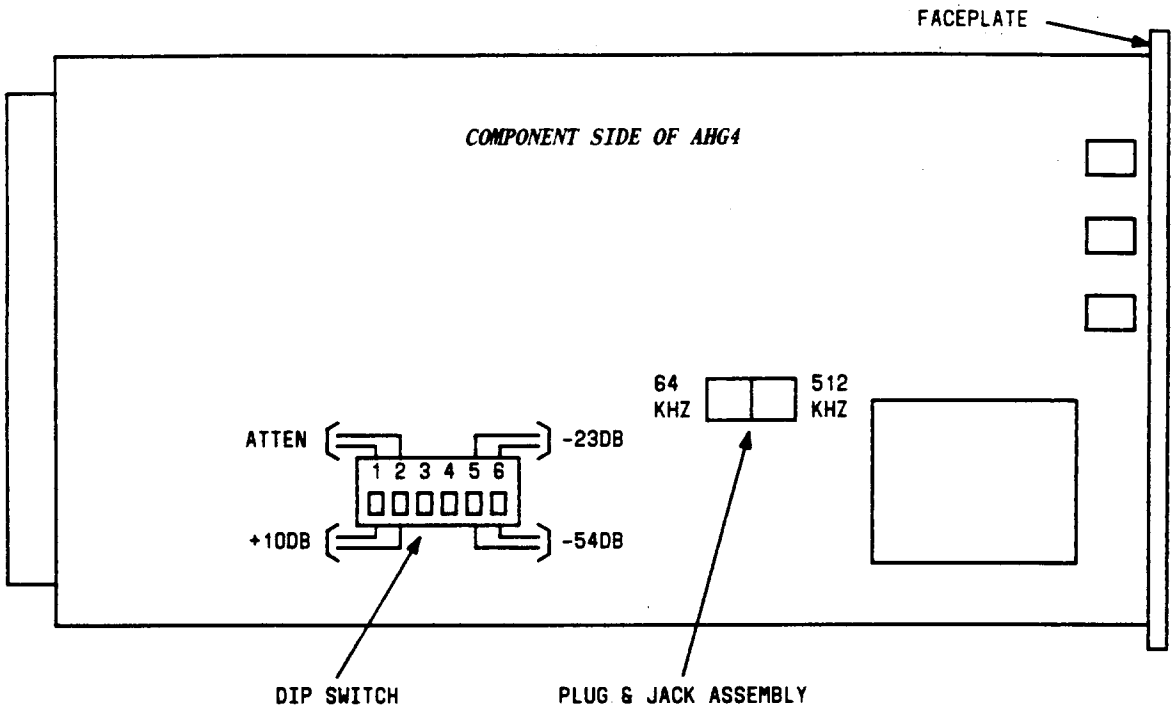


Fig. 18 - Location of Options for the AHG4 Timing Distributor

visual, and status reporting alarms. The LEDs on the TA indicate which unit or units are in trouble. The option (shorting) plugs (fig. 23) on the TA are for preventing alarms coming from unused TD positions. An option plug is inserted in the position below the IN position corresponding to the number of the TD position not being used. There is no alarm defeat for TD position one since at least one TD is required for an operational CDU. The lamps on the fuse and alarm panel indicate if a trouble is minor, major, or due to fuse or battery failure. The locking ACO (alarm cut-off) switch is used to silence the audible alarms while the visual and status reporting alarms are registered. When activated, the ACO switch lights. After a fault is cleared, the alarm registration indicated by lighted LEDs is cleared by momentarily operating the nonlocking MEM (memory) switch. All the lamps on the fuse and alarm panel are automatically extinguished when the fault is cleared, except the lighted ACO switch, which must be pressed to extinguish. Table C summarizes the locations and classes of alarm indications that appear for different types of CDU malfunctions.

4.24 Power alarms may be registered in several ways. If one of -48V A or B battery feed fuses blows, the fuse and major alarm indication on the F & A (fuse and alarm) panel will light and a major office alarm will be reported. If the -48V ABS fuse blows, then only the fuse alarm will light on the F & A panel and both major and minor office alarms will be reported. If any two battery feeds fail, then a major office alarm will be registered. A summary of the power failure alarm responses may be found in Table C.

TABLE C

ALARM RESPONSES IN THE CDU

TIMING OR ENERGY SOURCE	FAILED UNIT	ALARM SENSOR LOCATION	OFF ALM & STATUS	ACO	LAMP/LED LOCATION		BACKUP
					FUSE PANEL	TA	
16.384 MHz (A) or DS-1 (A) or 2.048 MHz (A)	TI A	TI A TD(1,3)	MJ	Audible	MJ	TI A TD1 TD3	None
16.384 MHz (B) or DS-1 (B) or 2.048 MHz (B)	TI B	TI B TD(2,4)	MJ	Audible	MJ	TI B TD2 TD4	None
16.384 MHz (A&B) or DS-1 (A & B) or 2.048 MHz (A&B)	TI A and TI B	TI (A,B) TD(1,2,3,4)	MJ	Audible	MJ	TI A and TD(1-4) TI B	None
TI (A & B)	TD-1	TD-1	MJ	Audible	MJ	TD-1	None
TI (A & B)	TD-2	TD-2	MJ	Audible	MJ	TD-2	None
TI (A & B)	TD-3	TD-3	MJ	Audible	MJ	TD-3	None
TI (A & B)	TD-4	TD-4	MJ	Audible	MJ	TD-4	None
-48VABS	Fuse F1	Fuse panel	MJ		MJ, FA	None	None
-48VABS	-48ABS	Fuse panel	MJ,MN	None	None	None	None
-48VA	Fuse F2 or -48A	Fuse panel	MJ	Audible	MJ, FA	None	F3 (-48V B)
-48VB	Fuse F3 or -48B	Fuse panel	MJ	Audible	MJ, FA	None	F2 (-48V A)

H. AUXILIARY PANEL EXPANSION

4.25 The AHG16 and AHG27 TIs have the capability of being able to support up to two auxiliary CDU panels from the main panel which they are located (fig. 24). The auxiliary panel configuration is compatible with the J98726Z-1 panel. The auxiliary panels act as an extension of the main panel allowing the number of available output taps to be increased by a factor of two (with one auxiliary panel) or by a factor of three (with two auxiliary panels). Because placement of the auxiliary panels must be no greater than a six foot cabling distance to the main panel, their intended use is to achieve a concentrated timing distribution arrangement.

4.26 An auxiliary panel is comprised of only a single TA and up to four TD circuit packs. Input signals to the auxiliary panel come directly from dedicated output taps on the AHG16 in the main panel, thereby eliminating the need for TI circuit packs on each auxiliary panel. These output taps are accessed

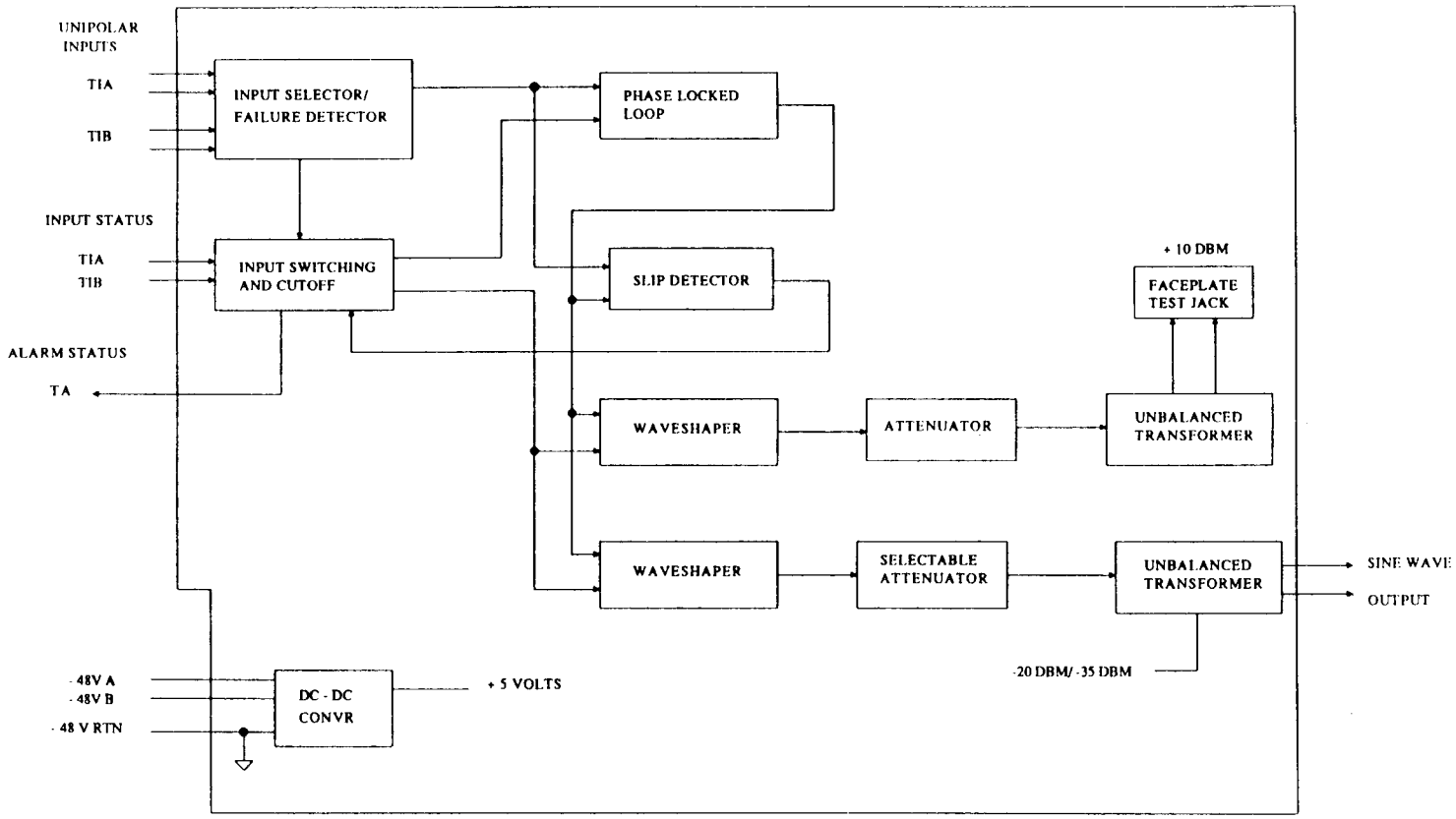


Fig. 19 - Block Diagram of AHG26 Timing Distributor

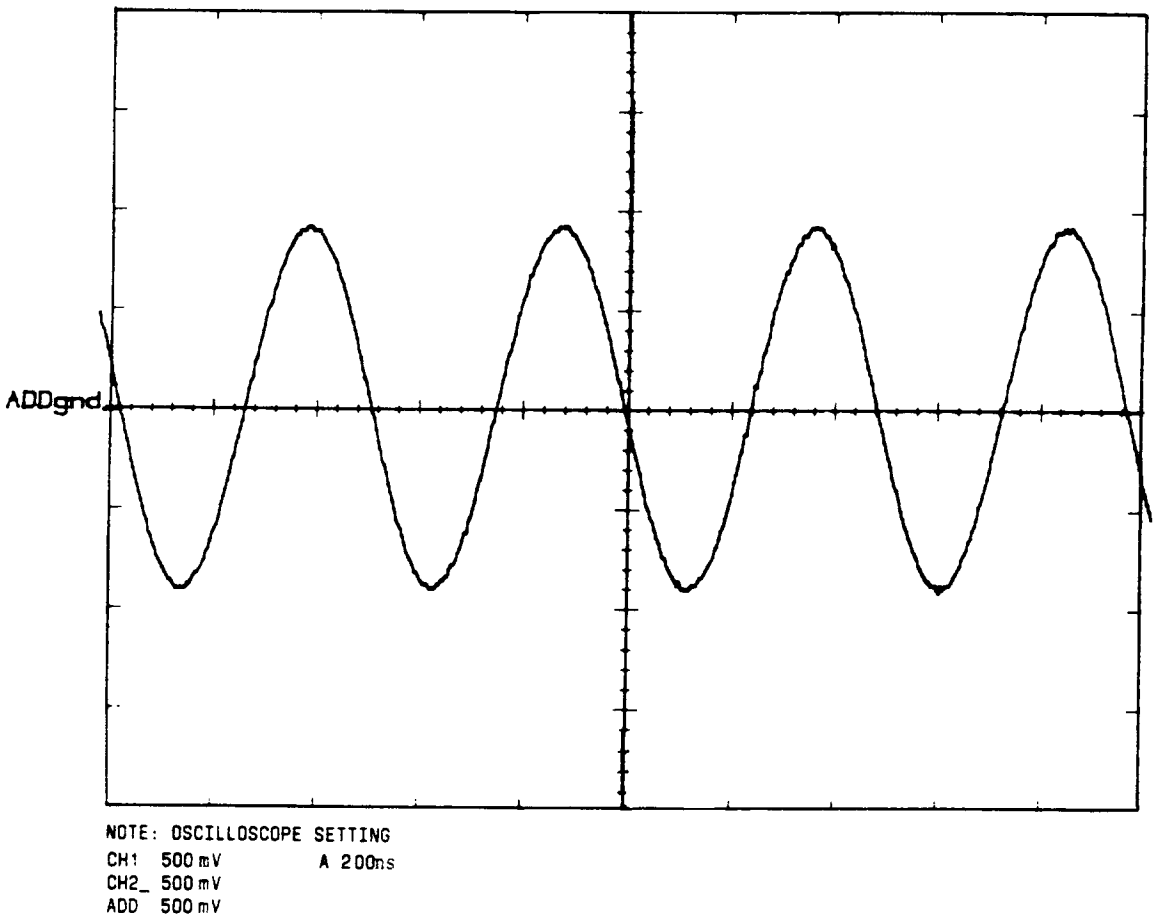


Fig. 20 - AHG26 TD Faceplate Jack (2.048 MHz at +10 dBm)

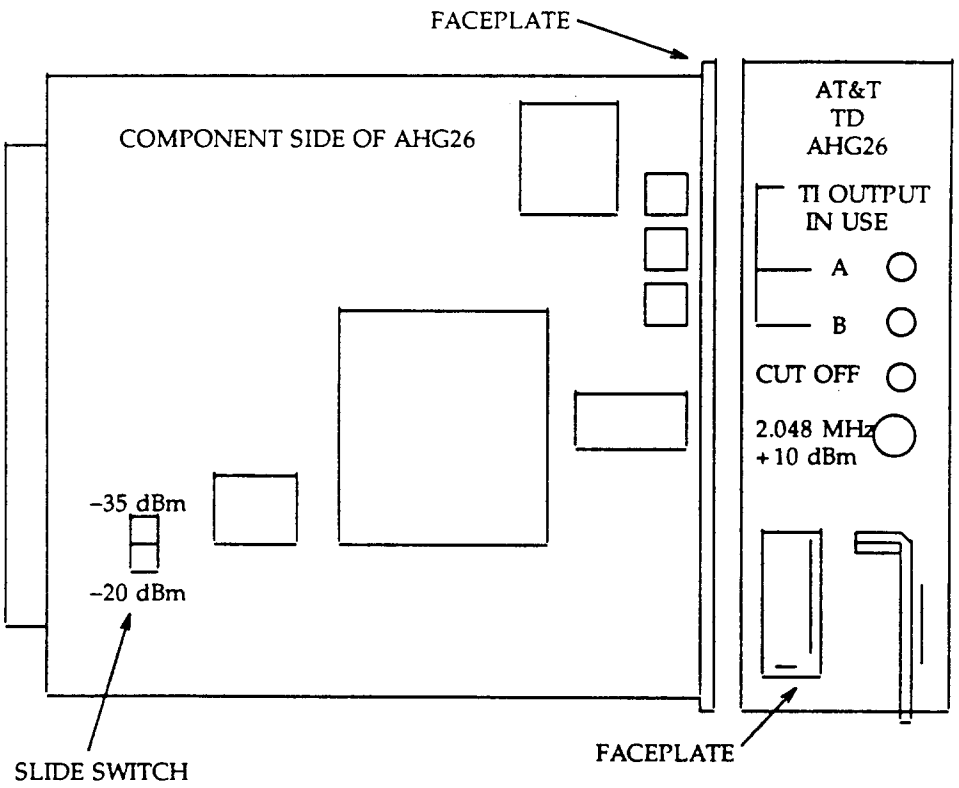


Fig. 21 - Location of Options on the AHG26 TD

through wiring a series of 26-gauge twisted pairs in a common shield from the backplane connectors for TI A (J2) and TI B (J3) on the main panel to the respective backplane connectors for TI A (J2) and TI B (J3) on the auxiliary panel (Table D). The shield is connected to the main panel and left unconnected at the auxiliary panel in all cases. As an ESD precaution, it is recommended that dummy board ED-8C715 (or equivalent) be placed in the vacant TI slots of the auxiliary panel.

4.27 Each auxiliary panel is separately powered and alarmed so that redundancy of the main and auxiliary panels is preserved. There is no additional throughput delay of the output CDU signals contributed by the auxiliary panels. Therefore, the auxiliary acts as an extension of the main panel.

I. POWER

4.28 The CDU is powered from three separate -48 volt dc office battery feeds. Each battery feed is run separately from the power distribution panel. All battery feeds are protected by separate fuses located on the faceplate of the F & A panel. Both of the battery feeds (-48V A and B) supply power to each circuit pack in the CDU. If one of the redundant battery feeds fails, a steering diode circuit located in each circuit pack will automatically switch to the other good battery feed. The steering diode arrangement provides the input voltage for a dc-dc power converter that supplies each circuit pack with its own source of filtered and regulated 5 volt power for circuit operation. The third -48 volt battery feed (-48V ABS) is used to supply power to the F & A panel for lamp and relay operation.

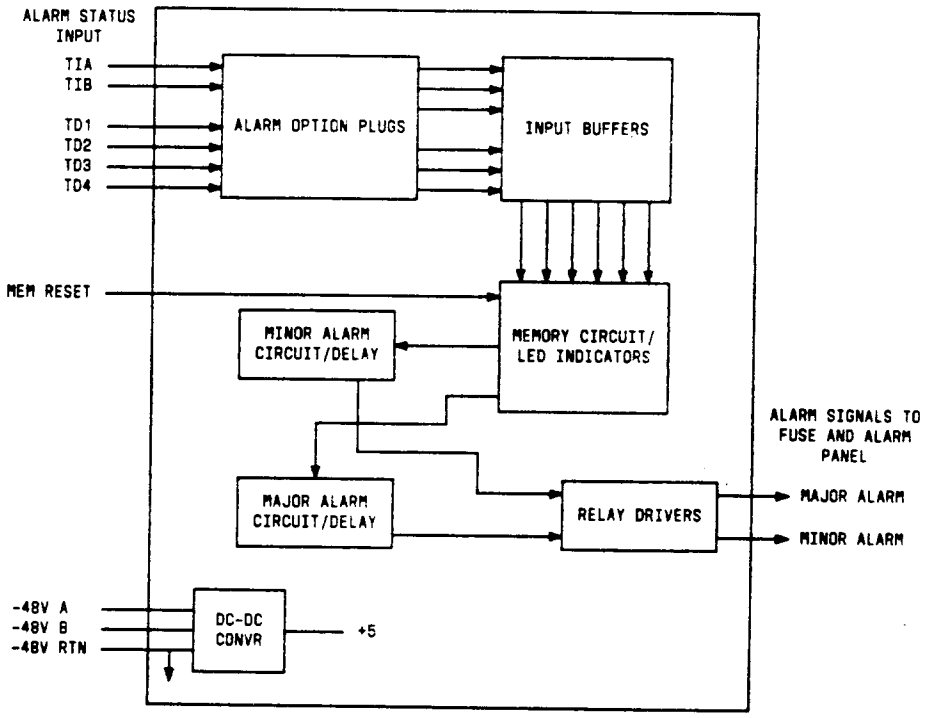


Fig. 22 - Block Diagram of Timing Alarm (AHG1)

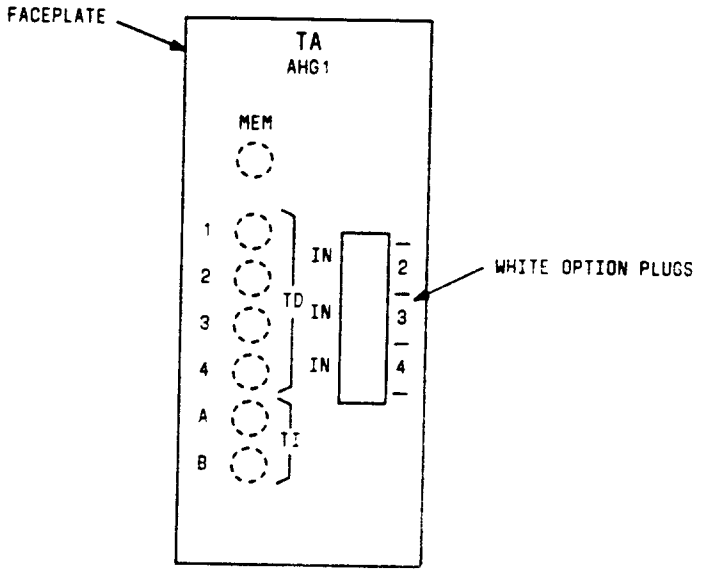


Fig. 23 - Location of Options for the AHG1 Timing Alarm

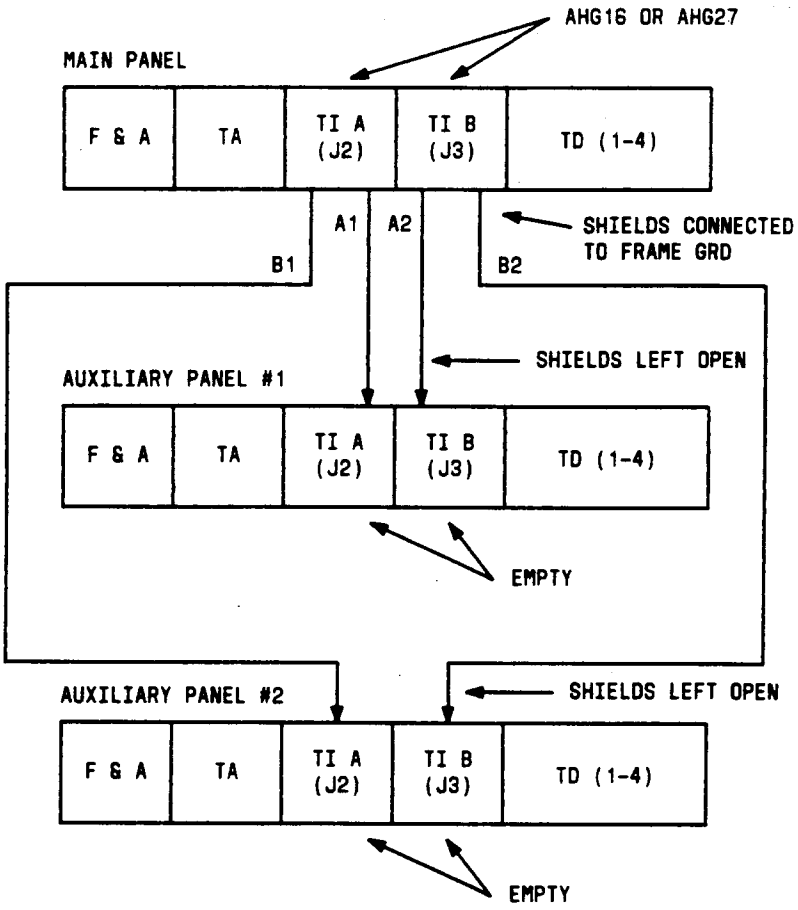


Fig. 24 - Cabling Diagram Showing Wiring Between Main and Auxiliary Panels

TABLE D (NOTES 1 AND 2)
CABLING CONNECTIONS FOR AUXILIARY PANELS

FROM MAIN PANEL		TO AUXILIARY PANEL #1 (NOTE 3)		
CONNECTOR	TERMINALS	CONNECTOR	TERMINALS	CABLE
J2 (TI A)	15	J1 (TA)	2	A1
J2 (TI A)	7	J2 (TI A)	3	A1
J2 (TI A)	34	J2 (TI A)	30	A1
J3 (TI B)	15	J1 (TA)	3	A2
J3 (TI B)	7	J3 (TI B)	2	A2
J3 (TI B)	34	J3 (TI B)	29	A2
FROM MAIN PANEL		**TO AUXILIARY PANEL #1 (NOTE 3)**		
CONNECTOR	TERMINALS	CONNECTOR	TERMINALS	CABLE
J2 (TI A)	42	J1 (TA)	2	B1
J2 (TI A)	8	J2 (TI A)	3	B1
J2 (TI A)	35	J2 (TI A)	30	B1
J3 (TI B)	42	J1 (TA)	3	B2
J3 (TI B)	8	J3 (TI B)	2	B2
J3 (TI B)	35	J3 (TI B)	29	B2

*Note 1:*Each auxiliary panel is fed by two shielded cables (A1 and A2 for auxiliary panel #1 and B1 and B2 for auxiliary panel #2). Each cable contains three twisted pairs of 26-gauge wire.

*Note 2:*The shield connection is tied to frame ground on the main panel, but not connected on the auxiliary panel.

*Note 3:*The maximum overall cable length for each auxiliary panel should not exceed 6 feet.

5. REFERENCE INFORMATION

A. PUBLICATIONS

5.01 The following publications provide more information on the CDU:

- T-7C389-33 Issue 5 (or higher)
- SD-7C389-02 Issue 3 (or higher)
- AT&T Practice 314-813-201 - Clock Distribution Unit - Installation and Maintenance
- AT&T Practice 314-913-222 - Data Sheet - AHG1 Timing Alarm
- AT&T Practice 314-913-223 - Data Sheet - AHG4 Timing Distributor
- AT&T Practice 314-813-102 - Data Sheet - AHG16 Timing Interface
- AT&T Practice 314-913-228 - Data Sheet - AHG25 Timing Distributor
- AT&T Practice 314-813-103 - Data Sheet - AHG26 Timing Distributor
- AT&T Practice 314-813-104 - Data Sheet - AHG27 Timing Interface

B. GLOSSARY

5.02 Terms used in this document are identified as follows:

- **CDU:** Clock Distribution Unit
- **CTS:** Composite Timing Signal
- **DACS:** Digital Access and Cross Connect System
- **ESD:** Electro-Static Discharge
- **IN FAIL:** Input Failure
- **IN SCE TR:** Input Source Transfer
- **LED:** Light Emitting Diode
- **PFS:** Primary Frequency Supply
- **PLL:** Phase-Locked Loop
- **TA:** Timing Alarm Circuit Pack
- **TD:** Timing Distributor Circuit Pack
- **TI:** Timing Interface Circuit Pack
- **TST:** Test Access Jack
- **4ESS:** Number 4 Electronic Switching System
- **TST:** Test Jack

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