AUTOMATED BIT ACCESS TEST SYSTEM (ABATS)
DESCRIPTION AND OPERATION
DIGITAL DATA SYSTEM

CONTENTS PAGE

1. GENERAL

1.01 This section describes the Automated Bit Access Test System (ABATS), which is a remote testing system capable of testing bidirectionally on the Digital Data System (DDS). It replaces the 950-type testboard.

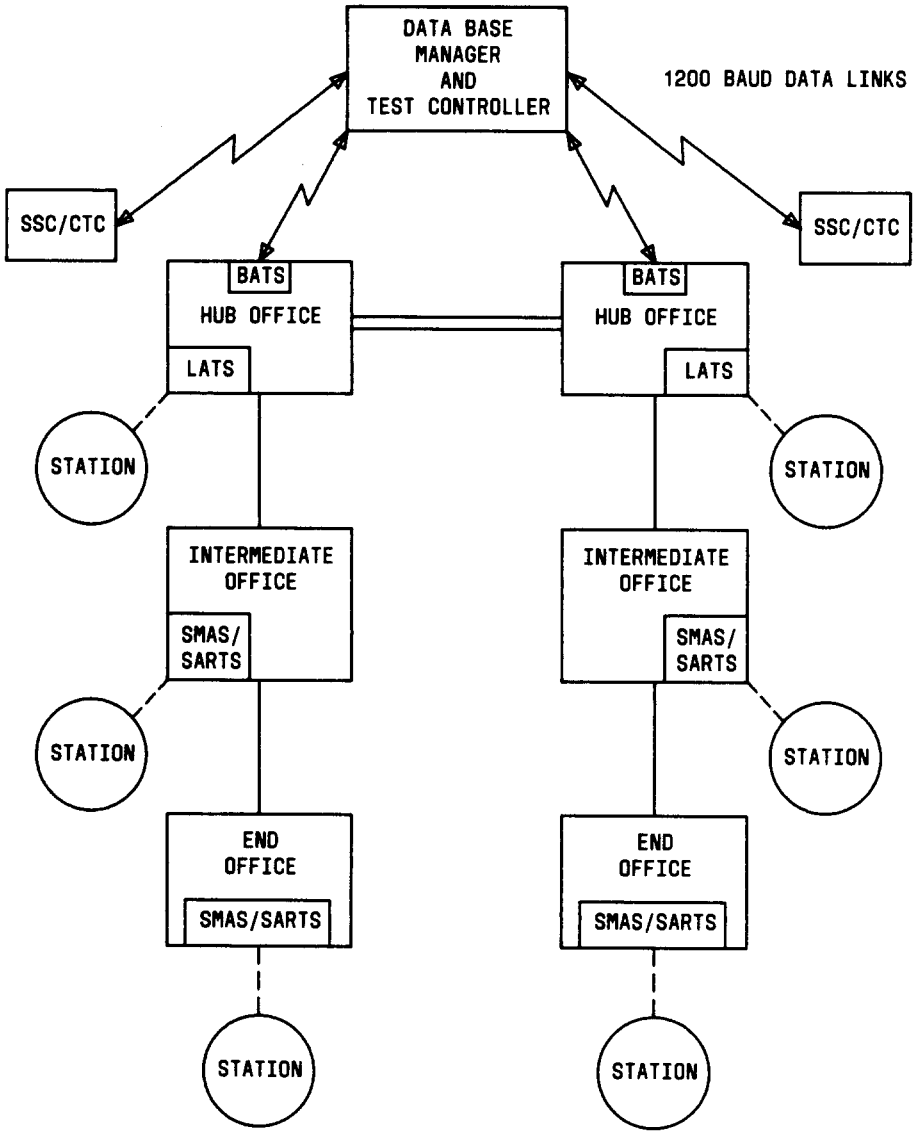
1.02 Whenever this section is reissued, the reason(s) for reissue will be given in this paragraph.

1.03 Figure 1 shows ABATS used in a simple DDS configuration. The data base manager and test controller (DBM and TC) is linked to each DDS hub office and/or Special Service Center/Centralized Test Center (SSC/CTC) via a dedicated 1200 baud data link.

1.04 Figure 2 shows a more detailed configuration of the DBM and TC location. The equipment inside the broken line box is backup equipment which provides for high reliability. A duplicate copy of the system and data base is kept on a second disk so that system downtime due to trouble or during routine maintenance will be minimal.

1.05 The SSC/CTC enters commands via a DATASPEED® 40/2 terminal set (keyboard, display, and printer) to gain access to ABATS. The commands activate the programs. The programs access the memory of the stored information. In ABATS, the data base information is entered by SSC/CTCs. The data base update procedures are documented in Section 314-901-532. The remote test procedures are documented in Section 314-901-531.

1.06 Figure 3 shows an ABATS arrangement at a DDS hub office. The ABATS provides access at the DS-1 level (1.544 Mb/s), at the DS-0A level (64-kb/s), or to customer loops. At the DS-1 level, access to individual customer channels is derived by time



LEGEND:
CTC - CENTRALIZED TEST CENTER
SSC - SPECIAL SERVICE CENTER
BATS - BIT ACCESS TEST SYSTEM
LATS - LINE ACCESS TEST SYSTEM
SMAS - SWITCHED MAINTENANCE ACCESS SYSTEM
SARTS - SWITCHED ACCESS REMOTE TEST SYSTEM

Fig. 1—Simplified DDS Configuration Using ABATS

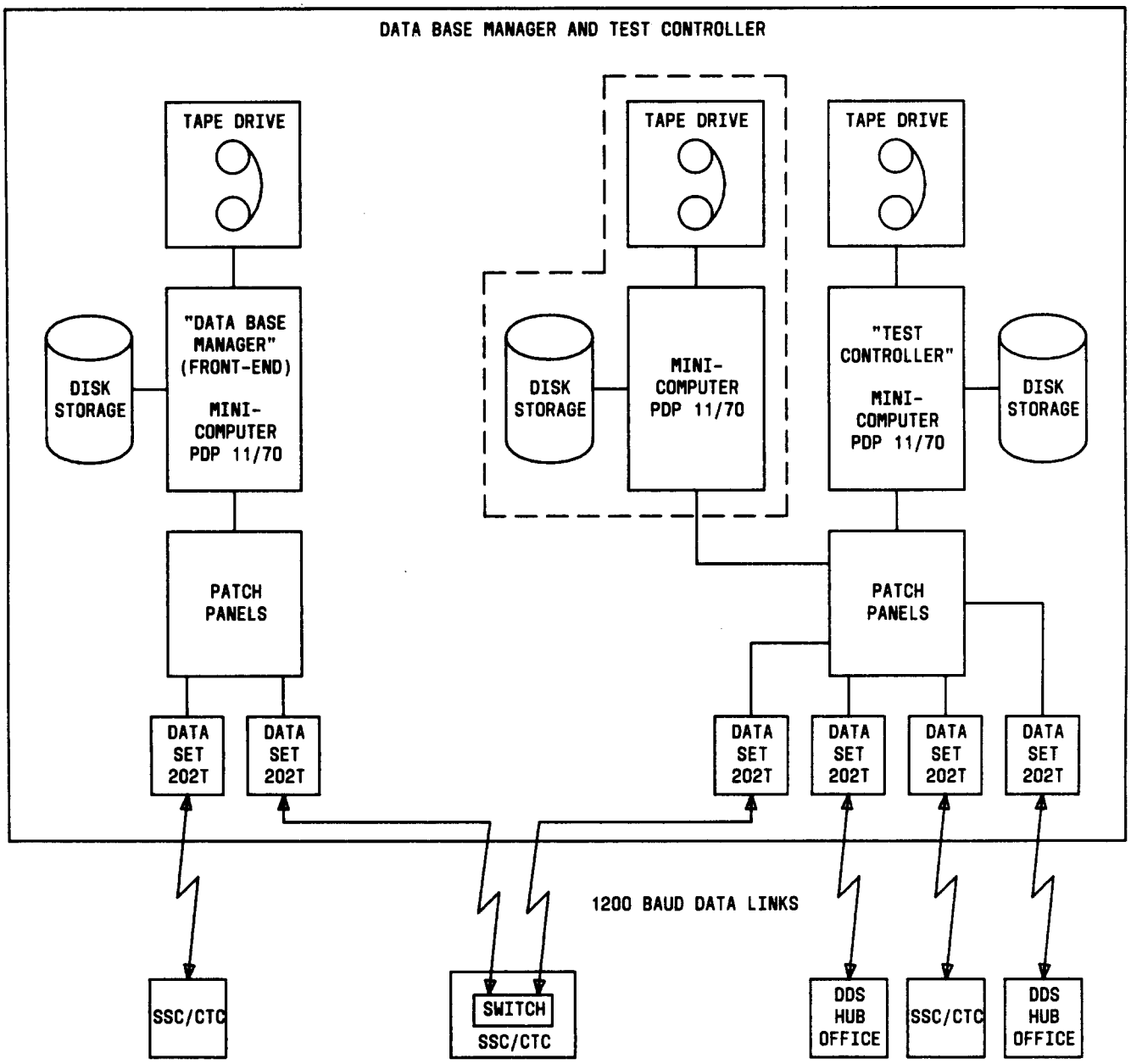
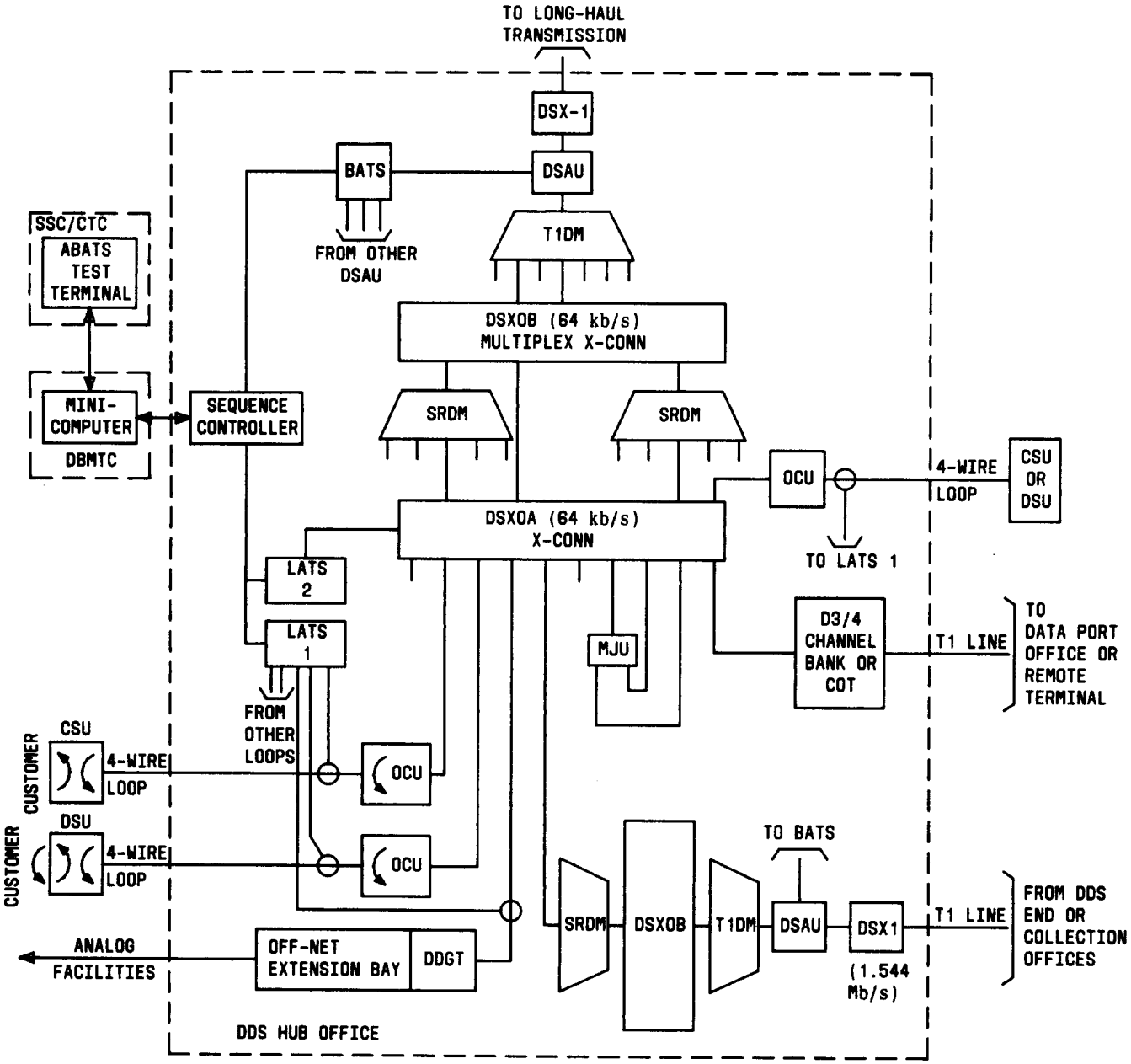


Fig. 2—Data Base Manager and Test Controller Configuration

division multiplexing/demultiplexing in a manner that duplicates the function of the primary and secondary data multiplex equipment in the normal transmission path with the exception that only the channel to be tested is made available. At the DS-0A level and to customer loops, test access is via a Line Access Test System (LATS).

1.07 Figure 4 shows the interconnections of the Bit Access Test System (BATS)/LATS equipment at a DDS hub office. The system consists of:

- A Microprocessor Sequence Controller (NJ01412A-1)
- A BATS or KS-21899 Data Test System (DTS)



LEGEND:

ABATS - DDS AUTOMATED BIT ACCESS TEST SYSTEM
BATS - BIT ACCESS TEST SYSTEM MEARSURES DIGITAL TRANSMISSION PARAMETERS TO AND FROM NEAR AND FAR CUSTOMER LOCATIONS
CSU - CHANNEL SERVICE UNIT
DSAU - DIGITAL SIGNAL LEVEL 1 ACCESS UNIT
DSX - DIGITAL SIGNAL LEVEL 1 CROSS CONNECT
LATS - LINE ACCESS TEST SYSTEM MEASURES VOLTAGE, RESISTANCE, AND CAPACITANCE OF 4-WIRE LOOP
MJU - MULTIPORT JUNCTION UNIT
OCU - OFFICE CHANNEL UNIT
SRDM - SUBRATE DATA MULTIPLEXER
T1DM - T1 DATA MULTIPLEXER
SSC - SPECIAL SERVICE CENTER
CTC - CENTRALIZED TEST CENTER
DBMTC - DATA BASE MANAGER AND TEST CONTROLLER
COT - CENTRAL OFFICE TERMINAL OF SLC96 SUBSCRIBER LOOP CARRIER SYSTEM

Fig. 3—DDS Hub Office Using ABATS/ALATS

- DS-1 Signal Access Unit (DSAU) shelves (J70177AW)

- A LATS by Data Products NE

The ABATS can be divided into two subsystems, BATS and LATS. When these two subsystems are accessed and controlled through the TC, they function as an integral part of ABATS.

1.08 The sequence controller (SC) that is located at a given hub office is connected to the TC located at a remote location to serve a given area. The 202T data sets are used to connect the SC and TC. The SC is cabled to the BATS and LATS control panels.

1.09 The KS-21899 DTS includes a shelf select unit for connecting to one of six DSAU shelves. A control panel provides displays and is used for manual operation of the system; refer to Section 314-901-530. Since each DSAU shelf provides 2-way access to 15 DS-1 signals, one KS-21899 DTS electronic unit can control access up to 90 DS-1 lines through one shelf select unit. It can also control a second shelf select unit if required and access up to 90 additional DS-1 signals.

1.10 The LATS control panel provides displays and can be used for manual control of loop testing. LATS is cabled up sequentially to 60 matrix units in any combination of Matrix I (loop access) and/or Matrix II (64-kb/s access) units. However, 64-kb/s Matrix II units are used only for access to customer signals which are not multiplexed to the DS-1 level for access with a DSAU.

1.11 The TC controls the operation of ABATS according to software application programs. The programs provide and store all circuit data information in its memory. The user enters the appropriate command at an ABATS test terminal for circuit testing. The TC minicomputer then transmits all of the necessary data for testing that circuit, including the type of test requested, to the SC at the appropriate hub office. Complete sequential end-to-end testing or specific DS-1, DS-0A, or loop testing can be requested and performed automatically or manually. Data generated by the KS-21899 electronic unit can be inserted on a DS-1 or DS-0A circuit for looping or straightaway tests. Voltage, resistance, and capacitance tests can be made on customer loops under direction of the SC or manually from the LATS control panel. A test system consisting only of line access test equipment under control of an SC and a TC can be implemented.

1.12 The SC acts as an interface between the functional equipment (BATS and LATS) and the TC. The SC contains a central processing unit and a memory and acts as a subcontrol unit for BATS and LATS under the overall control of the TC.

2. FUNCTIONAL DESCRIPTION

2.01 The primary function of ABATS is to localize malfunctions of an individual customer link. ABATS is also used in preservice testing to establish benchmarks. By routing each DS-1 signal through a DSAU, a selected channel can be monitored or any of the DDS test codes can be inserted on that channel. The SC will control the bit stream access equipment and report the results of the test to the TC. The TC will then display the test results to the operator on the ABATS test terminal. By entering an acceptable command, a circuit number, and any of the desired or required parameters at the test terminal, a customer circuit can be automatically accessed, monitored, and tested from near-end data service unit (DSU) or channel service unit (CSU) to far-end DSU or CSU within a few minutes. If a trouble happened to be in a DSU, it could be isolated in approximately 30 seconds. Thus a trouble condition can be localized more quickly with ABATS than with other methods previously used to test DDS.

2.02 A circuit is assigned an A end and a Z end. There is no relationship between A and Z and near-end or far-end. The designations A and Z end are used when performing the remote ABATS test procedures. The system tests toward the A end or the Z end. The designations near end and far end are used when performing the manual BATS test procedures.

2.03 In addition to the primary function, tests for error rate, verification of completed repairs, and installation of circuits can be made. Monitoring of channels, without interruption, can be done to determine if the channel is idle or unassigned and the data rate of the channel.

2.04 In addition to the loopback tests (performed by a single test facility), straightaway tests can be made with technicians using a 912, 914, or 921 data test set at a distant office; straightaway tests can also be made to a DSU loopback key. A series of progress messages will be transmitted to the operator as a test advances.

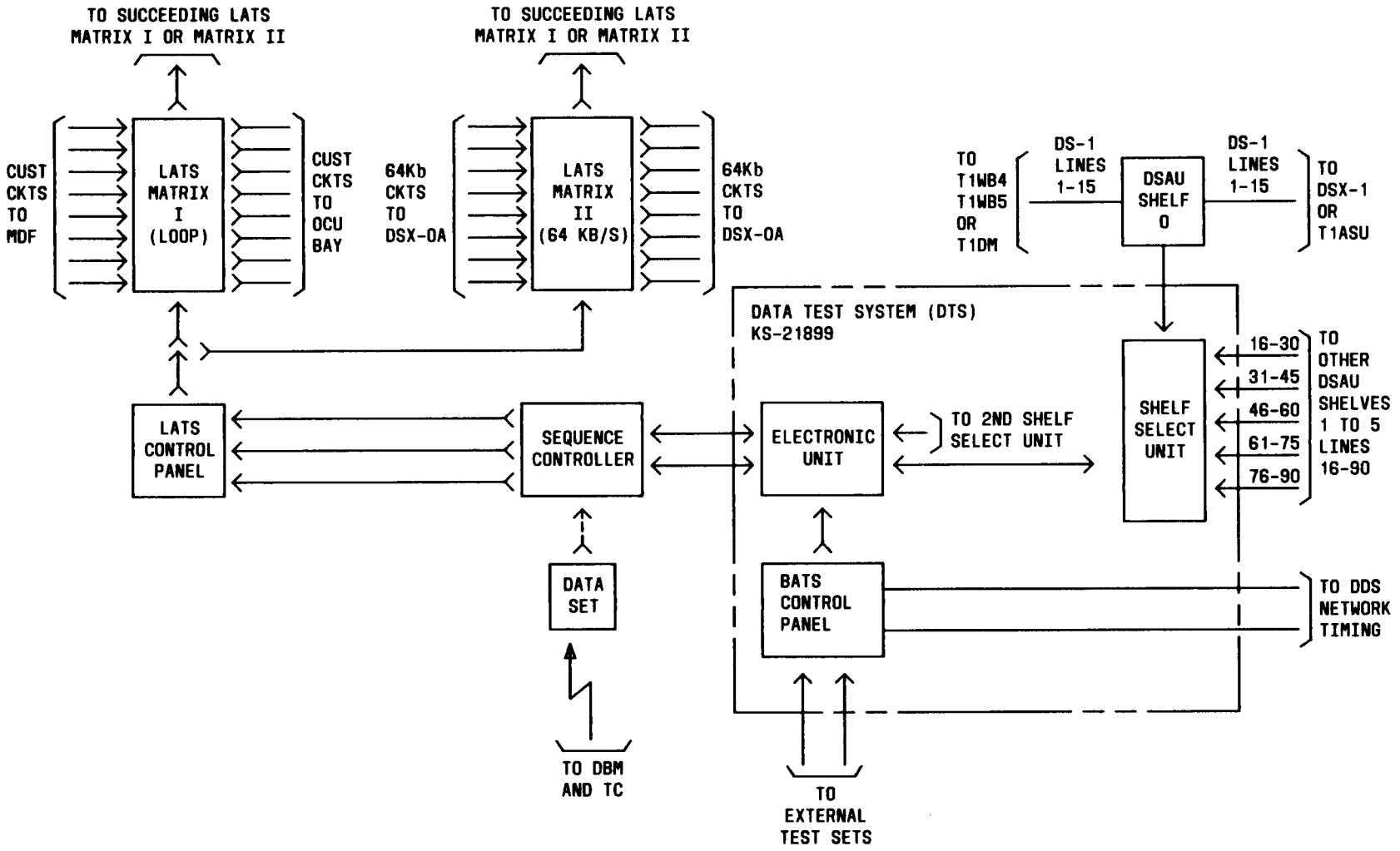


Fig. 4—Interconnection of BATS/LATS

2.05 When a trouble condition has been localized to the 4-wire local loop, the LATS equipment under control of the SC provides access to that 4-wire local channel to enable voltmeter testing. The LATS is used only on loops that terminate in hub offices. For loops that are not accessible by LATS, refer to the SSC for testing. A complete automatic voltmeter test consists of the following:

- Foreign Voltage Test—Checks for foreign voltage on the cable pairs at the serving central office.
- Insulation Resistance Test—Checks the resistance between the cable pairs and ground at the office channel unit (OCU) location in the serving central office (SCO).
- Loop Plus Terminal Resistance Test—Measures the sum of the resistance of the cable pair and the input resistance of the DSU or CSU.
- Open-Line Capacitance Test—Measures the capacitance of cable pairs that are found to be open.

The above tests are performed sequentially when the operator enters the VMT command and a circuit number. Also these tests may be initiated automatically during the normal sequence of events when the TST command is used (available March 1982).

2.06 Hub office to station tests performed by one employee at the ABATS terminal or by two employees between the station and the ABATS terminal can be done during installation and maintenance periods. These tests are referred to as directed tests. The 2-employee tests described in Section 314-901-530 require that the pairs be opened, shorted, or terminated at the station; thus, the DSU (or CSU) is removed from the local loop before these tests are performed.

2.07 On occasions, it may not be desirable to go through a complete series of tests from DSU to DSU. At these times, directed loopback testing of A-end or Z-end DSU, CHAN, or OCU can be done by entering the appropriate test command, circuit number, and direction parameter (A or Z). For example, to perform only a 15-second loopback at the Z-end OCU, enter the command LBO, the circuit number, and the parameters direction = Z and duration = 0.

Note: A duration time of zero provides a 15-second test period, and duration equal to one provides a 1-minute test period. When no duration parameter is used, time defaults to 15 seconds.

2.08 Parameters have been mentioned several times in the preceding paragraphs without definition. As applied to ABATS, a parameter is a character(s) used as an additional instruction to the TC. It instructs the TC to perform the specified test in a certain direction, for a specified time, and/or on specific leads. It is used primarily with directed tests. Refer to Section 314-901-531 for the required and optional parameters.

2.09 As a maintenance aid, progress messages are provided giving indications of various status and trouble conditions encountered during a test sequence. In addition, integrity checks are made each time the SC sends a command to the BATS or LATS equipment. If the BATS or LATS equipment fails to respond to the command, an error message describing the malfunction will be sent to the TC and to the operator terminal. Refer to the ABATS Input-Output Manual for a listing of the error and progress messages. Also listed are error messages that will be displayed to the operator if an incorrect test command or invalid parameter is entered at the ABATS test terminal.

3. EQUIPMENT DESCRIPTION

GENERAL

3.01 The ABATS equipment operates automatically under the direction and control of the TC. All data for the circuit to be tested is contained in the mass storage unit of the TC. The TC communicates directly with the appropriate SC, giving it test requests and information on the circuit to be tested. The sequence controller then handles the details of the test and notifies the TC of test status reports, failures encountered, and test results. The TC then displays various messages to the operator on the ABATS test terminal.

DS-1 SIGNAL ACCESS UNIT

3.02 The DSAU is an active device that is placed in series with the DS-1 line and located between the terminal equipment, eg, a T1DM and the DS-1 cross-connect (DSX-1). The DSAU, while transparent to the DS-1 signal, is capable of extracting timing information, regenerating the bipolar signal, and

detecting bipolar violations from both near and far directions. The unit presents the derived clocks and data through a buffered interface to the KS-21899 DTS. In addition, it provides appropriate alarm indications to the DTS when trouble conditions in the DSAU circuits are detected. The DSAU accepts test data and control signals from the DTS via interface circuits, which enable the DTS to insert data into one or more selected bits of the DS-1 signal stream.

3.03 The DSAU shelf houses a maximum of 15 DSAUs, each providing the electronics for access to a DS-1 signal, and a maximum of four bypass units, each providing the independent protection transfer paths for four DSAUs. In addition, the shelf houses an interface unit, a self-test unit, and a power converter unit. The interface unit contains the interface drivers and receivers and the office alarm circuitry, enables decoding, and verifies enable decoding logic. The self-test unit provides the means for testing the integrity of the interface between the DSAU shelf and the test equipment by simulating the normal operation of a DSAU with respect to the interface. The power converter unit is a dc-to-dc converter which accepts central office power (−48 volts) and provides power at appropriate voltages as required by all other units in the DSAU shelf. All units are provided as plug-in circuit packs to the shelf.

3.04 In conjunction with the KS-21899 DTS, the DSAU can perform self-testing by the use of a spare DSAU plug-in with input and output signals looped and a DS-1 signal generated by the DTS. Certain trouble conditions can also be isolated on the DSAU shelf by observing the states of certain interchange circuits to the DTS.

3.05 A complete description of the DSAU and auxiliary circuits is presented in Section 314-960-100. Maintenance and trouble locating procedures for the DSAU are provided in Section 314-960-300.

KS-21899 DATA TEST SYSTEM

3.06 The KS-21899L1 DTS provides the actual test functions for locating trouble that may result in a customer signal with excessive errors. This can be accomplished with access to customer signals at either the DS-1 (1.544 Mb/s) or DS-0A (64 kb/s) level for customer data rates of 2.4, 4.8, 9.6, or 56 kb/s. The DS-1 signal can be examined for bipolar violations, and test signals can be inserted into any selected channel and retrieved for comparison at these levels for isolation of troubles that may adversely affect a customer signal. The DTS consists of an electronic unit (EU) (KS-21899,L2), a control panel (KS-21899,L3), and a shelf select unit (SSU) (KS-21899,L4). It is normally operated under the control of the SC but can also be operated manually by controls on the control panel (called BATS). Test data can be transmitted from and received by DTS test logic or by an associated test set connected to the control panel or by the SC. Timing signals for operation of the DTS are provided to the control panel from the office timing supply. The DTS access to DS-1 signals is through the SSU, which connects up to six DSAUs providing full duplex access to up to 90 bidirectional DS-1 signals. Access to 180 DS-1 signals can be provided by adding a second SSU under control of the EU.

3.07 Access to DS-0A level signals by the DTS EU is provided through the SC, the LATS control panel, and appropriate LATS Matrix II units.

3.08 The primary functions of the control panel are to serve as a display for EU status data and to generate control data for EU operation. Status data is multiplexed at the EU into two bit streams, near and far, for transmission to the control panel. The status data is received by the control panel, demultiplexed, and stored to control the indicators and displays on the panel. Control data generated at the control panel is multiplexed into a single bit stream for transmission to the EU. Control data representing the state of control panel switch settings is received at the EU, demultiplexed, and stored to control the overall testing process.

3.09 Front panel jacks (miniature-type telephone jacks) allow the connection of external counters to monitor errors that can occur at a rate high enough to preclude transmission over multiplexed lines.

3.10 The control panel contains a 12-element touch pad with numerics of 0 to 9 and the functions of DS-0A and clear (CE). Pressing the DSO button places the EU in the DS-0A mode. The numerics are used for entering data, such as group, shelf, DSAU, data multiplex (DM) channel, and subrate data multiplex (SRDM) channel, into a register for transmission to the EU.

3.11 The EU contains the logic for controlling tests on a selected customer data channel for either

the DS-1 or the DS-0A level. Synchronization logic synchronizes internal T1 frame, and SRDM counters to the incoming T1 bit stream so that a particular customer data byte can be monitored and inserted at the correct byte time.

3.12 Data inserted for a selected customer channel interface (DS-1 or DS-0A) can be loopback codes, pseudorandom test patterns, multipoint signaling unit (MSU) command data, or block data from an SC or control panel dataports. Selection of the inserted data is made under EU control by the control data storage hardware. Data received by the EU from the selected customer channel is monitored for the occurrence of loopback codes. Pseudorandum codes are correlated in the EU, and errors are accumulated and displayed on the control panel.

3.13 Control and status data storage circuits in the EU contain the data for control of the overall customer channel test process. Control data consists of information identifying the settings of switches on the control panel in addition to other pertinent data, such as circuit select, test mode, customer rate, and test control. Status data storage is a source of status data for control panel or SC. Data held in status data storage gives the status, at any point in time, of the test process.

3.14 Inserted data to the DS-1 and DS-0A facilities is generated within the EU, with selection of the data determined by the test in process. Input data is received by DS-1 and DS-0A interfaces and distributed to external devices such as the SC and KS-21899 DTS.

3.15 A relay matrix interface in the EU allows for connection between the DS-0A customer interface and the DTS. A controller interface in the EU allows the DTS to be remotely controlled by the SC.

3.16 A station clock interface provides timing for data exchanges at a 64-kb/s rate between the DTS, test set, and DS-0A customer interface.

3.17 An SSU consists primarily of (1) logic for decoding and verifying a specific shelf address, (2) gating logic for routing the appropriate DSAU enable and signal information to a selected shelf, (3) data selectors for multiplexing signals from any of the six shelves onto common data lines to the EU, and (4) line drivers/receivers for appropriate interface and signal transfer capability between the SSU and the DTS EU or DSAU shelves.

3.18 In addition to routing the normal test or monitor data and control signals between the EU and the DSAU shelf, the SSU contains logic for transferring alarm, bipolar violation, self-test enable, and self-test verify information from and to the addressed shelf.

3.19 Descriptive information, installation procedures, operating procedures, and maintenance procedures for KS-21899 DTS are covered in Sections 107-605-100, 107-605-200, 107-605-300, and 107-605-500, respectively.

LINE ACCESS TEST SYSTEM

3.20 The LATS provides for centralized accessibility to individual customer 4-wire loops as well as to 64-kb/s circuits. Loop testing includes dc and ac voltage, resistance, and capacitance measurements. The 64-kb/s testing includes monitoring of customer DS-0A signals for errors and inserting signals for testing on a loopback or straightaway basis. The system consists of a control panel for operational control of loop testing and up to 60 Matrix I (loop access) and/or Matrix II (DS-0A access) units. Each matrix unit accommodates up to 80 customers. Testing is normally under control of the SC, with loop tests generated at the LATS control panel and DS-0A tests generated at the KS-21899 DTS, including multipoint junction unit (MJU) branch testing. Loop tests can be performed manually from the LATS control panel, and DS-0A tests can be performed manually from the BATS control panel. These manual tests will be preempted and terminated by the automatic tests.

3.21 When under manual control, the LATS control panel provides test controls and displays the identification of the circuit under test, the type of test being performed, and test results. When under control of the SC, all displays are blanked and controls disabled. The control panel also provides tip-ring jacks for access to external test sets for loop testing as well as for DS-0A testing with the KS-20908 and KS-20909 data test sets. DS-0A access can be made to both directions (near or far).

3.22 Matrix I units are connected between an OCU bay and main distributing frame (MDF). Matrix II units are connected at the DSX-0 cross-connect points in place of the 950 testboard.

3.23 The Matrix 1 unit (Fig. 5A) is a break only plug-in relay for each circuit to be accessed.

The Matrix II unit (Fig. 5B) is a monitor and break (two direction) plug-in relay for each circuit to be accessed. The monitor function is accomplished by operating relay K1 and performing tests on test bus A. The break function is accomplished by operating relays K1 and K2 simultaneously. Testing toward the line is accomplished on test bus A,and testing toward the equipment on test bus B.

3.24 The following paragraphs are concerned with LATS front panel controls and indicators for manual operation. The test procedures are given in Sections 314-901-530 and 314-901-531.

3.25 The LATS controls and displays (Fig. 6) function as follows:

- CIRCUIT SELECTION CONTROL/LED READOUT—A pushbutton keyboard assembly that is used for bay and OCU circuit call-up (when accessing the local loop) or for BAY/CKT (when accessing at the DS-0A level). Manual entry of the first 2-digit number selects the bay; subsequent entry of another 2-digit number sets up a particular circuit within that bay. The addressed circuit is displayed for verification by a light emitting diode (LED) readout above the keyboard assembly as each digit is entered.

- MIC—The micro-in-control indicator lamp, when lighted, signifies that the sequence controller is in control of the line access test system. In this mode of operation, all manual front panel controls are disabled, all lighted switches are extinguished, and the digital displays are blanked. Only while the MIC lamp is extinguished will manual operation of the test access system be possible.

- MON—Depressing the Monitor pushbutton switch (lighted while depressed) initiates connection of the LATS by activating the appropriate relays in the matrix unit to route via the Z-data bus the four wires, T, R pair and T1, R1 pair, of the addressed bay and circuit to the LATS test set (MM-100 test set unit). If the connection is made, eg, the FAULT lamp does not light, the MON switch remains lighted and cable pair measurements can proceed. Depressing the MON switch will only activate a Matrix II unit. If the MON switch is depressed when a Matrix I unit is addressed, the Fault lamp will light.

- BRK—Depressing the Break pushbutton switch causes the selected circuit to be broken at the matrix and the accessed leads to be connected to the central test panel. Matrix I operation brings the selected circuit to the front panel on the A bus. Matrix II operation brings both sides of the selected circuit to the front panel via the A and Z buses.

- FAULT—This red indicator lamp will light whenever the BRK pushbutton is depressed and the LATS fault monitoring circuitry detects that the matrix unit is not responding correctly, either because monitor was called for on a Matrix I unit or more than one matrix relay was about to be activated due to a wiring or system fault or because no circuit

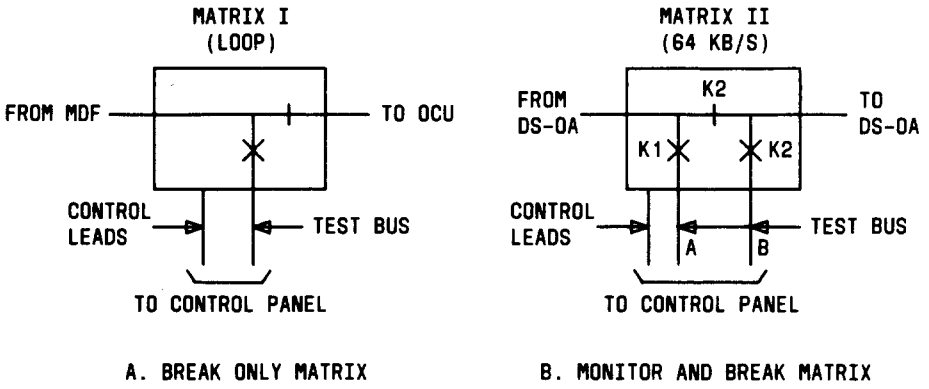


Fig. 5—Matrix Unit Configurations

matrix relay has been activated. As a precaution, detection of such a fault condition requires determination that the correct matrix was accessed or that off-line troubleshooting was undertaken to restore the access capability of the LATS to that circuit. The Fault light will clear when the circuit is released.

- RLSE—Depressing the Release pushbutton switch (lighted while depressed) disconnects the accessed circuit from the LATS test set and turns off the MON or BRK light. This switch must also be depressed to extinguish the FAULT light should a circuit access problem cause it to light.

- RLSE CKT—Depressing the Release Circuit pushbutton switch (lighted while depressed) blanks the 2-digit circuit address readout and releases the circuit under access; however, the selected bay 2-digit address remains intact. Manual entry of a 2-digit number selects a new circuit address in the same bay that may then be accessed by depressing the MON or BRK switch. The RLSE CKT switch is a convenience when testing more than one circuit in the same bay.

- EXT MEAS—Depressing the External Measure alternate (push-on, push-off) pushbutton switch (lighted while depressed) after a circuit has been accessed, routes the selected circuit to 8 pins on connector J3 on the rear panel of the LATS test set. This connection extends access to these lines for other testing purposes. While in the EXT MEAS mode, the selected circuit cannot be tested by the LATS measurement system nor can access be made through the front panel jacks.

- DIGITAL PANEL METER—Measurement data is presented on an easy-to-read digital panel meter which virtually eliminates any of the ambiguity or interpolation errors present in reading multiscaled analog meters. The display has the capability of presenting readings of 0 to 199 accompanied by decimel points between digits, a polarity sign prefix, and special overflow indication symbology (±OF) to inform the operator it is necessary to switch to the next higher measurement range.

- RANGE CONTROL—The range control is a multiposition rotary switch. Descriptions on the panel define which ranges can be used for a particular function.

- MTR ON—The meter is turned on with the pushbutton. The meter is automatically turned off whenever a circuit is released. This is to prevent a meter from inadvertently being placed across a circuit being monitored, which could under certain circumstances be undesirable. The meter cannot be turned on until after a circuit has been fully addressed. Only then will depressing the MTR ON switch activate the meter and light the switch.

- MTR RVS—The meter reverse pushbutton is an alternate action control which reverses the input connections to the meter. This is particularly useful in resistance measurements where diode-type action in the circuit being measured can only be detected with this feature. In the out or unactivated position, the meter polarity is as indicated on the front panel marking of the meter configuration LED indicator. When depressed and lighted, the meter polarity is reversed from that marked. It is important to note that for dc voltage measurements it is not necessary to reverse meter polarity as the meter measures and displays plus and minus voltages automatically.

- Function Control—The function control consists of four marked (VDC, VAC, RES, CAP) pushbutton switches that select the type of measurement to be made. These four switches are mechanically interlocked in a push-maintained arrangement so that only a single switch may be depressed at any one time. The button of the depressed switch is illuminated to highlight the function selection. The function selections are as follows:

  VDC—Selected for dc voltage measurements with full scale ranges of 19.9 Vdc and 199 Vdc.

  VAC—Selected for ac voltage measurements with full scale ranges of 1.99 Vac, 19.9 Vac, and 199 Vac.

  RES—Selected for dc resistance measurements with full scale ranges of 199Ω, 1.99 kΩ, 19.9 kΩ, 199 kΩ, and 1.99 MΩ.

  CAP—Selected for line capacitance measurements with full scale ranges of 199 nF, 0.199 μF, and 1.99 μF.

Note 1: All cable has a characteristic capacitance per mile, making it possible to determine the distance to an open or break by measuring its capacitance. On a typical cable having 0.083 μF/mile, the measurement would provide the distance to the fault with a resolution of 64 feet from 0 to 2.4 miles and 640 feet from 2.4 to 24 miles.

Note 2: Protection against accidental overloads to 130 rms volts is provided on all ranges.

- ZERO CHK—Depressing this pushbutton illuminates the marked button and initiates an internal self-checking mechanism which verifies the operational integrity of the test panel measurement circuitry by presenting an appropriate test display on the digital panel meter. The zero check operation should be performed for each of the 14 valid function/range measurement combinations before the LATS is going to be employed for measurement purposes. Acceptable meter display for any capacitance (CAP) range is +OF. For all other functions and ranges, the display should read between ±00 and ±05. If the meter indications are not in these ranges, the meter measurement circuitry is most likely in need of calibration or repair.

- Cable Pair Configuration Control LED Mapping—The cable pair configuration control consists of a set of ten marked pushbutton switches that select all the possible combinations of the T, R and T1, R1 circuit (any lead to any other or any lead to ground) as accessed with the matrix unit. These ten switches are mechanically interlocked in a push-maintained arrangement so that only a single switch may be depressed at any one time. The button of the depressed switch is illuminated to highlight the cable pair configuration selection, and a corresponding LED in the mapping structure above the switches is also illuminated to provide an alternate visual indication in a system perspective. The mapping also designates the polarity of the cable pair conductors relative to the test panel measurement system.

- Cable Pair External Access Jacks—Two 310 telephone tip-ring jacks enable the T, R and T1, R1 cable pairs that were selected with a Matrix I unit to be externally accessed from the test panel. Four mini-jacks and 8 pin-jacks are provided to the right of the map for simultaneous access to the A bus and the Monitor or Z bus. The 310 jacks are in parallel with the A bus mini-jacks. The meter should be left off if jack access is being used. Access through the jacks is not available if the EXT MEAS button is depressed.

MICROPROCESSOR SEQUENCE CONTROLLER (SC)

3.26 The NJ01412A-1 SC provides the microcomputer function to control testing of DDS circuits on direction from the TC. It consists of a central processor unit (CPU), random access memory (RAM) with a minimum storage of 2048 eight-bit words, a read only memory (ROM) that is programmable with a minimum storage of 8192 eight-bit words, eight input and eight output (I/O) ports, and five adaptive backplane system (ABS) circuits for connection to the KS-21899 electronic unit and the LATS control panel. Additional RAM and ROM circuit packs can be added to increase the memory capacity of the unit.

3.27 The SC acts as an interface between the functional equipment (BATS and LATS) and the TC. It acts as a subcontrol unit for BATS and LATS under the overall control of the TC. It acts much as a "subcontractor" to the TC in that it handles the details of a test request entered through the TC and reports test status and results to the operator through the TC. The front panel of the SC is shown in Fig. 7.

3.28 The SC is a small but complete computer. Figure 8 is a greatly simplified block diagram of the SC and shows the circuit pack (CP) number and CP slot positions, ie, AA, AP, BA, etc. The SC consists of plug-in circuit packs and a self-contained power supply operated from 117 Vac. The CPU function is provided by CP10 and is comprised of the Intel 8080 chip with additional buffering for the address and data bus, control signals, control for reading and writing RAM and ROM memories and I/O ports, a 2-phase clock for the 8080 chip, and interrupt control circuitry.

3.29 The RAM card (CP102) provides 2048 eight-bit words of random access storage and is used for scratch pad type storage. RAM can be read and writ-

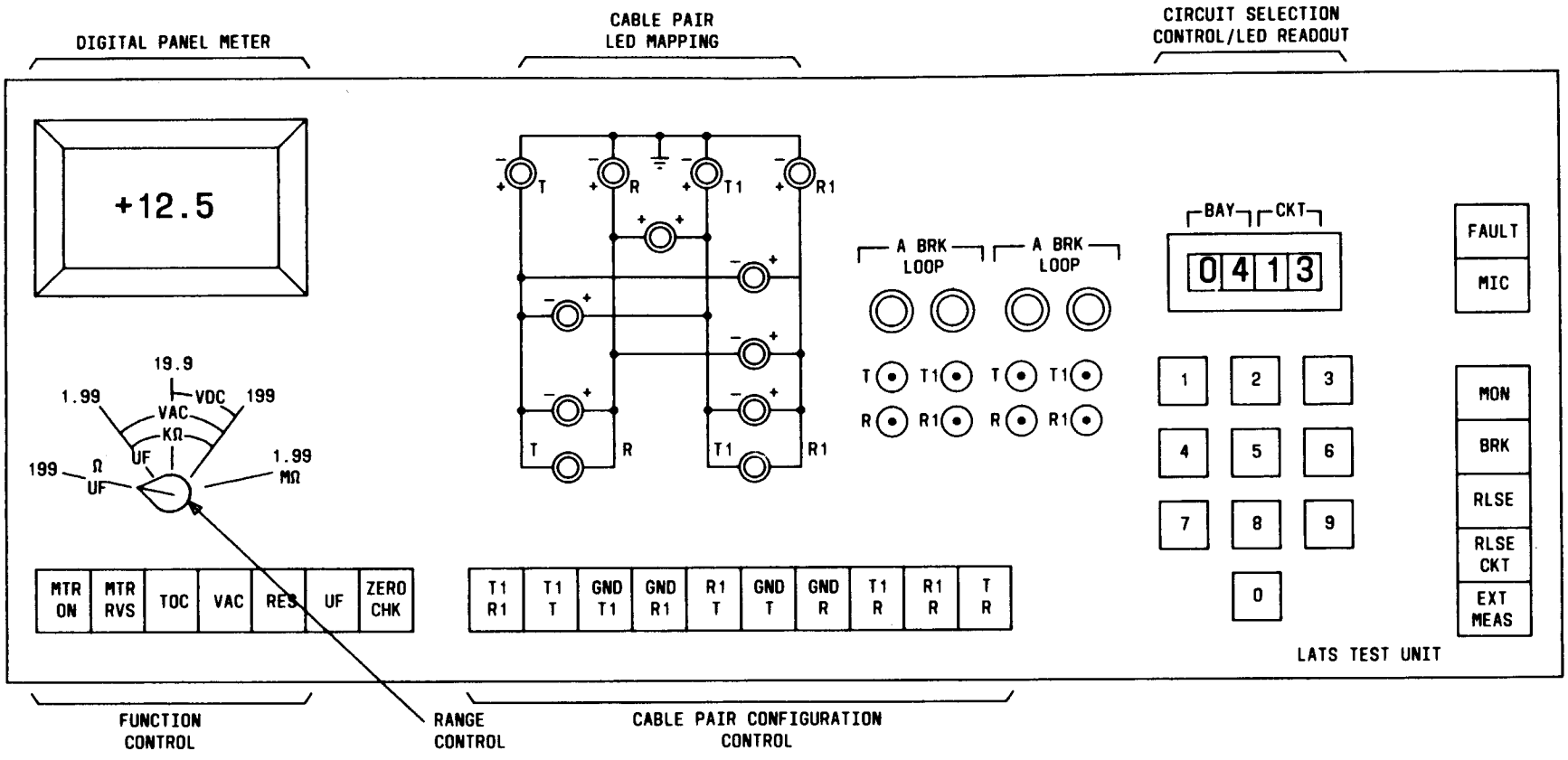


Fig. 6—Front View of LATS Control Panel

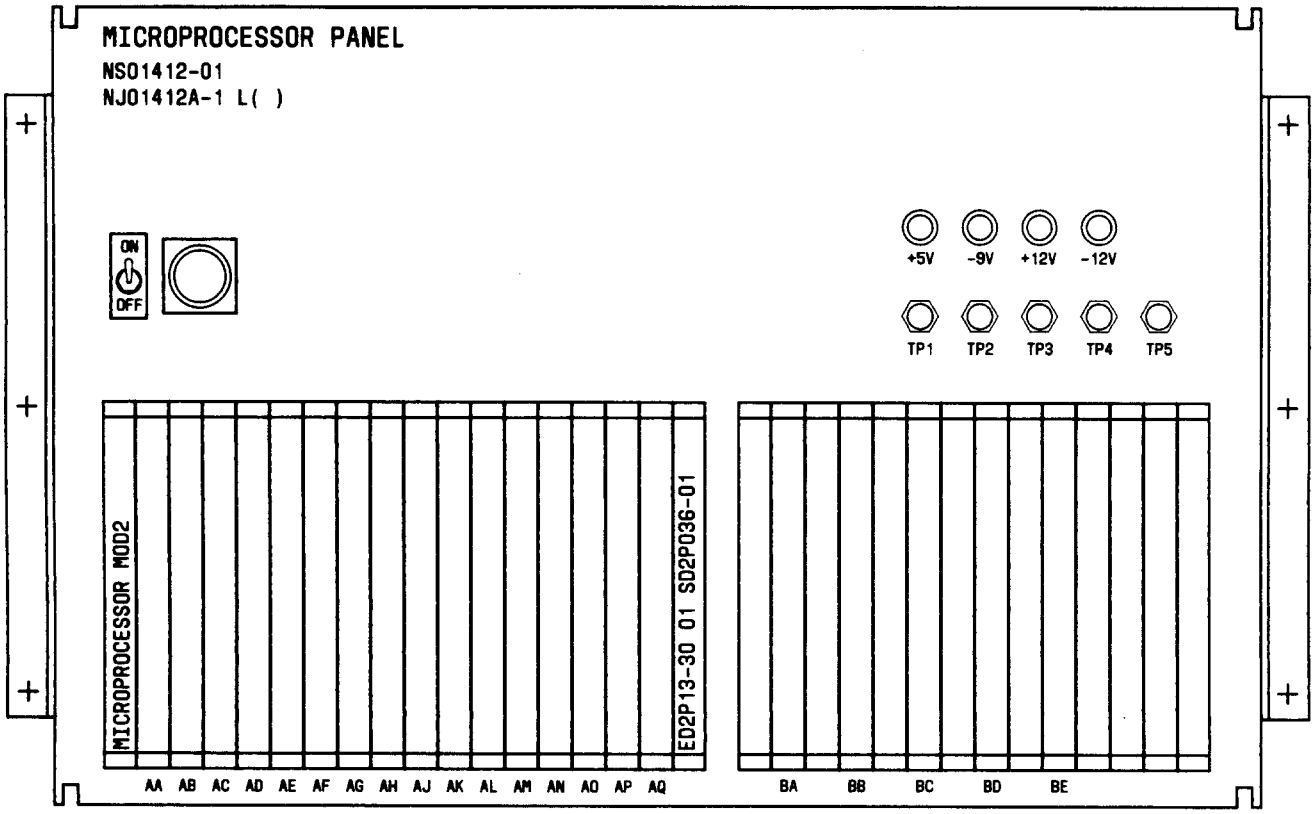


Fig. 7—Front View of Microprocessor Sequence Controller

ten by the CPU. One RAM card is provided initially, but additional cards can be provided as required.

3.30 The programmable read only memory (PROM) card (CP112) provides 8192 eight-bit words of read only memory using eight Intel 2708 erasable and programmable PROMs, each capable of storing 1024 words. One PROM card is provided initially, but additional cards can be provided as required.

3.31 The 4 by 4 I/O card (CP106) provides four 8-bit input and four 8-bit output ports. Two of these cards are required in each SC.

3.32 The dual serial EIA port card (CP11) provides two communications channels which can operate in either the asynchronous or synchronous mode. Each channel is treated as a peripheral device (in-out port) and can be programmed to provide any serial data transmission technique presently in use.

3.33 The programmable interrupt and timing card (CP12) provides a priority interrupt system for up to eight interrupt vectors and a programmable timer to set up required time intervals.

3.34 The adaptive backplane cards (CP13, 14, 15, 16, 17) provide a means of connecting I/O circuits from CP106 to external equipment via connectorized cables.

3.35 The SC panel includes a power supply to convert 117 Vac to the +5, −9, +12, and −12 Vdc required by the circuit packs for operation.

3.36 All SC circuit packs are interconnected by connectors mounted on a printed circuit backplane, which connects all pins on each connector having the same pin number together. Except for the two CP106 cards and the CP11 card, any card can be placed in any position in the basket. Another printed circuit backplane with connectors provides access from the adaptive backplane CPs to external cabling.

3.37 Drawing NS-01412-01 defines and controls the ABATS SC. The minimum configuration consists of one each of CP10, CP102, CP11, CP112, CP12, CP13, CP14, CP15, CP16, and CP17 and two each of CP106. Additional quantities of CP102 and CP112 can be added as required. The CP106 shall always be located in position AQ (I/O CKT #1) and AP (I/O CKT

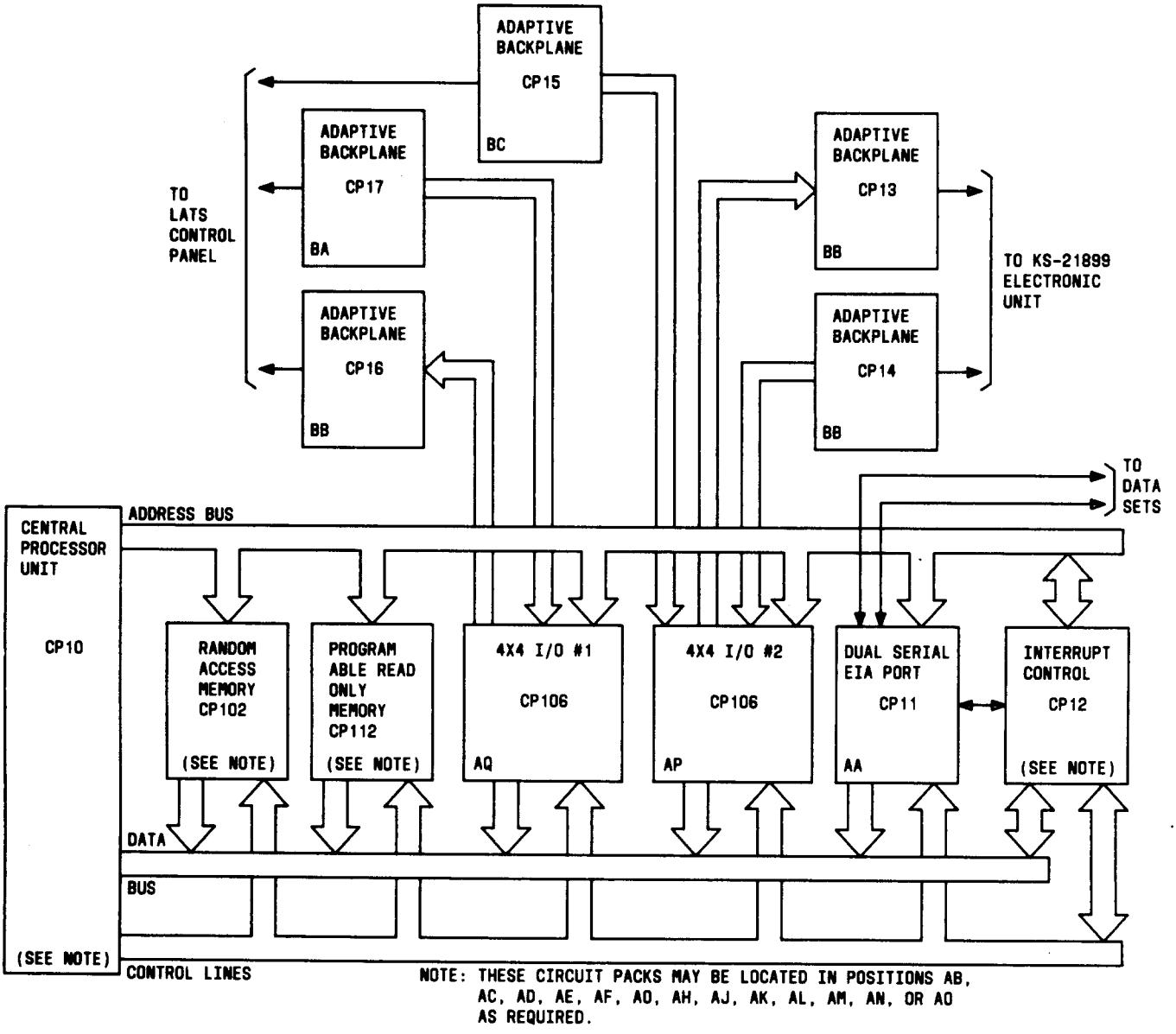


Fig. 8—Functional Diagram of Sequence Controller

#2), and CP11 shall always be located in position AA. Adaptive backplane system circuit packs shall always be located as shown in Fig. 8.

202T DATA SET

3.38 Data sets 202T or equivalent terminate the data link between the TC and the SC. The data set is located in the same bay with the SC. In an SSC/CTC testing application, the data sets terminate the links between the TC and the ABATS test terminals.

3.39 The data set accepts serial binary data from ABATS test terminal or the SC in the form of positive and negative dc voltage signals. The data set converts the signals to voice frequency tones which are transmitted over telephone facilities. At the dis-

tant data set, the tones are received, converted back to dc form, and delivered to the TC. For a detailed description of the 202T data set, refer to the 592 series sections.

4. OPERATIONAL FEATURES

GENERAL

4.01 This part describes the operational features of ABATS. All commands to the system are clear English or an easy to understand mnemonic. The commands are discussed in detail in Section 314-901-531. The messages exchanged between the system and the user or the SC and TC are listed in the ABATS Input-Output Manual. These messages are self-explanatory, but clarification is provided in the manual.

4.02 The BATS (part of ABATS) is provided with the capability to perform self-test and verification of its operation in an off-line condition without special purpose test equipment. Integrity check (INT CK) messages are also shown in the ABATS Input-Output Manual.

DATA BASE

4.03 Data base updates are allowed from the control console or the data base terminals. The control office is responsible for data base updates on its circuits. Data base updating procedures are presented in Section 314-901-532.

4.04 As much data information as possible is obtained through a direct connection to circuit layout (CL) (available March 1982). For example, when a new CL assigned DS-1 facility is to be established, the input from CL will tell the DBM to allocate a block of disk memory for this new facility. The rest of the block is then filled with a "data base not available" flag until the facility control office inputs the office dependent information. This allows the TC to return an error message to anyone that attempts to test a circuit before the data base has been brought up to date. This input information can also come from a central test location if for some reason the connection to CL is in trouble.

4.05 Generally the data base is stored in separate pieces: a master circuit list, a line facility (T1DM) record, a subrate multiplexer record (if applicable), and the local loop record (if applicable). The master circuit list contains all known circuits in the data base. The T1DM record contains the group, shelf, and DSAU assignment. The SRDM record contains the subrate multiplexer channel assignment (if the circuit is a subrate circuit). This information is needed by the KS-21899 data test system to access a given customer channel. Keeping separate records avoids the need to make changes to individual circuit records when there are changes in line facility.

4.06 In addition to the above access information, circuit layout information is also stored so a digital sketch or circuit layout card (Fig. 9) can be displayed as a testing aid (available March 1982). Another necessary piece of data that must be kept is the existence of 56-kb/s repeaters and the number of repeaters on a given loop. This information is necessary when doing digital testing on a repeated loop, due to a special sequence that must be followed. No special consideration is needed when doing a loop test because breaking the loop for dc tests removes the sealing current which in turn bypasses the 56-kb/s repeaters. One other data base consideration is 64-kb/s testing. The 64-kb/s access requires digital access information as well as LATS information.

DATA BASE OPERATION—TEST MODE

4.07 Since all testing functions are performed at the circuit level, all test commands must include the customer circuit number. The system, after checking the user's command for errors, will access the circuit index file and attempt to find the circuit number. If the circuit number is not found, an error message is sent to the requesting terminal and the system is ready to accept another command from that terminal.

4.08 If the circuit is found in the index, the master circuit record is read into memory and the eligibility of the requesting terminal to test that circuit is verified. If the terminal is eligible to test the circuit, the rest of the command line is examined to determine if the test is a directed test or an automatic test, because different steps will be taken for the different cases.

4.09 If the test requested is a full automatic test of the circuit, the circuit link records are scanned for the highest priority digital access point (DAP) and that link record is read into memory. From the link record, the system determines the SRDM record it needs (if subrate circuit); and from the SRDM re-

```
CKT: DSDT79466                                PCO:  MPLSMNDT
CUST:  WEST PUBLISHING COMPANY                CUST ID:
COMMENTS:  THIS IS AN EXAMPLE OF THE HIGH     RATE:  4.8
           LEVEL DISPLAY


CLEVOHO2S10
     MJU(1)    0/01/ - MSTR STN
               1/02/ - STN
               2/03/ - MJU(2)
               3/  / - SPARE
               4/  / - SPARE

NYCMNY54T30
     MJU(2)    0/03/
               1/04/ - MJU(4)
               2/05/ - STN
               3/06/ - MJU(3)
               4/09/ - STN

NYCMNYBWSL1
     MJU(3)    0/06/
               1/07/ - STN
               2/08/ - STN
               3/  / - SPARE
               4/  / - SPARE

PHLAPAMKW10
     MJU(4)    0/04/
               1/10/ - STN
               2/11/ - STN
               3/  / - SPARE
               4/  / - SPARE
```

Fig. 9—Display Request of Digital Sketch for a Multipoint Circuit

cord, the proper T1DM record is found. From these three records, the full access information for that access point is determined. If some of the required information is missing from one or more of the records, the requesting terminals will receive an error message to that effect. The user should then request, through the control office, a data base update.

4.10 Once all of the required access information is determined, the system checks the status of the SC covering the selected access point. If that SC is available to do the test, it is instructed to do so. If that particular SC is unavailable, the link records are scanned for the second highest priority DAP and the above process is repeated (available March 1982).

4.11 For a directed test (loopback DSU, loopback OCU, etc), the digital access point may be specified for any test command by the user. In this case, the link records are scanned to find that particular digital access point and from there on the process is the same as in the previous example (available March 1982).

4.12 In the case of a full automatic test (available March 1982), if the SC finds a suspected loop problem from the bit stream testing, the link record for the suspected loop is located and the proper SC is instructed to perform the loop test. If an office is not equipped with LATS and an SC, the local loop testing must be performed manually or via switched maintenance access system/switched access remote test system.

4.13 There are special cases of the above example. For instance, there are circuits that are all at 64-kb/s level in which we still pick the highest priority DAP; but the access arrangement is different, and SRDM or T1DM information is not required. Another special case is multipoint testing, which is explained in paragraphs 4.15 to 4.17.

LOCAL TESTING

4.14 Local testing can be done by using the access equipment in the manual mode. However, to realize maximum saving with ABATS, centralized testing is employed whenever possible.

MULTIPOINT TESTING

4.15 Multipoint testing is done on a segment-by-segment basis. Normal testing for a given segment is done from the nearest DAP on the down stream side of the serving MJU. This allows automatic tests to be done without disturbing the whole circuit, but still allows directed testing of MJUs and inter-MJU segments (available March 1982). Figure 10 shows the layout of a typical multipoint circuit. (Figure 10 is the circuit layout corresponding to the digital sketch shown in Fig. 9). Note, for example, that an automatic test on segment 5 (to station 5 out of Journal Square) and on segment 9 (to station 9 out of Boston) would be performed from New York #7 at the DAP at branch 2 or 4 on the MJU. This does not disturb the rest of the circuit while the test is in progress. However, a directed test can be made through branch 0 if the MJU needs to be tested (available March 1982). Refer to Section 314-901-531 for a discussion of test commands entered at an ABATS test terminal.

4.16 The programs for the TC and the SC are written to allow multiple tests to be in progress at a given location at the same time. Several dc loop tests can be interleaved with each other along with one or more digital tests.

4.17 If an automatic digital test cannot be done from the first choice access point due to busy equipment, the TC will select another access point on the circuit (available March 1982). For example, on Fig. 10 to test segment 11, the first choice DAP would be the Washington 3 side of the Philadelphia 2 office looking toward station 11 at Baltimore. If the equipment at Philadelphia 2 were already busy doing multiple tests, the TC would attempt the test first at Washington 3 and then at Baltimore. In either case, if the trouble was not found, the TC would automatically back up to Philadelphia 2 and try the test again from there. In most instances it should find the equipment available on the second try. If not, the TC will return a diagnostic message to the operator at the requesting terminal.

4.18 Multipoint circuits must always be tested to a station. Typically, the customer will report troubles on one particular segment of the circuit. The reportedly bad segment would most likely be one leading to a particular station, but it could also be a segment driving an MJU (refer to Fig. 10).

4.19 If the reported segment terminates in a station, the initial test sequence for the segment is very similar to that for a 2-point circuit. The TC will pick the highest priority access point on the segment (normally the DAP closest to the MJU port driving the leg to be tested) and call for a DSU loopback on the segment (available March 1982). If the loopback fails, the problem will be located exactly as if the segment were a 2-point circuit. If the DSU loopback is good, the system must back up to the DAP which drives the reported segment and test through the MJU to see if the port card for the segment is good. This test is ***not*** done automatically since it may require taking down more than one station on the customer network.

4.20 Based on the results of testing from the zero leg of the MJU, it may be necessary to back up the circuit even further in order to locate the trouble. Any subsequent testing after the initial test on the segment should always be done to the station already tested. If the troubleshooting procedures lead the user into having to test toward any other station on the network, start by testing the segment which terminates in that station as described above.

5. COMMAND LANGUAGE SUMMARY

5.01 The command language is used to initiate a test request at the ABATS test terminal. Section 314-901-531 will cover the format of the commands, the required and optional parameters for each command, and the format or the parameter specifications. Examples of correct and invalid command lines are also presented in the same section.

6. REFERENCES

6.01 For information concerning the units comprising ABATS, refer to the following sections:

SECTION	TITLE
107-605-100	KS-21899 Data Test System, Description
107-605-200	KS-21899 Data Test System, Installation

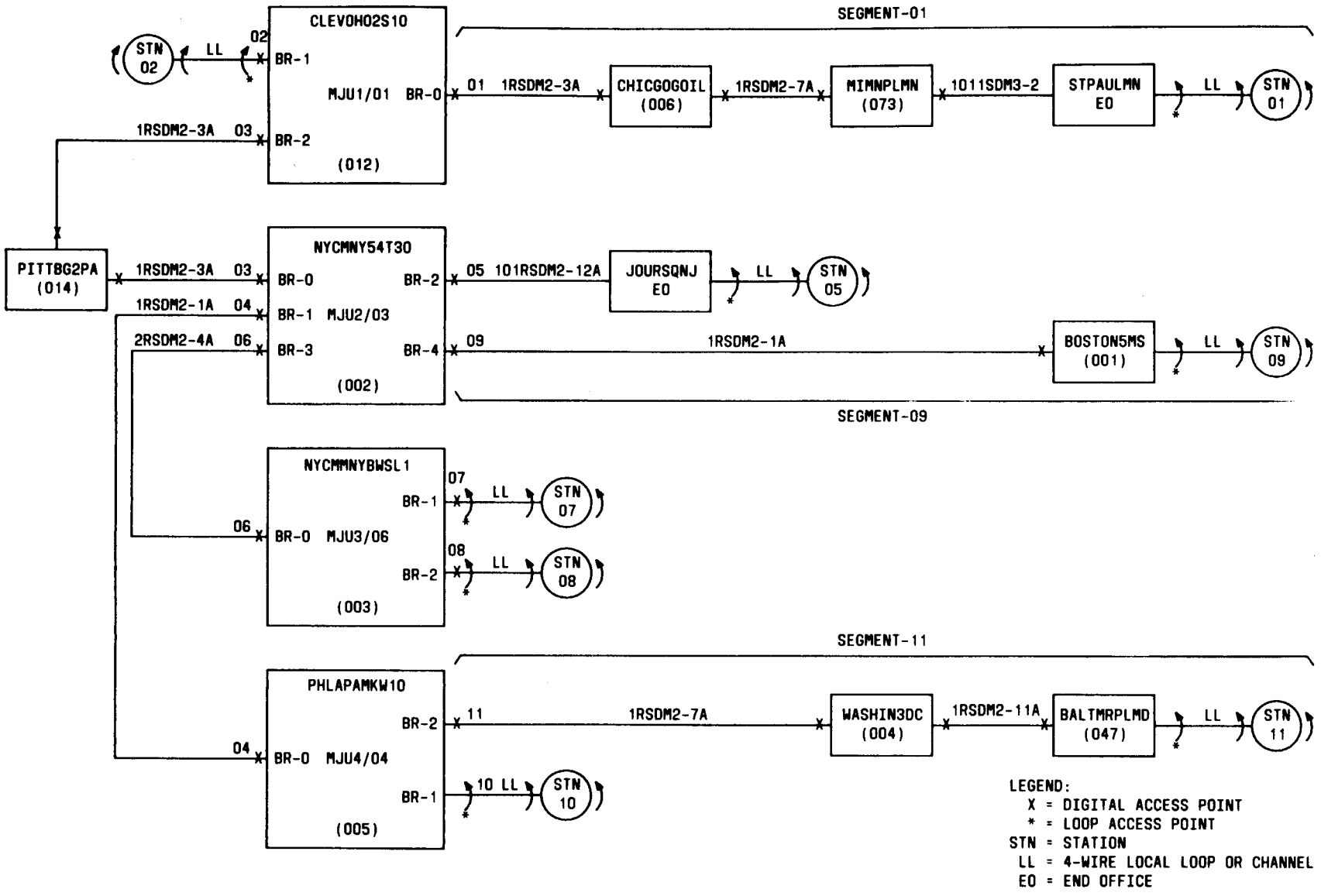


Fig. 10—Typical Multipoint Circuit Layout

SECTION	TITLE
107-605-300	KS-21899 Data Test System, Operation
107-605-500	KS-21899 Data Test System, Maintenance
314-960-100	Digital Data System—DS-1 Signal Access Unit and Auxiliary Circuits Description

6.02 For information concerning the units tested by ABATS, refer to the following sections:

SECTION	TITLE
314-901-530	Bit Access Test System (BATS) Manual Test Procedures, Digital Data System
314-901-531	Automated Bit Access Test System (ABATS), Remote Test Procedures, Digital Data Systems
314-901-532	Automated Bit Access Test System, Remote Data Base Update Procedures, Digital Data System
595-100-500	Digital Data System—550A-Type Channel Service Unit—Test Procedures
595-200-500	Digital Data System—500A-Type Data Service Unit—Test Procedures
595-200-501	500B-Type Data Service Unit, Test Procedures, Digital Data System
595-201-103	Digital Data System—510A-Type Data Service Unit—Maintenance
314-901-500	2-Point and Multipoint Private Line Circuit—Test Procedures—Digital Data System
314-917-500	Digital Data System—Multipoint Junction Units and Auxiliary Circuits—Test Procedures

6.03 The following sections can be referenced for additional information on maintaining local loops:

SECTION	TITLE
107-600-100	Digital Data System—KS-20909 Data Test Set (Transmitter)
107-601-100	Digital Data System—KS-20908 Data Test Set (Receiver)
314-410-310	Digital Data System, Local Loop, Maintenance Procedures
314-410-510	Local Loop, Tests and Requirements, Digital Data System
314-910-100	Digital Data System—Office Channel Unit—Description
314-910-300	Digital Data System—Office Channel Unit—Maintenance
314-910-500	Digital Data System—Office Channel Unit—Test Procedures
595-100-100	Digital Data System—550A-Type Channel Service Unit—Description
595-100-300	Digital Data System—550A-Type Channel Service Unit—Maintenance
595-200-100	Digital Data System—500A-Type Data Service Unit—Description and Operation
595-200-300	Digital Data System—500A-Type Data Service Unit—Maintenance
595-201-104	Digital Data System—510A-Type Data Service Unit—Test Procedures
880-601-115	Digital Data System—Engineering Considerations Customer Loops—Engineering and Maintenance

7. GLOSSARY OF TERMS

Automated Bit Access Test System (ABATS): A remote test system capable of testing bidirectionally on DDS. ABATS replaces the 950-type testboard.

Bit Access Test System (BATS): BATS may also be referred to as a KS-21899 data test system. BATS consists of the equipment mounted in a hub office that can be manually or remotely (ABATS) operated.

Data Base Manager and Test Controller (DBM and TC): A central location containing several minicomputers with associated equipment. The minicomputers are designated as data base manager and test controller. The test controller minicomputer has a complete backup system for continuous on-line operation.

Hub Office: An office in the DDS that combines T1 data streams from a number of local offices into signals suitable for transmission over DDS facilities at the DS-1 level or above. A hub office has test capability that is provided by a 950A testboard or KS-21899 data test system (also called BATS) or automated bit access test system.

KS-21899 Data Test System: See bit access test system.

Line Access Test System (LATS): A relay connection matrix that provides accessibility to individual customer 4-wire local loops and/or to DS-0 (64 kb/s) circuits. The matrix is installed only at DDS hub offices.

Microprocessor Sequence Controller (SC): A subcontrol unit that acts as an interface unit between the functional equipment (BATS and LATS) and the test controller. An SC is located with the BATS equipment.

Sequence Controller: See microprocessor sequence controller.

Special Service Center/Centralized Test Center (SSC/CTC): A distant location from the DBM and TC location where circuit trouble sectionalization is directed and coordinated.

Switch Maintenance Access Systems/ Switched Access Remote Test System (SMAS/SARTS): A system that provides remote circuit testing capability for intermediate and end offices. A SMAS/SARTS gives a tester the ability to access and test a circuit without the assistance of another tester in a distant office.

Test Terminal: The ABATS or remote test terminal consists of a DATASPEED 40/2 KDP terminal set for entering commands and displaying results. The terminal are located at the SSC/CTC locations.