# OFFICE CHANNEL UNITS AND AUXILIARY CIRCUITS

# DESCRIPTION

# DIGITAL DATA SYSTEM

CONTENTS PAGE



Figures



CONTENTS PAGE

CONTENTS PAGE

Tables



## 1. GENERAL

1.01 This practice provides physical and functional descriptions of the CPs (circuit packs), power supplies, logic and alarm circuit, 3-shelf OCU (office channel unit) and power supply assembly, and 2-shelf OCU assembly that makes up the OCU and auxiliary circuits used in the DDS (Digital Data System). Part 1 gives a general description of the purpose, function, and application of the OCU and auxiliary circuits. Part 2 covers the physical descriptions of the components that make up the OCU. Part 3 covers the functional description of an individual OCU channel and each CP required.

1.02 This practice is reissued for the following reasons:

(a) To add information on the HL225 CP

(b) To make minor changes to Tables C, D, and H

(c) To delete Tables J and K

(d) To make minor changes to Fig. 3, 4, 11, 16, 17, 18, and 19

(e) To delete old Fig. 14 and 15

(f) To delete old Part 4.

Revision arrows are used to emphasize the more significant changes.

1.03 The OCU is the unit in the DDS that provides the link between the local channel and the 64-kb/s data stream at the CO (central office). Each individual OCU is dedicated to a single customer loop which is terminated in either a DSU (data service unit) or a CSU (channel service unit) at the customer location. The OCUs are housed in 3- and 2-shelf OCU assemblies which are capable of providing space for up to 20 individual OCUs. Each shelf of an OCU assembly is electrically divided in half with each half-shelf containing five OCUs which operate at the same single customer service rate (2.4, 4.8, 9.6, or 56 kb/s).


***All five stations being served by the OCUs in a particular half of an OCU shelf MUST operate at the SAME customer service rate except for the HL201-203, HL220, ▸and HL225 CPs.◂***

1.04 Each channel of an OCU assembly performs the following functions:

(a) Converts data received from the local channel at the customer service rate to the intraoffice distribution rate (64 kb/s) and vice versa

(b) Recognizes and encodes system control codes required by the private line DDS

(c) Performs line conditioning for the local channel

(d) Recognizes the OCU loopback code when received from the CTC (centralized test center) and places the OCU in the OCU loopback mode

(e) Recognizes the CHAN loopback code when received from the CTC and signals the DSU or CSU at the customer location to enter the CHAN loopback mode

(f) The OCU (HL220) provides a latching loopback capability with new loopback procedures and responds to the loopback codes which are presently in use.

**1.05** The block diagram in Fig. 1 shows the relationship of the OCU within the DDS network. The points at which the data signals are looped back on recognition of the OCU loopback code are shown by arrows.

**1.06** In addition to OCUs, each shelf of an OCU assembly also contains:

1 - CT&O (common timing and oscillator)

1 - D-T (driver terminator) or ISMX (integral subrate multiplexer)

1 - CLKG (clock generator) if all of the OCUs in the particular half-shelf are not ▶HL201, 202, 203, 220, 222, or 225.◀

**1.07** If all the OCUs in a particular half-shelf are HL1 through 4, 141, or 142, the CLKG circuit provides timing and clock signals to the OCUs at a single customer service rate. If the OCUs are HL201, 202, 203, 220, or ▶225,◀ the timing and clock signals are provided by circuitry in the OCU and the CLKG is not required. The CT&O circuit, which is phase-locked to the DDS office clock signal, provides the associated CLKG or OCUs with the proper control signals required for rate matching and synchronizing the customer data and intraoffice data. The CT&O circuit also eliminates any phase incompatibilities between the received signal timing and the OCU common timing.

**1.08** The D-T circuit performs signal conversions while providing an interface between the OCUs and an SRDM (subrate data multiplexer) or T1 multiplexer (T1DM, T1WB4, or T1WB5). The ISMX circuit multiplexes signals received from OCUs and delivers the composite signal to a T1DM, T1WB4, or T1WB5. The ISMX circuit also demultiplexes the composite signal received from a T1DM, T1WB4, or T1WB5 into individual channel signals and delivers the signals to the appropriate OCU.

**1.09** The power supply shelf in the 3-shelf OCU assembly contains a logic and alarm circuit which monitors the output of the power unit serving the OCUs in the 3-shelf OCU assembly and, if provided, the output of the power unit serving a 2-shelf OCU assembly. If either power unit fails, the logic and alarm circuit automatically switches in the spare power unit and activates an alarm. This feature minimizes the circuit downtime during power unit failures. Refer to AT&T Practice 314-910-300 for installation and testing procedures.

**1.10** The DSU or CSU at the customer location is connected to the OCU at the hub or local office via two cable pairs. The intraoffice distribution is over 4-wire cable consisting of two nonloaded pairs.

**1.11** Transmission on the nonsecondary channel customer loop is a modified bipolar signal format. The format modification takes the form of controlled violations of the bipolar requirement that all successive ones must be transmitted opposite in polarity. One of the two uses for these bipolar violations is to provide a means for recovering timing when customer data consists of an extended sequence of uninterrupted zeros. The other use is to distinguish between network status control codes and customer data. A requirement of a data stream containing bipolar violations is that the sum of the polarities of the positive and negative pulses must be zero. This ensures that no dc buildup occurs in the customer loop. An example of bipolar data transmission, both with and without violations, is given in Fig. 2. In the nonsecondary channel mode, the HL220 performs the rate and format conversions between the DS-0A and customer rates (2.4, 4.8, 9.6, and 56 kb/s). It receives a bipolar bitstream from the loop at the customer rate. This stream may contain bipolar violation codes which will be mapped to the network code.

**1.12** Data transmission on a nonsecondary channel customer loop is in the form of a continuous stream of bipolar ones and zeros, while all intraoffice data is organized into 8-bit bytes by an OCU. The eighth bit position of each byte is dedicated to channel status information coding (a zero for control codes and a one for data). In the case of channels serving 2.4-, 4.8-, or 9.6-kb/s customers, the first bit position is dedicated to the SRDM framing code. The remaining bit positions (six for 2.4-, 4.8-, or 9.6-kb/s channels and seven for 56-kb/s channels) contain the customer data.

**1.13** In the nonsecondary channel mode these previous functions are the same as those of earlier OCUs such as the HL201, 202, 203, and HL4. If the secondary channel option is set, data received from

the loop must meet different criteria. The actual loop rates relative to the customer rates of 2.4, 4.8, 9.6, and 56 kb/s are 3.2, 6.4, 12.8, and 72 kb/s, respectively. ▶(The customer must have secondary channel compatible with network terminating equipment.)◀ The data rate is increased because in the secondary channel mode the eighth bit, that is, the network control bit which is shared by the secondary channel bit, is transmitted in the loop along with a loop framing pattern which is added by the OCU. The loop is still in a bipolar format; however, the previously used bipolar violations are eliminated. In the loop-to-network direction, the OCU performs no mapping. In the network-to-loop direction, the mapping takes place only when the OCU or channel is in the loopback mode and the OCU is receiving its respective loopback code. The loopback code is mapped to a data byte as it has been in the past.

**1.14** The following restrictions pertain to all OCU assemblies.

(1) The intraoffice cable between the OCUs and the SRDM or T1 multiplexer must not exceed 1500 feet. In hub offices, this distance includes the cabling necessary to access the CTC.

(2) The customer loop length must not exceed the limits given in AT&T Practice 314-410-310.

(3) All five OCUs in a particular half of an OCU shelf must operate at the same customer service rate. An LEC (local exchange company) can mix OCUs in the shelf as long as the records are kept straight.

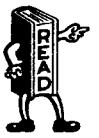
(4) For 10-channel ISMX applications, the full-shelf or each half-shelf must be either 2.4- or 4.8-kb/s OCUs.

(5) A CLKG is not required in a particular half-shelf when all the OCUs are HL201, HL202, HL203, HL220, ▶or HL225.◀

**1.15** Secondary channel information (S Bit) is carried through the network on the eighth bit which is time shared with network control information. On 2-point circuits and in the control station to tributary station direction of multipoint circuits, no more than every third S/C bit may be used to carry secondary channel information. Fewer bits may be used if desired. In the opposite direction of transmission on multipoint circuits, every third bit must be used when the secondary channel is active.

**1.16** ***Secondary Channel OCU (HL220 ▶and HL225◀):*** A secondary channel is an independent lower speed (133 1/3, 266 2/3, 533 1/3, 2666 2/3 kb/s) channel that will operate in parallel with the primary data channel through the DDS network. This feature will provide customers with a low speed secondary channel through which the customer may, for example, control or monitor his own network. These OCUs will provide all customer data rates and circuits (2.4, 4.8, 9.6, and 56 kb/s). The circuits will use the same basic network equipment and transmission facilities as the primary channel. A secondary channel will be derived at the network channel terminating equipment (DSU) and can be used independently of the primary channel. ▶(The HL220 or HL225 should not be used in the secondary channel mode unless the customer has secondary channel compatible with network terminating equipment [DSU].)◀

**1.17** ▶The HL220 provides latching loopback. The HL225 does not provide latching loopback.




***Secondary channel service introduction must be coordinated in the network as described in AT&T Practice 314-900-100.◀***

## 2. PHYSICAL DESCRIPTION

**2.01** This part describes the physical appearance of the components which make up the 3- and 2-shelf OCU assemblies. A brief description of the OCU assembly terminal strip arrangements is also given, along with the power requirements for OCU assemblies.

### A. 3-Shelf OCU Assembly (Fig. 3)

**2.02** The 3-shelf OCU assembly (J70177AA), which consists of two equipment shelves (A and B) and a power supply shelf (C), has external dimensions of 24.5 inches high, 23 inches wide, and 12 inches deep. The 3-shelf OCU assembly weighs approximately 34 pounds with CPs and power units removed and 108 pounds when fully equipped. The CPs, TSs (terminal strips), connectors, and power units that are part of the equipment shelves and power supply shelf are described in paragraphs 2.03 through 2.10.

**Equipment Shelves**

**2.03** A fully equipped equipment shelf contains from 13 to 15 CPs which consist of ten OCUs, two CLKGs (required only when all the OCUs in a particular half-shelf are HL1 through 4, 141, or 142), one CT&O CP, and two D-T CPs, or two 5-channel ISMX CPs, or one 10-channel ISMX CP. All of the CPs are of the HL-type and are approximately 10.5 inches long, 7.7 inches high and from 0.5 to 1.75 inches wide. A description of the CPs available for installation in an equipment shelf is given below.

- HL1 OCU — One for each 2.4-kb/s private line. This OCU contains 24 TPs (test points) and the identification on the faceplate is printed on an orange background. The HL1 OCU is rated Mfg Disc.

- HL2 OCU — One for each 4.8-kb/s private line. This OCU contains 24 TPs and the identification on the faceplate is printed on a yellow background. The HL2 OCU is rated Mfg Disc.

- HL3 OCU — One for each 9.6-kb/s private line. This OCU contains 24 TPs and the identification on the faceplate is printed on a green background. The HL3 OCU is rated Mfg Disc.

- HL4 OCU — One for each 56-kb/s private line. This OCU contains 24 TPs and the identification on the faceplate is printed on a blue background. The HL4 OCU is rated Mfg Disc.

- HL141 OCU — One for each 56 kb/s and each 56-kb/s special feature private line. This OCU contains 24 TPs and the identification on the faceplate is printed on a blue background. The HL141 OCU is rated Mfg Disc.

- HL142 OCU — One for each 9.6 kb/s and each 9.6-kb/s special feature private line. This OCU contains 24 TPs and the identification on the faceplate is printed on a green background. The HL142 OCU is rated Mfg Disc.

- HL201 OCU — One for each 2.4-kb/s private line. This OCU contains 12 TPs and the identification on the faceplate is printed on an orange background. The HL201/HL201B OCU is rated Mfg Disc.

- HL202 OCU — One for each 4.8-kb/s private line. This OCU contains 12 TPs and the identification on the faceplate is printed on a yellow background. The HL202/HL202B OCU is rated Mfg Disc.

- HL203 OCU — One for each 9.6-kb/s private line. This OCU contains 12 TPs and the identification on the faceplate is printed on a green background. The HL203/HL203B OCU is rated Mfg Disc.

Figure 4 shows typical HL1 through 4, HL141, HL142, HL201, HL202, and HL203 OCUs.

- ◗HL220 OCU — Provides all data rates plus secondary channel rates and latching loopback. This OCU contains 12 TPs and the identification on the faceplate is printed on a dull aluminum background.◖ Figure 4 shows the HL220 OCU.

- ◗HL225 OCU — Provides all data rates plus secondary channel rates but without latching loopback. This OCU contains 12 TPs and the identification on the faceplate is printed on a dull aluminum background. Figure 4 shows the HL225 OCU.◖

- HL96 LSI — One for each dataport channel that terminates on the DDS local office from a D3/D4 channel bank. Figure 5 shows the LSI (loop side interface) CP (HL96) with the TPs and option switches identified.

- HL222 LSI — One for each dataport channel that terminates on the DDS local office from a D3/D4 channel bank. This LSI provides a latching loopback capability to the testing center.

- HL80 CLKG (2.4-kb) — One for each OCU half-shelf equipped with the 2.4-kb/s OCU (HL1). This CLKG is not required when the OCU half-shelf contains OCU HL201. This CLKG contains 12 TPs and the identification on the faceplate is printed on an orange background.

- HL5 CLKG (4.8/9.6-kb) — One for each OCU half-shelf equipped with either 4.8- or 9.6-kb/s OCUs (HL2, 3, or 142). This CLKG is not required when the OCU half-shelf contains

OCU HL202 or 203. All OCUs in the corresponding half-shelf must operate at the same speed. A screw switch option located on the HL5 CLKG is used to set the CLKG at 4.8 or 9.6 kb/s. This CLKG contains 12 TPs and the identification on the faceplate is printed on a gray background. Figure 6 shows a 4.8/9.6-kb CLKG (HL5).

- HL6 CLKG (56-kb) — One for each OCU half-shelf equipped with 56-kb/s OCU CPs (HL4 or HL141). This CLKG contains 12 TPs and the identification on the faceplate is printed on a blue background.

- HL7 D-T — One for each OCU half-shelf equipped with OCUs which are to be connected directly to an SRDM or a T1 multiplexer (T1DM, T1WB4, or T1WB5) using an SM-JCP (submultiplexer jack and connector panel) or M-JCP (multiplexer jack and connector panel). This D-T contains 20 TPs on the faceplate. Figure 7 shows the HL7 D-T with test points identified.

- HL89 D-T — One for each OCU half-shelf equipped with 56-kb/s OCUs which are to be connected directly to a T1 multiplexer (T1DM, T1WB4, or T1WB5) at local offices using an M-JCP or a QTP (quad terminal panel). This D-T contains twenty TPs, five KS-21001-L4 jacks, and one KS-21001-L1 jack on the faceplate. Figure 7 shows the HL89 D-T CP with the test points and jacks identified.

- HL8/HL8B ISMX (5-channel) — One for each OCU half-shelf equipped with 2.4-, 4.8-, or 9.6-kb/s OCUs at local offices using an M-JCP or a QTP. This ISMX contains twenty TPs and five KS-21001-L2 jacks on the faceplate. Figure 8 shows the 5-channel HL8/HL8B ISMX with the out-of-sync alarm LED (light emitting diode), test jacks, and TPs identified. The HL8 ISMX is rated Mfg Disc., and is replaced by HL8B.

- HL88/HL88B ISMX (10-channel) — One for each OCU whole-shelf equipped with 2.4- or 4.8-kb/s OCUs at local offices using an M-JCP or a QTP. This ISMX is made up of two circuit boards attached to a single faceplate which contains twenty-seven TPs, ten KS-21001-L2 jacks, and five LEDs. Figure 8 shows the 10-channel HL88/HL88B ISMX with out-of-sync clock failure, and circuit failure alarm indicators, test jacks, and TPs identified. The HL88 ISMX is rated Mfg Disc., and is replaced by HL88B.

- HL9 CT&O — One for each OCU whole-shelf. This CT&O contains 12 TPs on the faceplate.


***None of the above listed OCUs are supplied with the OCU assemblies; therefore, all must be ordered separately.***

**2.04** The rear of each of the equipment shelves (A and B) has provision for mounting the following connectors. The relationship of the OCU channels to the equipment shelf connectors is shown in Fig. 9.

- Twenty-five 940-type connectors — One for each OCU. Certain OCUs (HL1 through 4, 141, and 142) and the HL88/HL88B CP require two 940-type connectors.


***Although two 940-type connectors are provided for each OCU, the HL201, 202, 203, and 220 OCUs require only one of these connectors. An additional list A wiring option or field modification (SD-73074-01 wiring option J, J-70177AB List 1) must have been installed in the OCU equipment assembly before these CPs will function properly when installed in an equipment shelf.***

- Two KS-16672-L12 jacks (J1A and J1B) — Each jack contains 50 pins and provides the means for connecting the 64-kb/s side of the OCU channels in their respective shelves to the DSX-0A or SM-JCP.

- Five KS-16672-L18 jacks (J2A, J4A, J2B, J3B, and J4B) — Each jack contains 24 pins and provides the means for connecting the 64-kb/s side of the OCU channels in their respective shelves to the M-JCP or QTP. The ISMX CP (HL8 or HL88) multiplexed input and output signal leads appear at J3B.

- Two KS-16672-L2 jacks (J5A and J5B) — Each jack contains 50 pins and provides the

means for connecting the customer loop side of the OCUs in their respective shelf to the MDF (main distributing frame) for cross-connection to the octal channel.

**2.05** When a 10-channel ISMX is used in all equipment shelves of a 2- or 3-shelf OCU assembly, two quads out of the 4-quad cable between connector J3B of the OCU assembly and the M-JCP or QTP will each be carrying a 64-kb/s multiplexed data channel from the ISMX. Two of the quads remain unused resulting in two inaccessible ports in the second stage multiplexer (T1DM, T1WB4, or T1WB5). To avoid having these inaccessible ports in the multiplexer, a 3-headed splitting cable (ED-73435-22, G8) should be used to combine the two active quads from the 4-quad OCU cable of a 2-shelf OCU assembly and the two active quads from the 4-quad OCU cable of a 3-shelf OCU assembly into a single connector containing four active quads (Fig. 9).

**Power Supply Shelf**

**2.06** The power supply shelf in a 3-shelf OCU assembly has provisions for containing up to three plug-in power units, a logic and alarm circuit pack (ED-82512), and a fuse panel.

**2.07** The power units which can be installed in the power supply shelf are listed in Table A, along with the central office battery supply needed to power each one. Each of the power units measures 10.2 inches long, 7.7 inches high, 5.2 inches wide and weighs approximately 15 pounds. Each 71C or 76C power unit consists of two circuit boards attached to a single faceplate. The faceplates of the 71C and 76C power units (rated Mfg Disc.) contain two pushbutton switches, six test points, and two LEDs. Each 71C1 or 76C1 power unit consists of only one circuit board attached to a single faceplate. The faceplates of the 71C1 and 76C1 power units contain one toggle switch (momentary contact), seven test points, and two LEDs.

**2.08** The logic and alarm circuit pack is a plug-in unit which measures 10.2 inches long, 7.7 inches high, and 2 inches wide. The logic and alarm circuit pack consists of two circuit boards attached to a single faceplate which contains two LEDs and seven test points.

**2.09** The fuse panel is an integral part of shelf C and contains three 70F-type fuses (0.25 amps).

**2.10** The terminal strips and connectors located on the rear of the power supply shelf (C) provide power to the power units in the shelf, and power and timing signals to the equipment shelves in the 3- and 2-shelf OCUs. These terminal strips and connectors are described below with their interconnections shown in Fig. 10.

- TS1C (6 terminals on list 1 assemblies and 15 terminals on list 2 and list 3 assemblies) — Power to shelf B of a 2-shelf OCU assembly.
- TS2C (6 terminals on list 1 assemblies and 15 terminals on list 2 and list 3 assemblies) — Power to shelf A of a 2-shelf OCU assembly.
- TS3C (9 terminals on list 1 assemblies and 15 terminals on list 2 and list 3 assemblies) — Power from the LTS (local timing supply) or BCPA (bay clock, power, and alarm) shelf and, if required, redundant 5-volt power to the BCPA shelf.
- One KS-16672-L18 jack (J1C) — This jack contains 24 pins and provides timing signals, received from the BCPA or LTS shelf via jack J2C, to a 2-shelf OCU assembly.
- One KS-16672-L12 jack (J2C) — This jack contains 50 pins and provides timing signals from the BCPA or LTS shelf to the CT&O CPs in the associated equipment shelves and to the CT&O CPs in an OCU 2-shelf assembly. This jack also provides alarms from the logic and alarm circuit to the BCPA or LTS shelf.

Power is supplied to the two equipment shelves in the 2-shelf OCU assembly directly from the power shelf via the KS-13385 wire.

**B. 2-Shelf OCU Assembly (Fig. 11)**

**2.11** The 2-shelf OCU assembly (J70277AB) consists of two equipment shelves and has external dimensions of 16.5 inches high, 23 inches wide, and 12 inches deep. The 2-shelf OCU assembly weighs approximately 27 pounds with all CPs removed and 54 pounds when fully equipped. A list of the CPs which can be installed in each of the equipment shelves is given in paragraph 2.03. The rear of the 2-shelf OCU assembly has provision for mounting the connectors listed in paragraph 2.04, plus the following connector and terminal strips. Locations of CPs,

connectors, and terminal strips associated with a 2-shelf OCU assembly are shown in Fig. 11. The relationship of the OCU channels to the equipment shelf connectors is shown in Fig. 9.

- TS1A and TS1B (6 terminals on list 1 assemblies and 15 terminals on list 2 and list 3 assemblies) — Each terminal strip provides the means for connecting power from TS2C and TS1C, respectively, of the 3-shelf OCU and power supply assembly, to shelf A and B, respectively, of the 2-shelf OCU assembly.

- One KS-16672-L18 jack (J3A) — This jack contains 24 pins and provides timing signals from the 3-shelf OCU assembly (J1C) to the CT&O CPs in the 2-shelf OCU assembly.

Power and timing signals to the 2-shelf OCU assembly are provided via connectors on the 3-shelf OCU assembly as shown in Fig. 10.

**2.12** The 2- and 3-shelf OCU assemblies can be installed in a 7-foot or an 11-1/2 foot bay. A typical example of these bay arrangements is shown in Fig. 12.

### C. Options

**2.13** Options, which are described below, are available on the 2-shelf (J70177AB) and 3-shelf (J70177AA) OCU assemblies, and are concerned with the availability of connectors and terminal strips on the rear of these assemblies. Options are also available in the OCUs, CLKG (HL5), and the logic and alarm circuit. They are summarized in Table B.

*Note:* When OCU HL141 or HL142 is used in a private line with no special features, it should have options A and E installed. OCU HL201, HL202, and HL203 should have options A and E installed. Options B and F are used to provide future special features.

- Option S — Provides connectors J1A, J1B, J3A, J5A, and J5B on the rear of a 2- or 3-shelf OCU assembly. This option is for use in offices that use an SM-JCP or DSX-0 type cross-connect rather than an M-JCP.

- Option Q — Provides connectors J1A, J1B, J3A, J2A, J2B, J3B, J4A, J4B, J5A, and J5B on the rear of a 2- or 3-shelf OCU assembly. This option is for use in offices using M-JCPs rather than SM-JCP or DSX-0 type cross-connects.

**2.14** Options are also available in the LSI (HL96). These are for selecting the proper speed clock generator (switches S1 and S2) and for bypassing the bit and byte realignment circuit (switches S3 and S4). These options are summarized in Table C and D, respectively. These options are not available on HL222.

## 3. FUNCTIONAL DESCRIPTION

### A. General

**3.01** This part provides a functional block diagram description of an individual OCU channel when equipped with either a D-T or an ISMX. A functional block diagram description of each CP that makes up an OCU channel is also included, along with a description of the power supply shelf in a 3-shelf OCU assembly.

### B. OCU Channel Description

#### OCU Channel Equipped With HL7 or HL89 D-T CP

**3.02** The block diagram in Fig. 13 shows an OCU channel equipped with a D-T. This arrangement may be used at all three (hub, intermediate, and end) DDS offices. At hub office installations, the D-T is connected to a multiplexer, an SRDM, or another OCU D-T via the DSX-0A and the CTC. At intermediate and end offices, an HL7 D-T is connected to a multiplexer or an SRDM via an M-JCP or SM-JCP, respectively. If the D-T at an intermediate or end office is an HL89, connection to a multiplexer is made via a QTP or an M-JCP.

**3.03** The OCU receives data from the customer in the serial bipolar format with the system control codes identified by bipolar violation sequences (paragraph 1.11). After amplification and equalization, the OCU converts the customer data to logic level signals. It then encodes the data into 8-bit bytes and, through a byte stuffing technique, rate matches the customer data rate to the intraoffice distribution rate of 64 kb/s.

**3.04** When any loop is intended to carry secondary channel service, it must be equipped with the new OCU (HL220) ▶or HL225.◀ These units are capable of operating at any of the customer rates with or

without secondary channel capability. Options must be set on the units to select the desired customer primary channel rate of 2.4, 4.8, 9.6, or 56 kb/s and whether or not secondary channel capability is desired. A channel will operate satisfactorily end-to-end with one end loop equipped for secondary channel operation and the other end not equipped as long as no secondary channel transmission is attempted. Except for the need for the framing bit, there is no restriction on the content of the loop data signal.

**3.05** ▶The CT&O provides a number of timing signals which are derived from the 8- and 64-kHz intrabay office clock distribution. The CLKG uses these timing signals to generate a number of clock and timing pulses which are required by some of the OCUs (HL1, HL2, HL3, HL4, HL141, or HL142) for rate matching, etc. The OCUs HL201, 202, 203, 220, and 225 use the timing signals from the CT&O to generate their own clock and timing pulses.◀

**3.06** The D-T converts the logic-level signals from the OCU to the baseband bipolar format; amplifies the signal; and then delivers it toward the DSX-0A, M-JCP, SM-JCP, or QTP. Conversely, the D-T terminates the line from the DSX-0A, M-JCP, SM-JCP or QTP; converts the baseband bipolar signal to logic-level signals; and delivers the logic-level signals to the OCU.

**3.07** The OCU monitors the byte-encoded, logic-level signals for all zeros data or system control codes (idle, OCU loopback, and CHAN loopback), converts the logic-level signals to the serial bipolar format, inserts bipolar violations when control codes are present, or transmits the control codes. In the case of a secondary channel, it transmits the bipolar code to the customer. If the OCU or CHAN loopback codes are detected, the OCU connects the local channel transmit pair to the local channel receive pair (OCU loopback) or signals the CSU or DSU at the customer location to connect the line receiver to the line driver on the local channel side (CHAN loopback).

**3.08** The plan to provide the DDS with an end-to-end secondary channel capability combines two different, complementary schemes. The first of these schemes provides the required secondary channel capacity in the local loop from the customer premises to the OCU; the second provides for the transmission of the secondary channel information throughout the DDS network to the far-end OCU. The network transmission plan exploits the excess capacity inherent in the eighth bit of each network byte, the control (C) bit, to introduce a secondary channel without requiring major modifications of the existing network transmission equipment. The C bit at present is used only to indicate if the network byte carries data (C = 1) or control information (C = 0), and the system actually uses more C bits than necessary for proper network operation. To support secondary channel operation in the DDS, every third C bit may be replaced by a secondary channel (S) bit. The resulting secondary channel capacity at the different customer rates is shown in Table E.

**3.09** In the local loop there is no excess capacity; therefore, it must be created wherever secondary channel capability is required. Two extra bits are added to every byte at every customer rate; one to carry the secondary channel and network control (C/S), and one for framing (F), which defines the byte and, thus, the location of the secondary channel bit. With the introduction of the C/S bits in the loop, the C bits become available at the customer premises; thus, the present necessity of using bipolar violations for loop control will be eliminated.

### OCU Shelf Equipped With an HL8/HL8B or an HL88/HL88B ISMX

**3.10** The block diagram in Fig. 14 shows the OCU shelf equipped with either an HL8/HL8B or an HL88/HL88B ISMX. This arrangement is used at an intermediate or end office only. In all cases, either ISMX is connected to a multiplexer via an M-JCP or a QTP.

**3.11** The functions of the CT&Os and CLKGs are the same as described in paragraph 3.05 for the OCU channel equipped with the D-T, except that the CT&O also provides either ISMX with office clock signals. The functions of the OCUs are the same as described in paragraphs 3.03 and 3.07.

**3.12** When an HL8 ISMX is provided, it is capable of serving up to five subrate OCUs which are located in a particular half of an OCU shelf. It provides the means for multiplexing the output of five subrate OCUs into a single logic-level data stream at the intraoffice distribution rate and vice versa. In addition, it contains circuitry which converts the logic levels to and from the bipolar 64-kb/s stream in the same manner as described in paragraph 3.06 for the D-T.

**3.13** When an HL88/HL88B ISMX is provided, it is capable of serving up to ten 2.4- or 4.8-kb/s OCUs which are located in a whole-shelf OCU. Speed mixing is permissible with up to five 2.4-kb/s OCUs and up to five 4.8-kb/s OCUs being served by the same ISMX. The multiplexer combines the logic-level signals from ten OCUs into a single 64-kb/s bipolar signal for transmission to the port of a T1DM, T1WB4, or T1WB5. The demultiplexer converts the received 64-kb/s bipolar signal to ten logic-level signals and passes these demultiplexed signals to the OCUs in the same shelf.

### C. Circuit Pack Description

#### OCUs

**3.14** The block diagram in Fig. 15 shows OCUs HL1 through 4, 141, 142, 201, 202, and 203. The main difference in operation between the individual OCUs is the number of stuff bytes required to bring the customer service rate up to the 64-kb/s intraoffice distribution rate. The number of data and stuff bytes required by HL1, 2, 3, 142, 201, 202, and 203 for rate matching is given in Table F. Byte stuffing is not required for HL4 or HL141 because the addition of the network control bit (bit 8) to the data stream brings the 56-kb/s customer service rate up to 64 kb/s.

#### ▶Secondary Channel HL220 and HL225 OCUs

**3.15** The HL220 and HL225 OCUs offer the following features:

(a) These OCUs are used for all rates with or without secondary channel capability. The rate and secondary channel capability are selected.

(b) These OCUs do not require a clock generator (i.e., HL5, 6, or 80).

(c) HL220 provides a latching loopback capability and a nonlatching loopback capability. The HL225 does not provide latching loopback.

(d) The HL220 and 225 are single printed wiring board units and may be used in all DDS bays which are wired for single board use (option J).◀

In the nonsecondary channel mode, the HL220 ▶and HL225◀ perform the rate and format conversions between the DS-0A and customer rates (2.4, 4.8, 9.6, and 56 kb/s). These OCUs receive a bipolar bit stream from the loop at the customer rate. This stream may contain bipolar violation codes which will be mapped to the network code. Data is sampled in 6-bit blocks when at the subrates 2.4, 4.8, and 9.6 kb/s and 7-bit blocks at the 56-kb/s rate. These data blocks are placed into a byte format for network transmission. At the subrates the six data bits are combined with a framing bit and a control bit. The 8-bit bytes are then repeated (byte stuffed) to make up the 64-kb data stream. At 56 kb/s the 7-bit data block is combined with a control bit to make an 8-bit byte at 64 kb/s and transmitted on the network.

**3.16** To implement a secondary channel, the excess capacity inherent in the eighth bit (network control bit) of each network byte will be shared with the customer. Specifically, the customer can use the control bit in every third byte at all subrate speeds as well as 56-kb/s channels. Table E defines the secondary channel capacity at the various customer rates. As a result of increasing the bit rate on the loop and the customer use of the control bit, the customer interface and certain network components have been modified.

#### D-T or ISMX to Local Channel Signal Flow

**3.17** The D-T or ISMX delivers data to the OCU as a byte-encoded binary bitstream on the DATA IN lead. One random byte out of each 5, 10, or 20 bytes in a repetitive cycle is sampled under control of the SAMPLE PULSE from the CLKG or from the timing counters and sync circuit in the OCU.

> *Note:* Several OCUs (HL1 and 201 through 203) are designed to always sample the first byte of the 5-, 10-, or 20-byte repetition cycle. This is accomplished by the byte aligner circuit. In this case, the CLKG or timing counters and sync circuit in the OCU deliver the sample pulse to the serial buffer through the byte aligner and bipolar encoder circuits.

As the byte is shifted into the buffer circuit, the SRDM framing bit (bit 1) is discarded. For 56-kb/s service, bit 1 is data; therefore, HL4 and HL141 are designed to retain bit 1.

**3.18** While the byte is in the serial buffer circuit, it is checked for specific bit sequences by the pattern monitor circuit. If all zeros data or any of the network control codes or loopback test codes (except

the CHAN loopback code) are detected, the pattern monitor circuit signals the bipolar encoder to replace bits 5, 6, and 7 of the byte with the bipolar violation sequence. In the case of the OCU loopback and CHAN loopback codes, the pattern monitor also enables the loopback flywheel circuit which, in turn, signals the test circuits on the OCU or CHAN loopback lead that the loopback code has been received. The test circuits then either connect T1 and R1 to T and R (OCU loopback), or signal the DSU or CSU to enter the CHAN loopback mode by reversing the polarity of the simplex sealing current that is on the local loop pairs. When the code detected is the CHAN loopback code, the signal to insert the bipolar violation sequence is inhibited. Some specific codes detectable by the pattern monitor in HL1, 2, 3, or 4 are given in Table G, along with the pattern monitor circuit response. As shown in Table G, all codes with a zero in bit 8, except the all zeros control mode, cause the pattern monitor in HL1, 2, 3, or 4 to signal the bipolar encoder to insert a bipolar violation.

**3.19** The pattern monitor in HL141, HL142, and HL201 through 203 CPs normally responds to the codes as specified in Table G. Control mode codes with bits 5 and 8 equal to zero are sent as data mode codes (no violations) along with four other control codes; 0001100, 0001110, 1001110, and 1001100 (bits 2 through 8). The remaining control codes (bit 8 = 0) are sent with the bipolar violations sequence. If the CRCT (customer remote CHAN test) option is installed in HL141 or 142, the DSU loopback code defined in Table G is treated as a CHAN loopback code; that is, the sealing current is reversed to effect a CHAN loopback in the CSU and the insertion of the bipolar violation sequence is inhibited.

**3.20** Once the complete byte is in the serial buffer circuit, the bit clocks shift it into the bipolar encoder circuit. If the insert violation signal is present, bits 5, 6, and 7 are replaced by the bipolar violation sequence and the data is serially delivered to the line driver circuit as a dual rail form of the bipolar signal.

**3.21** The A/D (analog-to-digital) converter portion of the line driver changes the dual rail logic level inputs into controlled amplitude 50-percent duty cycle bipolar pulses. These are filtered to reduce high frequency energy, buffered by an amplifier, and then used to differentially drive the output transformer which delivers the balanced bipolar signal to the local channel on the T and R leads. A nominal output impedance of 135 ohms is presented to the local channel cable pair by the line driver.

**3.22** The serial balanced bipolar data stream is received from the local channel on T1 and R1 and delivered to the line receiver which presents a 135-ohm impedance to the local channel cable pair. The line receiver consists of the ALBO (automatic line build-out) circuit, pulse shaping filter, equalizer circuit, and A/D circuit. The ALBO circuit is a network that automatically adds frequency-shaped loss to the signal path to make the total transmission loss of the customer loop appear to be that of a maximum length cable. The range of automatic adjustment in the ALBO circuit is limited; therefore, an optional FLBO (fixed line build-out) pad, controlled by screw switches S1, S2, S3, and S4, is provided in the line protection and test circuits to add additional loss for extremely short cable pairs. The FLBO pad is installed in the receiving path by closing screw switches S3 and S4, and opening screw switches S1 and S2. Conversely, the pad is removed from the receiving path by closing screw switches S1 and S2, and opening screw switches S3 and S4.

**3.23** The pulse-shaping filter is a low-pass filter that smooths the pulses. The equalizer circuit provides a frequency gain characteristic that is the inverse of the maximum length cable loss characteristic. Due to behavioral differences in the variety of cable gauges that may be encountered in the local channel cable pairs, the equalization provided is a compromise average of the equalization required for each of the standard gauge (19 through 26) cables. The preamplifier circuit provides sufficient gain to overcome the transmission loss encountered by the signal and delivers a dual rail equalized signal to the A/D circuit.

**3.24** The A/D circuit converts the dual rail equalized signal to dual rail logic signals and delivers them to the bipolar decoder circuit. In addition, the A/D circuit provides frequency and phase information to the clock recovery circuit, and a presence of signal indication to a signal-presence monitor circuit which are auxiliary circuits in the preamplifier and A/D circuit. If for any reason there is no data signal present, the signal-presence monitor circuit will signal the assembly buffer circuit to send to the distant end either the idle code 1111110 (bits 2 through 8), if the OCU is HL1, 2, 3, or 4; or the ASC (abnormal station code) 0011110 (bits 2 through 8), if the OCU is HL141, 142, or 201 through 203.

**3.25** The clock recovery circuit consists of a VCO (voltage controlled oscillator) and counter circuit connected in a phase-locked loop. The VCO output is counted down and a specific speed is tapped off at a certain stage in the counter to clock the sampling of data by the bipolar decoder circuit. The bipolar decoder circuit retimes the data to the office bit clock, examines the data for bipolar violations, converts the data to binary form, and shifts the data into the assembly buffer circuit. Bipolar violations in the received data cause the bit stream to be examined for the idle, zero suppression, and OCU loopback codes. If one of these codes is detected, the bipolar decoder circuit changes the bipolar violation sequence; that is, the pulse with the polarity violation plus the two preceding pulses, to all ones (idle code) or all zeros (zero suppression and OCU loopback codes). In addition, detection of the idle code sets a flip-flop in the recirculating buffer which causes the idle code to be sent to the D-T or ISMX the next time the byte is shifted into the recirculating buffer circuit regardless of the contents of the assembly buffer at that time.

**3.26** The HL141, HL142, and HL201 through 203 OCUs examine the bit stream for eight codes with bipolar violations including the three processed by HL1, 2, 3, and 4. The idle, zero suppression, and OCU loopback codes are normally processed in a manner similar to that used by HL1, 2, 3, and 4. All the codes with bipolar violations which are recognized and processed by HL141, HL142, and HL201 through 203, and the corresponding DS0 control codes are given in Table H. When a code with a bipolar violation, other than zero suppression and normally the OCU loopback code, is detected, the information is stored in a set of flip-flops and the corresponding entry in the DS0 column in Table H is transferred to the recirculating store at the appropriate time.

**3.27** Once a complete byte of data (seven bits for 56 kb/s or six bits for 2.4, 4.8, and 9.6 kb/s) is shifted into the assembly buffer, the recirculating buffer circuit is cleared and the new byte is parallel shifted into the recirculating buffer circuit.

> ***Note:*** In the 2.4-kb/s OCU, the new byte is serially shifted into the recirculating buffer circuit.

**3.28** At this time, the network control bit (bit 8) is added to the byte. For rates below 56 kb/s, bit 1 of the 64-kb/s byte (used for framing by the SRDM) is transmitted by the OCU as a zero. In 56-kb/s service, bit 1 is normally a one when control codes are transferred into the recirculating store. There are two exceptions to this statement. When the CRCT option is installed on HL141, bit 1 is a zero when 0101100 (bits 2 through 8) is transferred to the recirculating store. The other exception occurs when the customer multiplexing option is installed on HL141. When this option is installed, the data in bit position 1 of the assembly buffer is always transferred to bit position 1 of the recirculating store whenever a control code is transferred into the recirculating store. The byte is serially shifted out of the recirculating buffer by the 64-kb/s clock. The output of the recirculating buffer is fed back to its own input so that as the byte is shifted out, it is also serially shifted back into the recirculating buffer. In this way, the byte is repeated the required number of times to rate match the customer service rate to the intraoffice distribution rate.

> ***Note:*** Since the addition of bit 8 brings the 56-kb/s rate up to 64 kb/s, this recirculation and repetition of the byte is not required in HL4 and 141.

The recirculating buffer circuit delivers the 64-kb/s byte organized data to the D-T or ISMX on the DATA OUT lead. It also includes a bipolar polarity generating circuit to control the balance of the intraoffice line driver when HL7 (D-T) is used.

**3.29** The line protection and test circuits complete the OCU. This circuit provides lightning protections for the customer loop transmit and receive paths as well as relay circuitry for testing the OCU (OCU loopback) and signaling the DSU or CSU to enter the CHAN loopback mode. A simplexed dc sealing current is maintained on the local channel with negative battery applied normally to the T and R transmit pair through a current limiting resistor. Reversal of the simplex current by applying the negative battery to the T1 and R1 receiver pair signals the CSU or DSU to enter the CHAN loopback mode.

**HL96/222**

**3.30** The HL96/222 provides for dataport channels to access either an ISMX, an HL89 D-T, or an HL7 D-T by using the OCU position and the OCU loop-side cabling. The HL96/222 can be mounted in

any OCU position in a standard local office arrangement.

**3.31** The standard loop-side cabling from the OCU assembly to the distribution frame is used to connect the HL96/222 to DS0 dataport channels. The logic level signals from HL96/222 are connected to either an ISMX or a D-T using existing OCU backplane wiring. The use of an HL96/222 in place of an OCU does not affect the conventional DDS application of the OCU assembly.

**3.32** Any HL96/222 that is connected to a subrate dataport channel is to be installed in the same half-shelf with the DDS subrate OCU of the same subrate speed. If HL201, 202, or 203 type OCUs are used in the shelf, the use of an HL96 requires the addition of a clock generator which is not normally needed. The HL222 may be installed without the clock generator. The HL222 also offers a latching loopback capability.

**D-T**

**3.33** The block diagram in Fig. 16 shows the D-T HL7 and HL89. These CPs consist of five identical, balanced, line driver and line terminator circuits. They provide the means to interface up to five OCUs with an SRDM, a T1DM, T1WB4, or T1WB5. Each line terminator receives the byte-encoded, balanced, bipolar signal from an SRDM, a T1DM, T1WB4, or T1WB5 on the T and R leads; converts them to byte-encoded, logic-level signals, and delivers them to the OCUs. Conversely, byte-encoded, logic-level signals received from the OCU, are converted by the line driver to a byte-encoded, balanced, bipolar signal and delivered to the SRDM, T1DM, T1WB4, or T1WB5 on the T1 and R1 leads. Polarity steering signals are provided to the line driver by the OCU on the polarity pulse lead.

**3.34** The faceplate of D-T HL89 also contains six jacks which provide access to the five OCU channels between the OCU and the D-T circuit. When a plug is inserted into any one of jacks J1 through J5, the signal terminated on channels 1 through 5, respectively, and the signal on that channel can be checked by inserting the KS-20908 DTS (data test set) receiver plug into the TEST jack.

**HL8/HL8B ISMX**

**3.35** The ISMX HL8/HL8B (Fig. 17a) provides the means to multiplex the byte-encoded, logic-level output of five OCUs, operating at one of the subrate speeds, and to interface the resultant 64-kb/s balanced bipolar data signal to a single T1DM, T1WB4, T1WB5, or D3B/D4B channel if used in hybrid/dataport configuration. Each port of the ISMX receives the logic-level signals from the OCU and delivers logic-level signals to the OCU, while receiving clock signals from the CT&O. The five port circuits in the ISMX interface the OCUs to the ISMX and common circuits at the logic level. The ISMX and common circuits time and combine the data from the port circuits into one composite 64-kb/s logic-level signal, and separate the composite 64-kb/s signal received from the line terminator into five individual logic-level streams under control of the clock signals. If the ISMX is unable to obtain frame synchronization on the incoming composite 64-kb/s data stream from the T1DM, T1WB4, T1WB5, or D3B/D4B channel if used in hybrid/dataport configuration, the OS (out-of-sync) LED on the faceplate will be lighted. The line driver and line terminator circuits perform the same function as described for the D-T in paragraph 3.31. The 5-channel ISMXs perform the same function as the SRDM and for secondary channel operation have the same requirement of modification. That is, in the network-to-loop direction of transmission, where the subrate framing pattern is stripped, a one is placed in the bit 1 position. In the loop-to-network direction of transmission, secondary channel capability is limited to channels which have a one for a framing bit as described with the SRDM. Like the SRDM, the ISMX HL8B is utilized only if the drop side connects to other than an OCU or a tandem subrate multiplexer. The HL8B may be used in place of the HL8 with normal DDS service.

**HL88/HL88B ISMX**

**3.36** A simplified block diagram of the 10-channel ISMX is shown in Fig. 17b. The outputs of ten OCUs operating at the 2.4- and/or 4.8-kb/s subrate speeds are multiplexed into a single bipolar DS0 signal. This signal, at the output of the DR (driver), is transmitted to the port of a T1DM, T1WB4, T1WB5, or D3B/D4B in hybrid/dataport configuration. In the receive direction, the DS0 signal from the output port of a T1DM, T1WB4, or T1WB5 is converted to a logic-level signal by the terminator. The signal is then

demultiplexed and sent to the OCUs associated with the ISMX.

**3.37** The 10-channel ISMX performs the same function as the SRDM and for secondary channel operation has the same requirement of modification. That is, in the network-to-loop direction of transmission, where the subrate framing pattern is stripped, a one is placed in the bit 1 position. In the loop-to-network direction of transmission, secondary channel capability is limited to channels which have a one for a framing bit as described with the SRDM. Like the SRDM, the ISMX HL88B is utilized only if the drop side connects to other than an OCU or a tandem subrate multiplexer. The HL88B may be used in place of the HL88, with normal DDS service.

**3.38** The block diagram of the 10-channel ISMX multiplexer and failure detection circuit is shown in Fig. 18. The ISMX contains two identical multiplexers, one regular and one spare, with timing being supplied by the 8- and 64-kHz clock signals from the CT&O. The DATA OUT signals from up to ten OCUs appear at input ports on the multiplexer circuit. The frame generator enables each input port for a 1-byte interval through the port selector leads and inserts an F (framing) bit into the first bit of each byte through the F bit input on the multiplexer. The F bits are inserted into the ten bytes in each frame in a prescribed pattern so that each data channel can be identified within the frame. The output of the multiplexer is a serial data stream consisting of the ten multiplexed channels containing data and framing information. This signal is then delayed to obtain proper byte alignment and sent through the output switch to the driver where the logic-level signal is converted to the bipolar DS0 format.

**3.39** The multiplexer failure detection circuit continually monitors the F bits in both the regular and spare multiplexed data streams. A failure within the regular multiplexer circuitry will cause F bit errors which will be detected in the failure detection circuit. A third frame generator is employed to make the decision as to whether the failure occurred in the regular or spare multiplexer. Framing bit errors which occur during four consecutive frames in the regular multiplexer cause the failure detection circuitry to switch the spare multiplexer into service via logic gates in the output switch.

**3.40** A switch from the regular to the spare multiplexer activates the alarm circuit on the HL88 by turning the ALM indicator on and by sending a minor alarm signal to the BCPA circuit or to the LTS. Detector circuits in both the regular and spare timing circuits monitor the 64-kHz clock signal. Loss of clock on HL88 results in the CFR (clock failure regular) and/or CFS (clock failure spare) LEDs being lighted and the alarm circuit being activated.

**3.41** A block diagram of the 10-channel ISMX demultiplexer and failure detection circuit is shown in Fig. 19. The ISMX contains a regular and a spare demultiplexer which are identical and obtain their timing from the timing circuit shown in Fig. 18. The DS0 signal from an output port on a T1DM, T1WB4, or D3B/D4B is converted to a logic-level signal by the TERM (terminator). This signal is composed of frames which are ten bytes long and contain a framing pattern made up of the first bit out of each byte. The framing pattern identifies the location of each channel in a frame so that each demultiplexed channel signal appears at the correct output channel.

**3.42** The frame generator puts out a framing pattern identical to the F bits in the incoming data signal. The sync detector and timer circuit monitor this framing pattern and the F bits to see if they are identical. When these signals do not agree after six F bits (due to loss of incoming signal, etc.), the timer expires and lights the ISR (in-sync regular) and ISS (in-sync spare) LEDs which indicate demultiplexer out-of-sync. The incoming signal is allowed to pass through the frame generator. When 12 valid F bits appear in the received signal, the frame generator realigns itself with this signal and resets the sync detector and timer circuit. The ISR and ISS LEDs go off, indicating that the demultiplexer is in sync.

**3.43** After leaving the frame generator, the multiplexed data signal enters the scanner, which is a 10-stage shift register, where it is split into the ten individual signals. Each individual channel signal then enters a recirculating channel register where each byte is repeated nine times; thus, the output of each channel register is ten identical 8-bit bytes for each byte at the input. The signals then pass through the channel output switches and go to the DATA IN inputs on the OCUs.

**3.44** The demultiplexer failure detection circuit continually monitors and compares the outputs of each pair of regular and spare channel registers. Bit errors at the output of any register during

four consecutive frame intervals result in a test word being generated and inserted into the spare demultiplexer. The generated test word is then compared with the outputs of each spare channel register and these signals should agree if the spare demultiplexer is operating properly. When the test word successfully passes through the spare demultiplexer, the regular demultiplexer is removed from service and the spare is switched into service by a switch consisting of logic-level gates. When a switch takes place, the alarm circuit (Fig. 18) is activated as previously described. When a failure occurs in the spare demultiplexer, a switch does not take place but the alarm circuit is activated to indicate a circuit failure condition.


***When the HL88/HL88B ISMX is first installed in the OCU shelf, the circuit must be initialized to ensure that flip-flops start up in their proper state. This is accomplished by momentarily grounding test points TP1 and TP2 via the ground furnished at test point TP27. If this is not done, the spare circuits may be switched into service and an alarm activated even though no trouble condition exists.***

### CT&O

**3.45** The block diagram in Fig. 20 shows the CT&O HL9. This CT&O accepts the office 8- and 64-kHz clock signals from the LTS or BCPA shelf and provides a number of timing signals to the CLKG or OCUs (HL201, 202, 203, and 220). These timing signals are in phase-lock with the office clocks.

**3.46** The 8- and 64-kHz office clock signals are converted to logic-level signals by the differential terminators TERM 1 and TERM 2, respectively. These logic-level signals are then used to provide reference for the countdown circuits and the phase-locked crystal oscillator in HL9 and for clock signals to the HL8 or HL88 ISMX when they are used in each associated half-shelf or whole shelf, respectively. All the other timing signals generated by the CT&O are derived from the VCO (voltage controlled oscillator) circuit by the countdown circuit. The 64-kb/s clock pulses are derived directly for delivery to all CLKGs. Various other rate pulses are delivered to the CLKG or OCUs (HL201, 202, 203, and 220) via the clock pulse gate circuits. The 64-kHz office clock and the derived 64-kHz signal from the VCO are fed to the phase comparator circuit which provides the signal that keeps the VCO output in phase locked with the 64-kHz office clocks. The byte phase sync circuit provides a timing signal that is phase-locked to the 8-kHz office clock.

### CLKG

**3.47** The block diagram in Fig. 21 shows the CLKGs HL80, HL5, and HL6. These CLKGs use the timing signals provided by the CT&O to generate the clock pulses required by some of the OCUs (HL1 through 4, 141, and 142) for rate matching, etc. The buffer gate circuits distribute two phases of 64-kb/s clock pulses to provide the sampling and transmit pulses for the 64-kb/s intraoffice signals. Other timing signals are fed to the countdown circuit either directly in the 56-kb/s CLKG HL6, via the ÷4 circuit in the 2.4-kb/s CLKG HL80, or via the rate selector circuit in the 4.8/9.6-kb/s CLKG HL5. Screw switches on the 4.8/9.6-kb/s CLKG provide the means for selecting either the 4.8- or 9.6-kb/s customer service rate. Outputs of the countdown circuit are gated by the transfer sequence and control signal gates and by the bit-rate clock gates to provide the byte sequence timing pulses and the customer service rate timing pulses to all five OCUs in the associated half-shelf.

*Note:* When all of the OCUs in an equipment half-shelf are HL201, 202, 203, or 220, a CLKG is not required for that particular half-shelf.

## D. OCU Assembly Power Supply Shelf Description (Fig. 22)

**3.48** A fully equipped OCU assembly power supply shelf is capable of providing +12, −12, and +5 V dc to the OCUs in the mounting shelves of the 3-shelf OCU assembly of which it is a part, and to one 2-shelf OCU assembly. The shelf consists of two or three power units (71C, 71C1, 76C, or 76C1) and a logic and alarm circuit pack (ED-82512). The +12, −12, and +5 voltages are derived from the −48 or −24 V dc central office battery by the power units. The shelf also serves as a distribution point for the office battery to the OCU simplex current circuits and the office 8- and 64-kHz clocks to the CT&O in each of the four OCU mounting shelves. A fuse panel at the right-hand end of the power supply shelf provides ▶three fuses for distributing redundant power to the protection relay logic in the three power units and in the logic and alarm circuit.◀

**3.49** ▶Seven fused office battery lines are provided by the LTS or BCPA shelf that serves as the office battery distribution point within the equipment bays. Three of these leads serve the power units via the fuses mentioned above. The other four leads provide power to the OCU simplex current circuits in each associated OCU mounting shelf.◀

*Note:* The three battery fuses should be provided in the BCPA shelf even though all three power units in the power supply shelf are not required. If one of the power units in the power supply shelf fails and a replacement is not immediately available, the power unit battery fuse in the BCPA shelf should be removed until a replacement is available.

**3.50** The equipment bay is provided with three ground systems which are physically separated from each other. These are the structural (frame) ground, −48 or −24 volt primary distribution ground, and signal ground. All three of the grounds are provided to each OCU assembly power supply shelf and connected to the office ground system at the top of the bay.

**3.51** The LOAD 1 power unit provides voltages to the two equipment shelves in the 3-shelf OCU assembly of which it is a part, and the LOAD 2 power unit provides the voltages to an associated 2-shelf OCU assembly. The spare power unit provides backup power to either the LOAD 1 or LOAD 2 power unit should the associated power unit fail. The logic and alarm circuit provides circuitry to switch in the spare power unit on a primary power unit failure. The circuit also provides circuitry to close relay circuitry for major and minor alarms in the LTS or BCPA shelf.

**3.52** Whenever the office battery is initially applied to a power unit, the ALARM RESET switch on the power unit front panel must be momentarily operated to activate the unit. With all three power units activated, the LOAD 1 power unit provides power to shelves A and B of the primary OCU assembly, the LOAD 2 power unit provides power to TS1C and TS2C for connection to a 2-shelf OCU assembly, and the spare power unit is on standby.

**3.53** Should any single power unit fail, the logic and alarm circuit will activate a minor alarm in the LTS or BCPA shelf. In addition, if the faulty unit is the LOAD 1 or LOAD 2 power unit and a spare power unit is installed in the shelf, the following events will occur simultaneously.

***Caution: If the spare power unit is not installed in the shelf, the major alarm will be activated, the FAILURE indicator on the faulty unit will be lighted, and service to the customers served by the OCUs powered by the faulty unit will be interrupted.***

(1) The output of the faulty unit will be replaced by that of the spare power unit.

(2) The FAILURE and SPARE CONN indicators on a faulty 71C or 76C power unit or the FAILURE and TRANS OUT indicators on a faulty 71C1 or 76C1 power unit will light.

(3) The logic and alarm circuit will inhibit the possible switch-over of the spare power unit to the other power unit position should that unit also fail.

(4) The appropriate SPARE CONNECTED TO indicator on the logic and alarm circuit will light in accordance with the power unit which has failed (LOAD 1 or LOAD 2).

In the event that a second power unit fails, the logic and alarm circuit will activate a major alarm in the LTS or BCPA shelf. The exception to this would be when the second power unit failure occurs in the spare power unit while the first power unit that has failed is removed from the shelf. It is imperative that the failed power unit be replaced with a working power unit as soon as possible to prevent interruption of customer service and erroneous alarm indications. The power unit failure alarms and transfer indications are listed in Table I.

***Warning: If a power supply shelf equipped with 76C or 76C1 power units is connected to a −48 volt office supply with screw switches S1A and S1B closed, a minor alarm will be activated until the logic and alarm circuit is removed from the shelf. Damage to the 76C or 76C1 power units may also occur.***

**3.54** The logic and alarm circuit is equipped with two screw switches (S1A and S1B) which must be set according to the central office battery voltage. The logic and alarm circuit comes from the factory

with the screw switches arranged for use with −48 volt office supply (screw switches S1A and S1B open). If the unit is to be used with −24 volt office supply, these screw switches must be closed.

## 4. GLOSSARY

**4.01** The following descriptions are included as an aid to the reader in understanding this practice.

- ***Local Channel*** — The connecting circuits between the customer and the first DDS office. This includes the DSU or CSU at the customer location, the 4-wire transmission pairs, and the OCU at the DDS office.

- ***Customer Service Rate*** — Data transmission speed of the customer station. In private line service, this is 2.4, 4.8, 9.6, or 56 kb/s with or without secondary channel service.

- ***Subrate*** — The 2.4-, 4.8-, and 9.6-kb/s customer service rates.

- ***DSX-0A (hub office only)*** — The cross-connect located between the 950-type testboard and OCU assemblies, an SRDM, or a T1 data multiplexer (T1DM, T1WB4, or T1WB5).

- ***Intraoffice Distribution Rate*** — The speed at which data is transmitted between the OCU assemblies and an SRDM, T1DM, T1WB4, or T1WB5. In the DDS, this is 64 kb/s.

- ***Local Office*** — A DDS office that concentrates customer circuits into T1 data streams that can be transmitted to a hub office.

- ***End Office*** — Any DDS local office that passes on toward the hub office, only circuits that enter the office over local channels.

- ***Intermediate Office*** — Any DDS local office that passes on toward the hub office, circuits that enter the office over T1 lines in addition to those that enter over local channels.

- ***Hub Office*** — Any DDS office that provides the DSX-0 cross-connect and combines the T1 data streams from a number of local offices into signals suitable for transmission over DDS facilities and/or provides the STC with test access. It may also serve as a local office for customers geographically located within the local channel cable length restrictions.

- ***M-JCP (intermediate and end offices only)*** — The multiplexer jack and connector panel located between a T1DM or T1WB4 and an OCU shelf which provides cable interconnections and test access at the 64-kb/s level.

- ***SM-JCP (end offices only)*** — The submultiplexer jack and connector panel located between an SRDM and an OCU shelf which provides cable interconnections and test access at the 64-kb/s level.

- ***Office Channel Unit*** — The office channel unit contains the logic and line interface circuitry for converting data signals from the intraoffice distribution rate to the customer service rate and vice versa.

- ***Loop Side Interface*** — The LSI provides subrate data port channel access to an ISMX and provides access for 56-kb/s channels to an HL89 D-T.

- ***2.4-kb Clock Generator*** — The HL80 provides the timing and clock pulses required by the 2.4-kb/s OCU HL1.

- ***4.8/9.6-kb Clock Generator*** — The HL5 provides the timing and clock pulses required by the 4.8- and 9.6-kb/s OCUs (HL2, HL3, and HL142).

- ***56-kb Clock Generator*** — The HL6 provides the timing and clock pulses required by the 56-kb/s OCUs (HL4 and HL141).

- ***Common Timing and Oscillator*** — The HL9 provides the timing and clock pulses required by the CLKG (HL80, HL5, or HL6) or OCUs (HL201, 202, 203, HL220, HL225, and LSI HL222).

- ***Driver-Terminator*** — The HL7 and HL89 interface five OCUs that are in one-half of an OCU shelf to five ports of an SRDM or a T1 multiplexer (T1DM, T1WB4, or T1WB5).

- ***5-Channel Integral Subrate Multiplexer*** — The HL8 multiplexes the signals from five subrate OCUs that are in one-half of an OCU shelf and interfaces the resultant composite 64-kb/s data stream to a single port of a T1DM, T1WB4, or T1WB5. The HL8B is required for secondary channel capability.

- ***10-Channel Integral Subrate Multiplexer*** — The HL88 multiplexes the signals from 10 subrate OCUs (at 2.4- and/or 4.8-kb/s) that are in a whole OCU shelf and interfaces the resultant composite 64-kb/s data stream to a single port of a T1DM, T1WB4, or T1WB5. The HL88B is required for secondary channel capability.

- ***3-Shelf Office Channel Unit Assembly*** — A J70177AA 3-shelf OCU and power supply assembly, consisting of two equipment shelves, for mounting the OCU, CLKG, CT&O, and D-T or ISMX required for up to 20 OCU channels. The third shelf is for mounting up to three power units and a logic and alarm circuit pack.

- ***2-Shelf Office Channel Unit Assembly*** — A J70177AB 2-shelf OCU assembly consisting of two equipment shelves for mounting the OCU, CLKG, CT&O, and D-T or ISMX required for up to 20 OCU channels. Power and timing are supplied to this assembly by a 3-shelf OCU assembly.

## 5. REFERENCES

5.01 The following SDs (schematic drawings), CDs (circuit descriptions), and AT&T Practices pertain to the 3-shelf and 2-shelf OCU assemblies.

| NUMBER | TITLE |
|---|---|
| SD-73074-01<br>CD-73074-01 | Digital Data System—Central Office—Office Channel Units and Auxiliary Circuits |
| SD-73087-01<br>CD-73087-01 | Digital Data System—Central Office—System Interconnection and Application Schematic |

| PRACTICE | TITLE |
|---|---|
| 314-410-310 | Local Loop—Maintenance Procedures—Digital Data System |
| 314-910-300 | Office Channel Unit and Auxiliary Circuits—Maintenance Procedures — Digital Data System |
| 314-910-500 | Office Channel Unit and Auxiliary Circuits—Test Procedures—Digital Data System |

## 6. ISSUING ORGANIZATION

Published by
The AT&T Documentation Management Organization

**TABLE A**

**POWER UNITS CONTAINED IN POWER SUPPLY SHELF**

| POWER UNITS | CENTRAL OFFICE SUPPLY (VOLTS) |
|---|---|
| 71C (Mfg Disc.)<br>71C1 | −48 |
| 76C (Mfg Disc.)<br>76C1 | −24 |

**TABLE B**

**CIRCUIT PACK OPTIONS**

| CIRCUIT PACK | OPTION | FEATURE | SWITCH | SWITCH POSITION |
|---|---|---|---|---|
| HL1-4<br>HL141, 142<br>HL201 - 203<br>(Fig. 4) | WW | FLBO network removed | S1, S2 | Closed |
| | | | S3, S4 | Open |
| | WV | FLBO network installed | S1, S2 | Open |
| | | | S3, S4 | Closed |
| HL5<br>(Fig. 5) | Y | 4.8-kb/s service | S1 | Closed |
| | | | S2 | Open |
| | X | 9.6-kb/s service | S1, S2 | Closed |
| HL201 - 203<br>(Fig. 4) | A | CRTC option removed | S5 | Open |
| | B | CRTC option installed | S5 | Closed |
| | E | CRCT option removed | S6 | Open |
| | F | CRCT option installed | S6 | Closed |
| Logic and Alarm Circuit<br>ED-82512 | T | –24 volts CO battery | S1A, S1B | Closed |
| | U | –48 volts CO battery | S1A, S1B | Open |
| | | | | DEPRESS SECTION OF SWITCH (NOTE 1) |
| HL141, 142<br>(Fig. 4) | A | CRTC option removed | S5 | Opposite to #4 |
| | B | CRTC option installed | S5 | Adjacent to #4 |
| | E | CRCT option removed | S5 | Opposite to #3 |
| | F* | CRCT option installed | S5 | Adjacent to #3 |

***Note 1:*** Depress switch sections firmly until a snap occurs.

* Must not be used on HL141 when option ZZ is installed.

**TABLE C**

**OPTIONS FOR HL96 SWITCHES S1 AND S2**

| SOURCE OF CLOCK | POSITION OF SWITCHES S1 AND S2 |
|---|---|
| HL80 (2.4 kb/s) | NORMAL (A) |
| HL5 or HL6 | OPERATED (B) |

**TABLE D**

**OPTIONS FOR HL96 SWITCHES S3 AND S4**

| DATA INPUT | POSITION OF SWITCHES S3 AND S4 |
|---|---|
| HL7 or HL89 | NORMAL (A) |
| ISMX | OPERATED (B) |

**TABLE E**

**TRANSMISSION RATE CAPABILITIES FOR PRIMARY, SECONDARY, AND OVERALL CHANNELS**

| DATA/SIGNAL (NOTE 1) | PRIMARY CH RATE | SECONDARY CH RATE | OVERALL CH RATE AT NETWORK INTERFACE |
|---|---|---|---|
| $D_1D_2D_3D_4D_5D_6$,F, C/S | 2.4 kb/s | 133 1/3 b/s | 3.2 kb/s |
| $D_1D_2D_3D_4D_5D_6$,F, C/S | 4.8 kb/s | 266 2/3 b/s | 6.4 kb/s |
| $D_1D_2D_3D_4D_5D_6$,F, C/S | 9.6 kb/s | 533 1/3 b/s | 12.8 kb/s |
| $D_1D_2D_3D_4D_5D_6D_7$,F, C/S | 56.0 kb/s | 2666 2/3 b/s | 72.0 kb/s |

***Note 1:*** $D_{1\text{-}7}$ = Primary Channel Data

F = Framing Signal (Repeated 101100 Pattern)

C/S = Shared Secondary Channel Data (S) and Network Control (C) Information (Repeated SCC Pattern)

**TABLE F**

**DATA AND STUFF BYTES REQUIRED FOR RATE MATCHING IN SUBRATE OCU MODULES**

| OCU MODULE | BIT RATE | DATA BYTES | STUFF BYTES | TOTAL BYTES |
|---|---|---|---|---|
| HL1 and HL201 | 2.4 kb/s | 1 | 19 | 20 |
| HL2 and HL202 | 4.8 kb/s | 1 | 9 | 10 |
| HL3, HL142, and HL203 | 9.6 kb/s | 1 | 4 | 5 |

**TABLE G**

**PATTERN MONITOR CIRCUIT BIT SEQUENCE DETECTION**

| SEQUENCE MEANING | BITS | | | | | | | PATTERN MONITOR CIRCUIT RESPONSE |
|---|---|---|---|---|---|---|---|---|
| | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
| All 0s data | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Signals bipolar encoder to insert bipolar violation. |
| All 0s control mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Signals bipolar encoder to inhibit bipolar violation. |
| OCU loopback test | 0 | 1 | 0 | 1 | 0 | 1 | 0 | Signals bipolar encoder to insert bipolar violation and generates OCU LOOPBACK signal. |
| CHAN loopback test | 0 | 1 | 0 | 1 | 0 | 0 | 0 | Generates CHAN LOOPBACK signal and inhibits insertion of bipolar violation |
| Idle code | 1 | 1 | 1 | 1 | 1 | 1 | 0 | Signals bipolar encoder to insert bipolar violation |
| DSU loopback test | 0 | 1 | 0 | 1 | 1 | 0 | 0 | |
| MUX out-of-sync | 0 | 0 | 1 | 1 | 0 | 1 | 0 | |
| Test code | 0 | 0 | 1 | 1 | 1 | 0 | 0 | |
| Unassigned MUX channel | 0 | 0 | 1 | 1 | 0 | 0 | 0 | |

**TABLE H**

**LOCAL LOOP TO DS-0 CODE MAPPING FOR HL141, 142, AND 201, 202, 203**

| LOCAL LOOP CODE (BITS 2-7) | DS-0 BITS | | | | | | | CODE DEFINITION |
|---|---|---|---|---|---|---|---|---|
| | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
| 000X0V | | | | | | | | Zero suppression, data mode 000000 |
| 001X0V | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Future use |
| 010X0V | 0 | 1 | 0 | 1 | 1 | 0 | 0* | |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1† | DSU loopback signal |
| | 0 | 1 | 0 | X | 0 | 1 | 1‡ | |
| 011X0V | 0 | 1 | 1 | 0 | 0 | 1 | 0 | Future use |
| 100X0V | 1 | 0 | 0 | 0 | 0 | 1 | 0 | Future use |
| 101X0V | 1 | 1 | 1 | 1 | 0 | 1 | 0 | NR (Not ready) code used in SDDS |
| 110X0V | 1 | 1 | 0 | 1 | 0 | 1 | 0 | DME (Data mode extension) |
| 111X0V | 1 | 1 | 1 | 1 | 1 | 1 | 0 | Idle |

* This code is present when the CRCT option is installed and the loopback flywheel is not in OCU loopback state.

† This code is present when the loopback flywheel is in the OCU loopback state.

‡ This code is present when the CRCT option is not installed and the loopback flywheel is not in OCU loopback state.

**TABLE I**

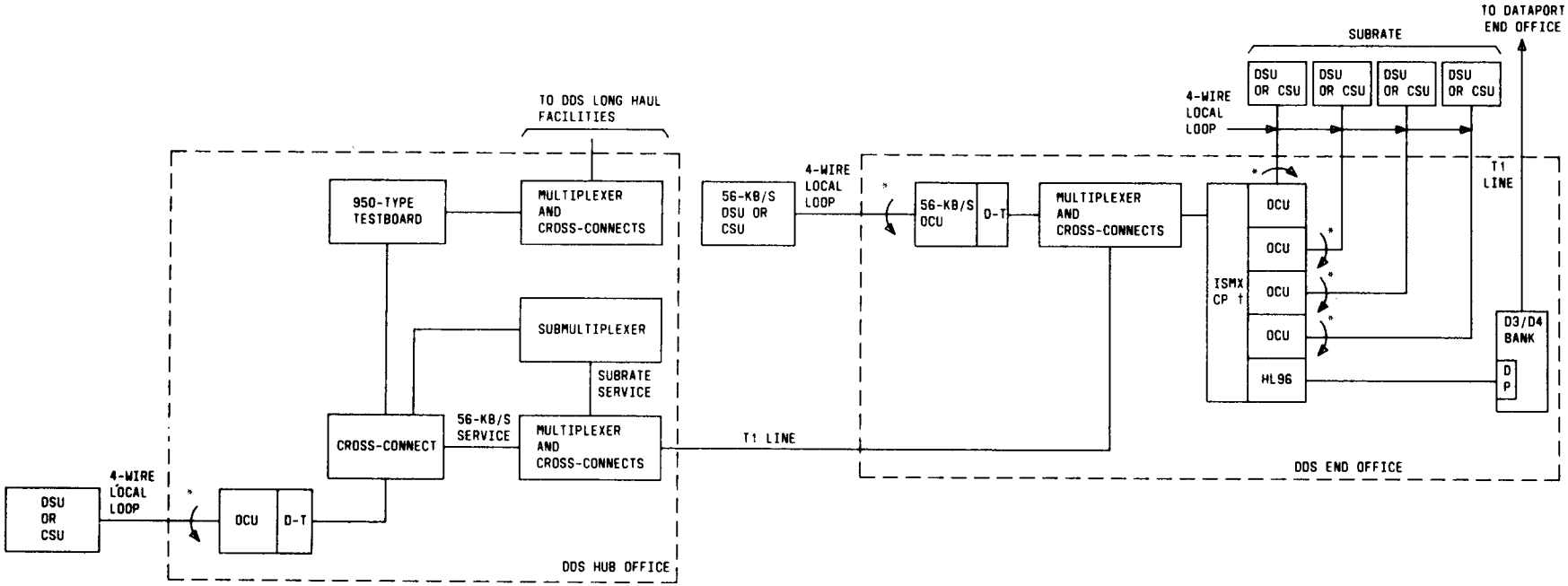
**POWER UNIT FAILURE ALARMS AND TRANSFER INDICATIONS**

| FAILED POWER UNIT | TYPE ALARM* | LOAD 1 POWER UNIT LED LIGHTED | | LOAD 2 POWER UNIT LED LIGHTED | | POWER UNIT | LOGIC AND ALARM CIRCUIT LED SPARE CONNECTED TO | |
|---|---|---|---|---|---|---|---|---|
| | | FAILURE | TRANSFERRED OUT | FAILURE | TRANSFERRED OUTFAILURE | LOAD 1 | LOAD 2 | |
| Power Unit 1 | Minor | ✓ | ✓ | — | — | — | ✓ | — |
| Power Unit 2 | | — | — | ✓ | ✓ | — | — | ✓ |
| Spare | | — | — | — | — | ✓ | — | — |
| Power Unit 1 and Power Unit 2 | Major | † | † | † | † | — | † | † |
| Power Unit 1 and Spare‡ | | ✓ | ✓ | — | — | ✓ | ✓ | — |
| Power Unit 2 and Spare‡ | | — | — | ✓ | ✓ | ✓ | — | ✓ |

* Alarm activated at LTS or BCPA shelf.

† Dependent upon which power unit fails first.

‡ A major alarm will not be activated if the spare power unit fails while the failed power unit (1 or 2) is removed from the shelf and a replacement has not been installed.



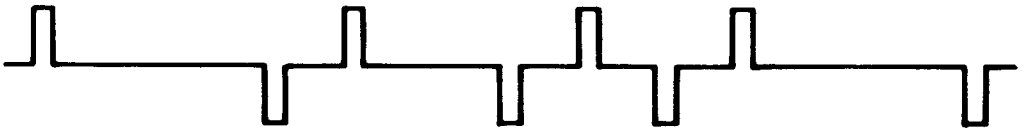

LEGEND:
CSU - CHANNEL SERVICE UNIT
CTC - CENTRAL TEST CENTER
DP - DATAPORT CHANNEL UNIT
OSU - DATA SERVICE UNIT
OCU - OFFICE CHANNEL UNIT

* CTC CONTROLLED OCU LOOPBACK POINT
† THE ISMX MAY BE HL8/HL88 (5 OCUs) OR HL88/HL888 (10 OCUs)

**Fig. 1—Block Diagram of Typical DDS Arrangement**

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BINARY | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| BIPOLAR | + | 0 | 0 | − | + | 0 | − | + | − | + | 0 | 0 | − |

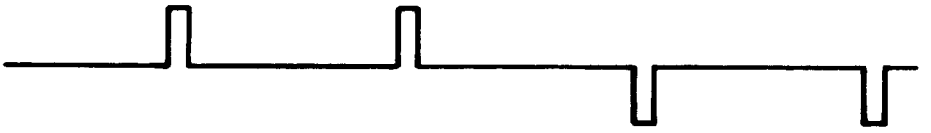
VOLTAGE WAVEFORM



WITHOUT VIOLATIONS

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BINARY | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| BIPOLAR | 0 | 0 | B | 0 | 0 | V | 0 | 0 | B | 0 | 0 | V |

VOLTAGE WAVEFORM



WITH VIOLATIONS

NOTE:

B – DENOTES THE TRANSMISSION OF A POSITIVE OR NEGATIVE VOLTAGE PULSE DETERMINED BY THE BIPOLAR RULE.

V – DENOTES THE TRANSMISSION OF A POSITIVE OR NEGATIVE VOLTAGE PULSE IN VIOLATION OF THE BIPOLAR RULE.

Fig. 2—Bipolar Sequences

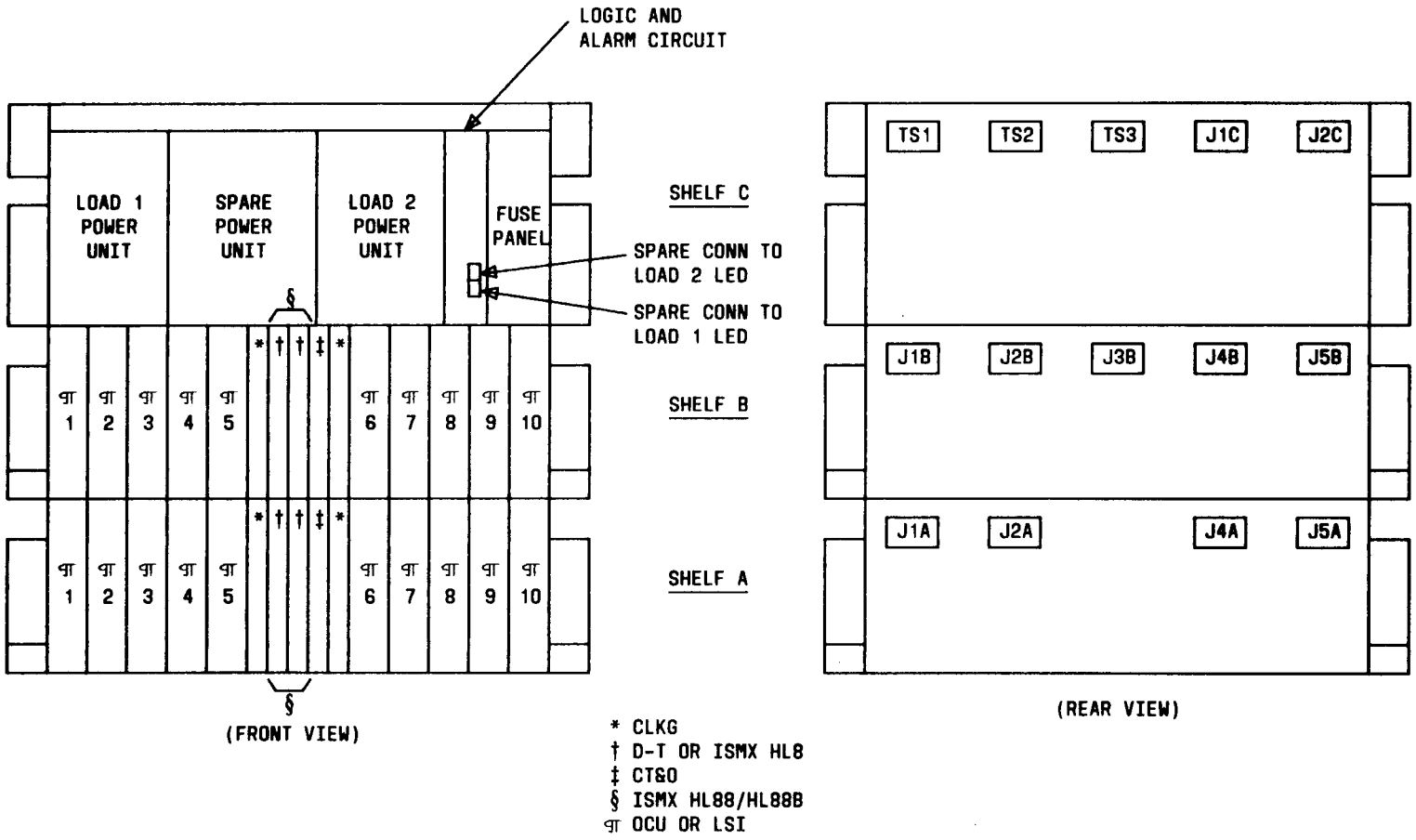



Fig. 3—3-Shelf OCU and Power Supply Assembly

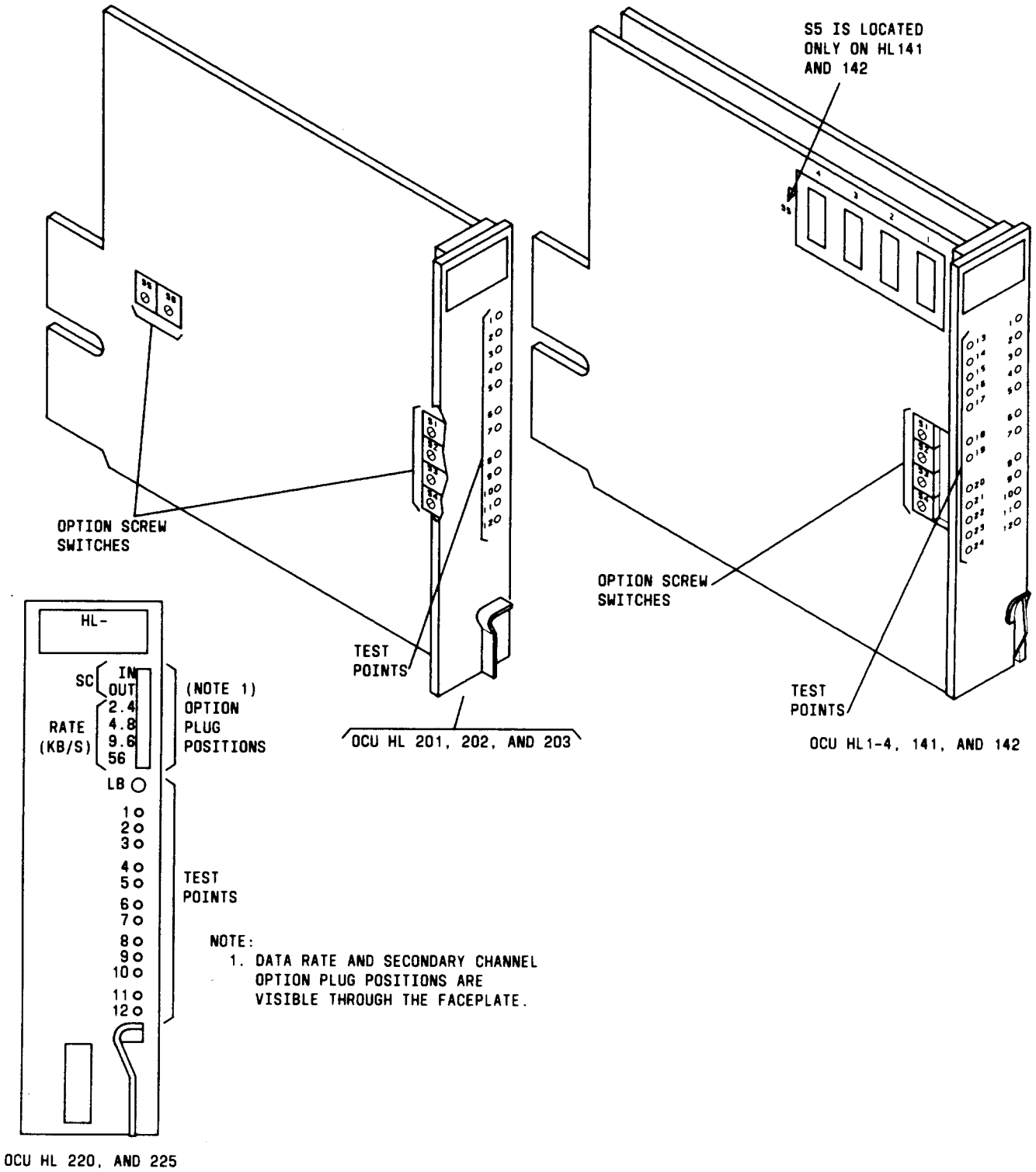



**Fig. 4—Office Channel Unit Test Points and Screw Switches (HL1-4, 141, 142, 201, 202, 203, 220, and 225)**

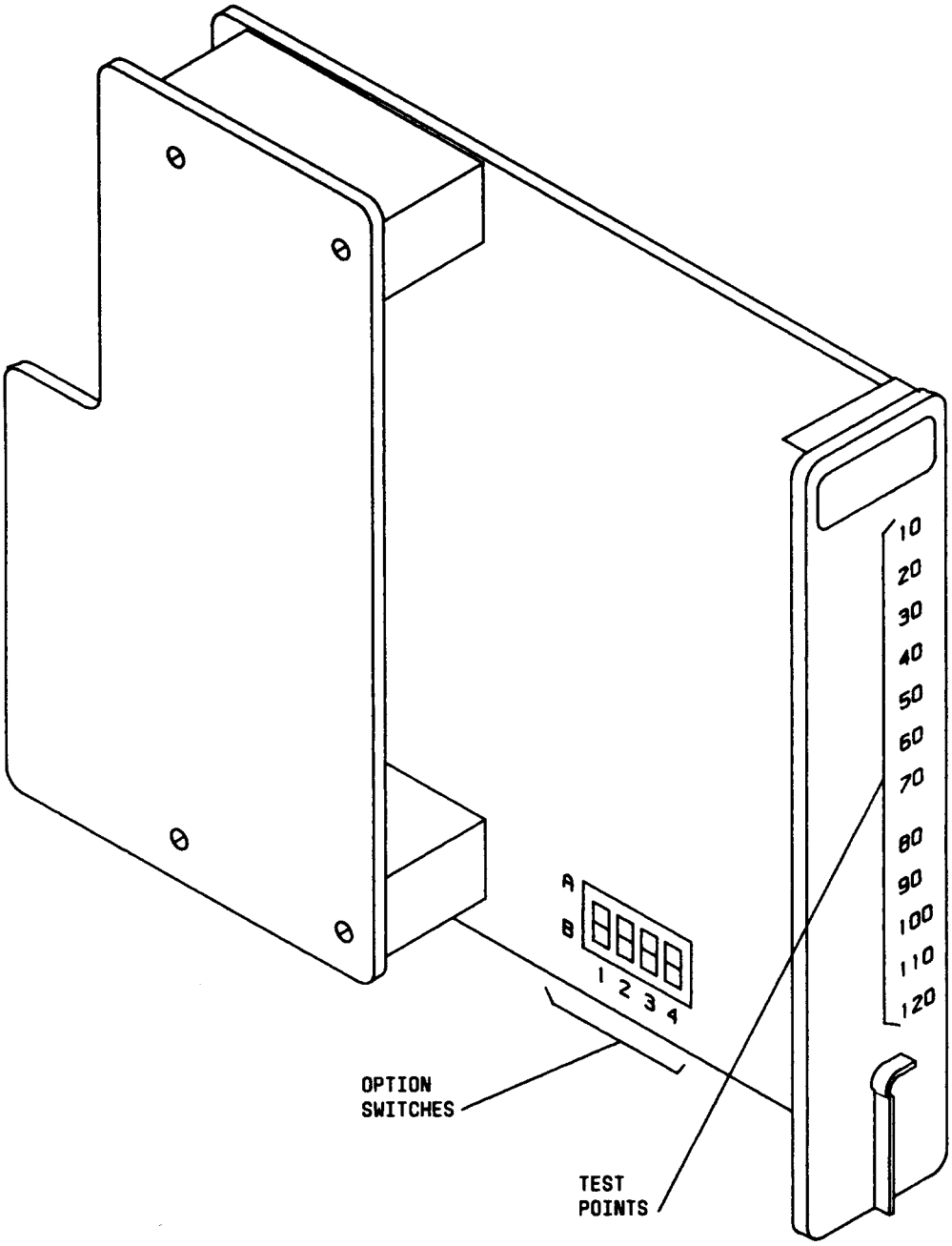



Fig. 5—LSI (Loop-Side Interface) HL96

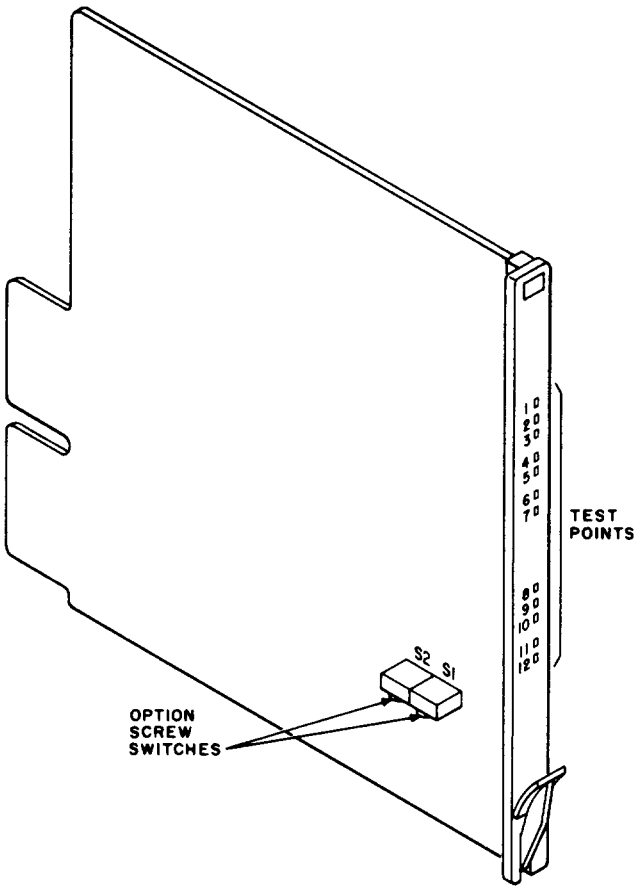



Fig. 6—4.8/9.6-Kb/s CLKG HL5

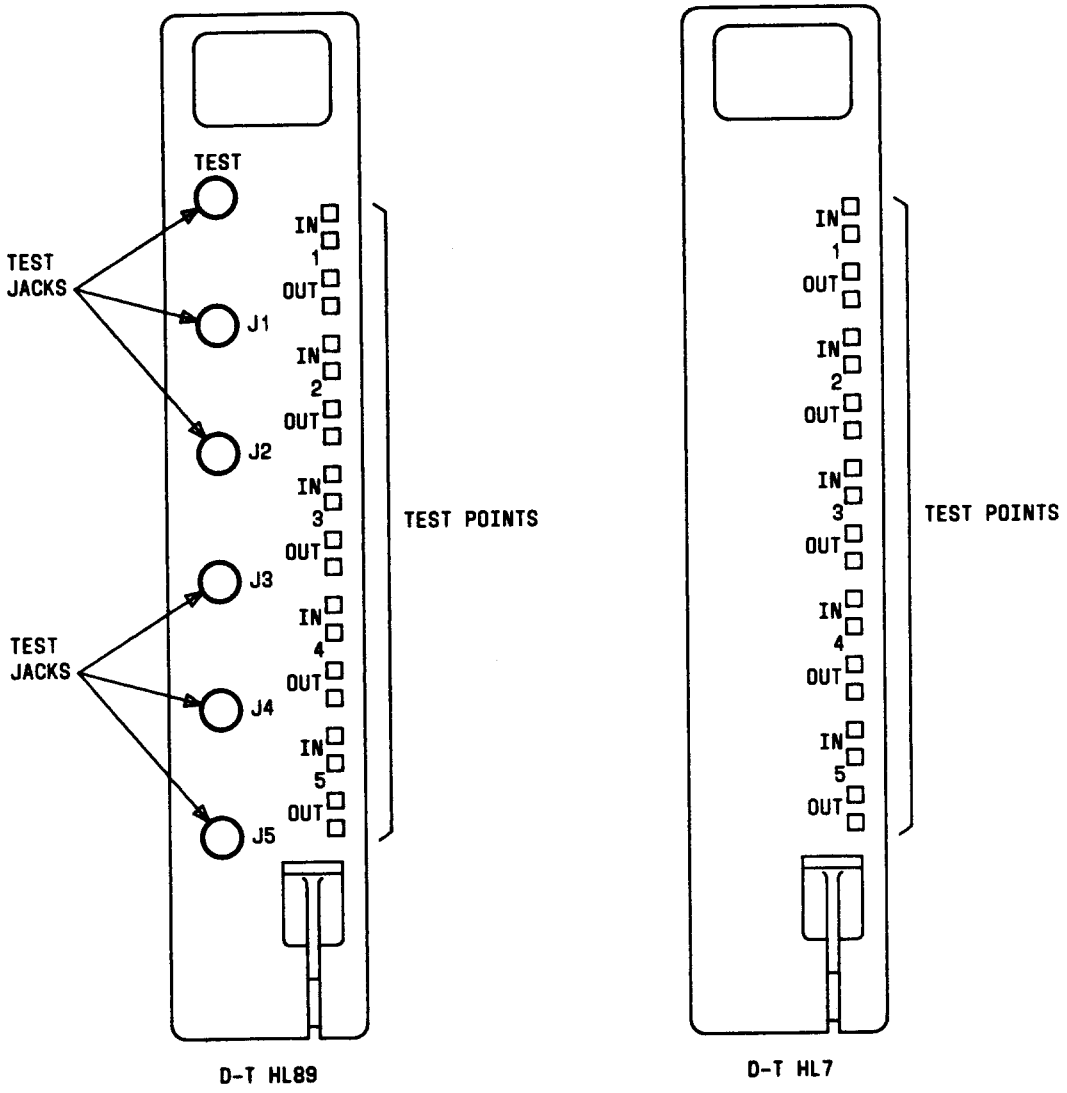



**Fig. 7—D-T HL7 and HL89**

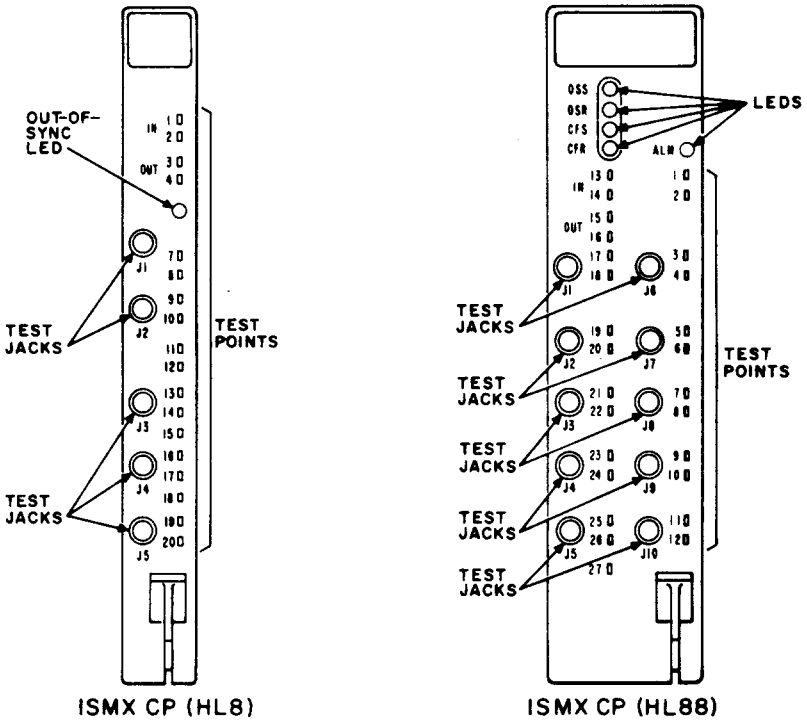



**Fig. 8—ISMX HL8/HL8B and HL88/HL88B**

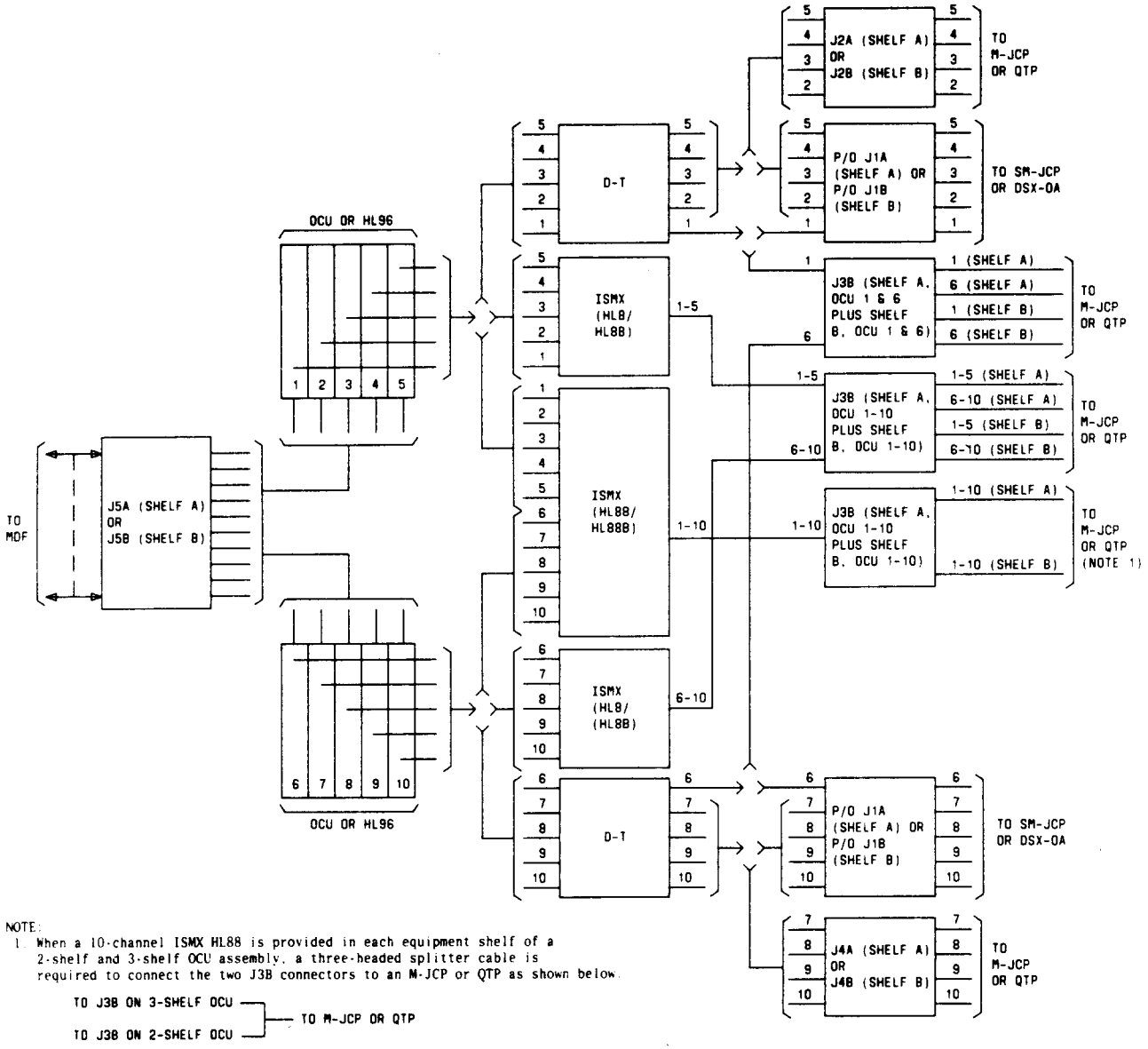



**Fig. 9—Relationship of OCU Channels to Connectors per Shelf**

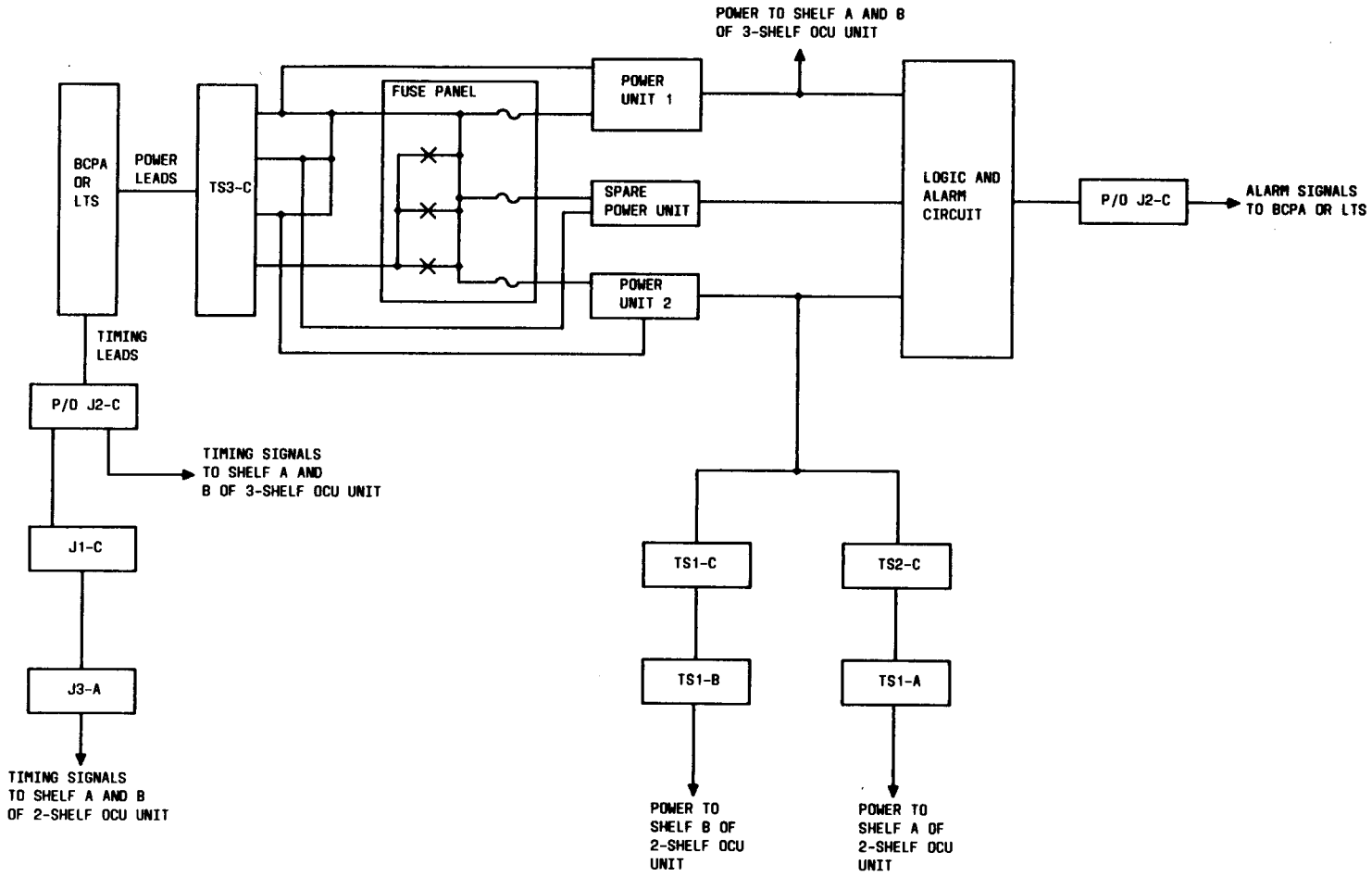



**Fig. 10—Connectors Supplying Power and Timing Signals to OCU Shelves**

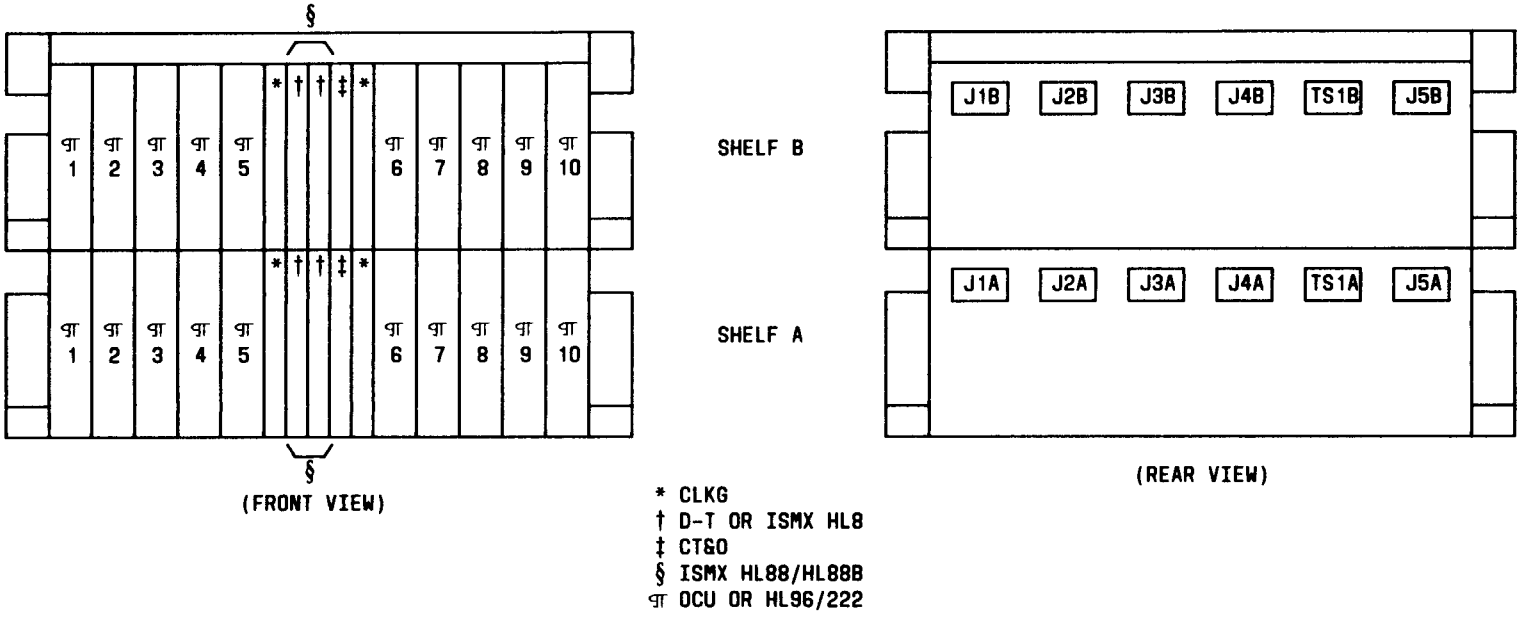



Fig. 11—2-Shelf OCU Assembly

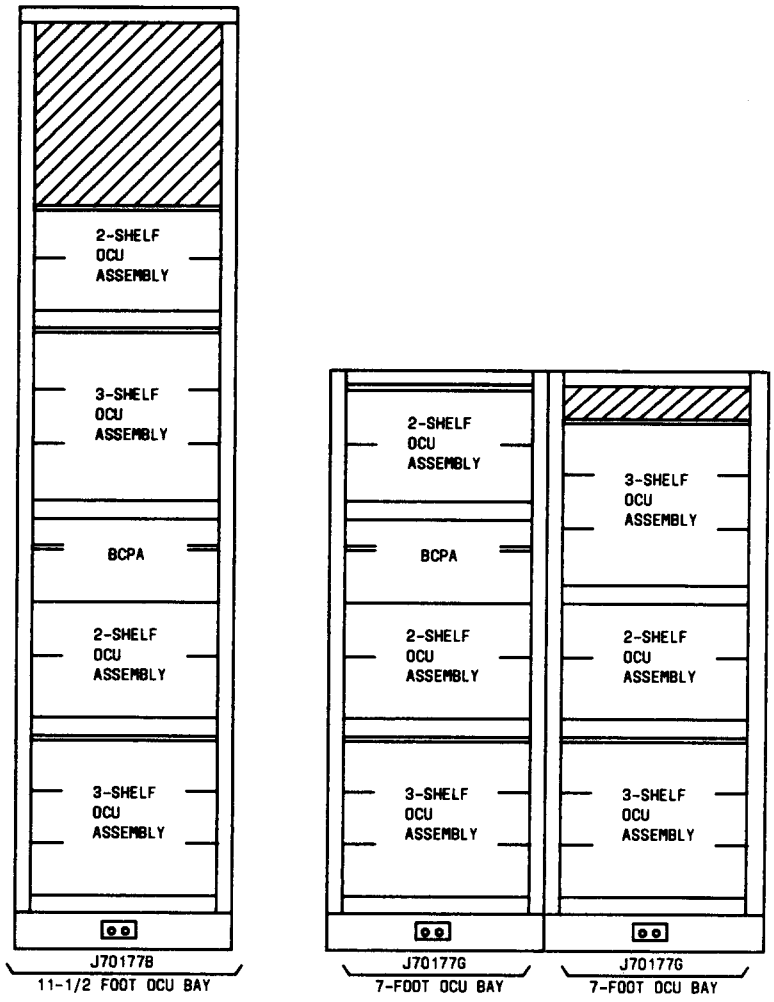
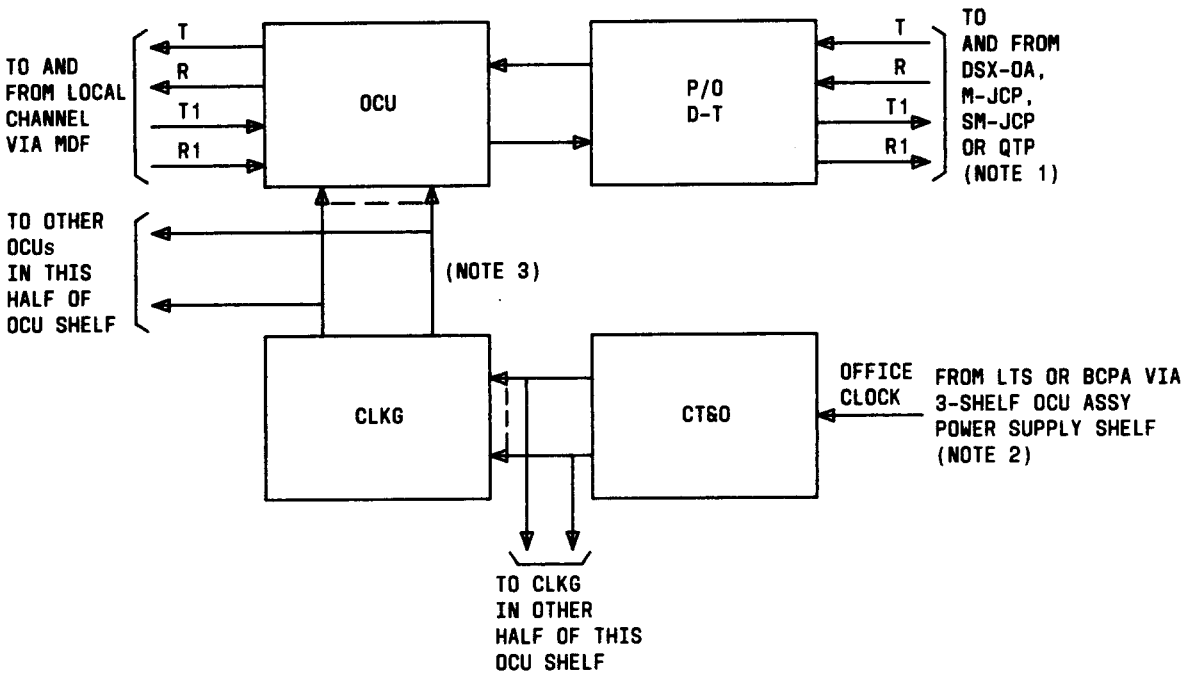
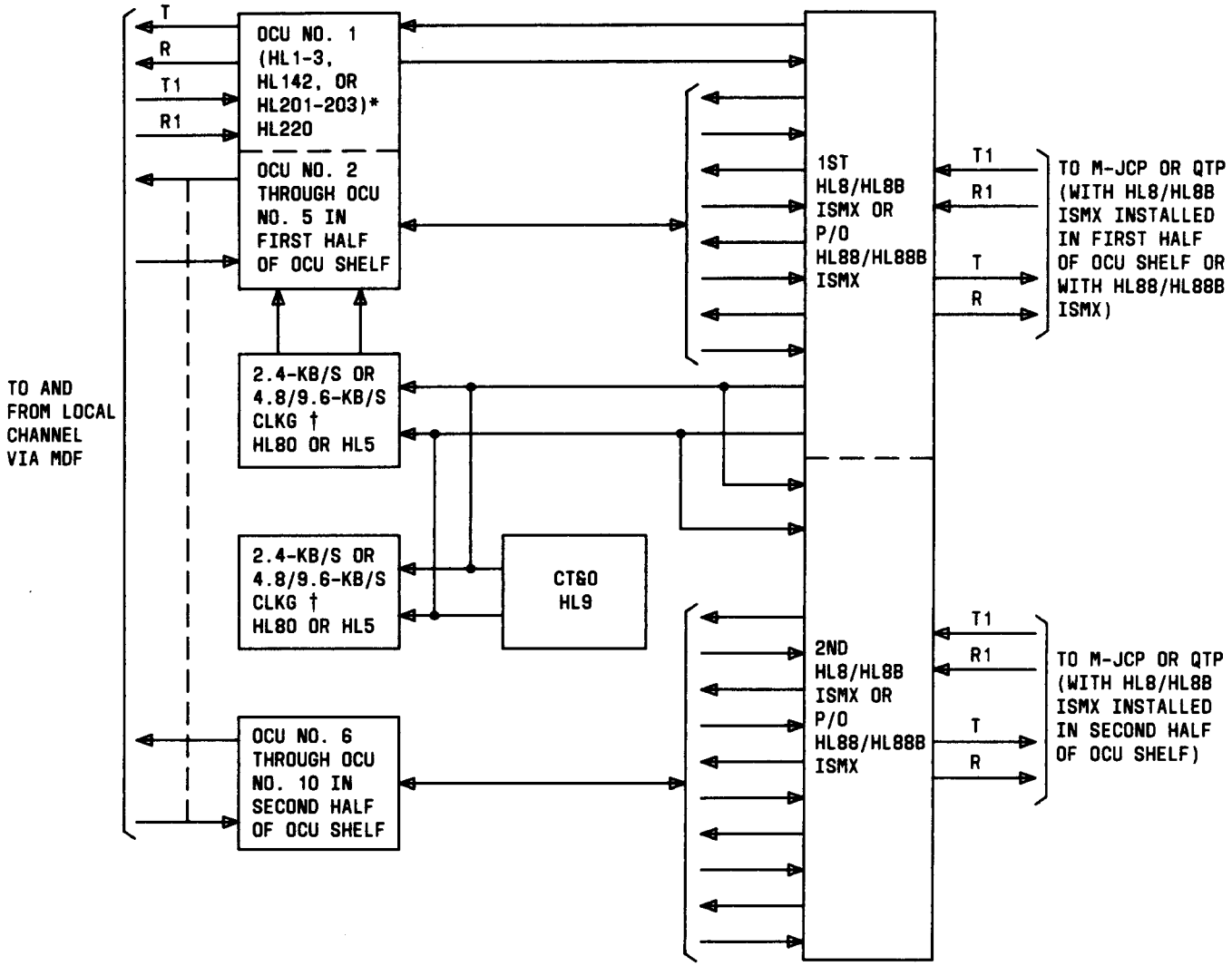



**Fig. 12—7 Foot and 11 1/2 Foot OCU Bay Arrangement**




NOTES:
1. DSX-0A AT HUB OFFICES; M-JCP OR QTP AT INTERMEDIATE AND END OFFICES WHEN OCU CHANNELS ARE NOT CONNECTED TO SRDM; SM-JCP AT INTERMEDIATE AND END OFFICES WHEN OCU CHANNELS ARE CONNECTED TO SRDM.
2. BCPA AT HUB OFFICES EQUIPPED WITH T1WB4; BCPA AT INTERMEDIATE AND END OFFICES EQUIPPED WITH T1WB4 OR T1WB5; LOCAL TIMING SUPPLY AT INTERMEDIATE AND END OFFICES NOT EQUIPPED WITH T1WB4 OR T1WB5.
3. IF ALL THE OCU IN A PARTICULAR HALF SHELF ARE HL201, 202, OR 203, THE CLKG IS NOT REQUIRED AND THESE LEADS ARE NOT USED.

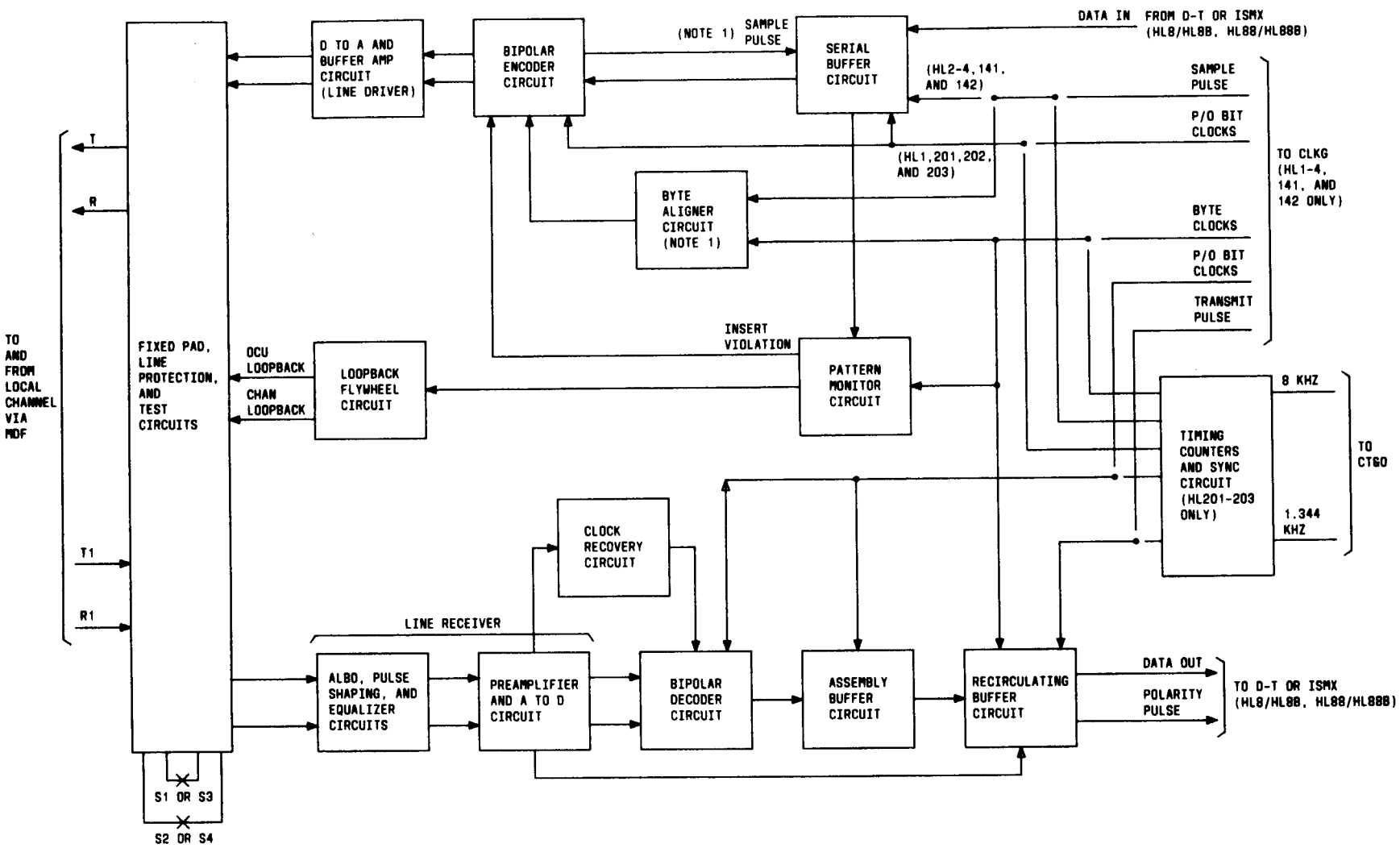
**Fig. 13—Block Diagram of OCU Channel Equipped with D-T**




* THE HL3 AND HL203 OCU CANNOT BE USED WHEN THE HL88 ISMX IS PROVIDED SINCE THIS ISMX CAN ONLY ACCEPT 2.4-OR 4.8-KB/S SUBRATE SIGNALS

† THIS CP IS NOT REQUIRED WHEN ALL THE OCU IN A PARTICULAR HALF SHELF ARE HL201, 202, OR 203.

Fig. 14—Block Diagram of OCU Shelf Equipped with HL8/HL8B or HL88/HL88B ISMX




NOTE:
1. This circuit is provided in OCUs HL1, 201, 202, and 203 only.

**Fig. 15—Block Diagram of OCU HL1-4, 141, 142, 201, 202, 203**

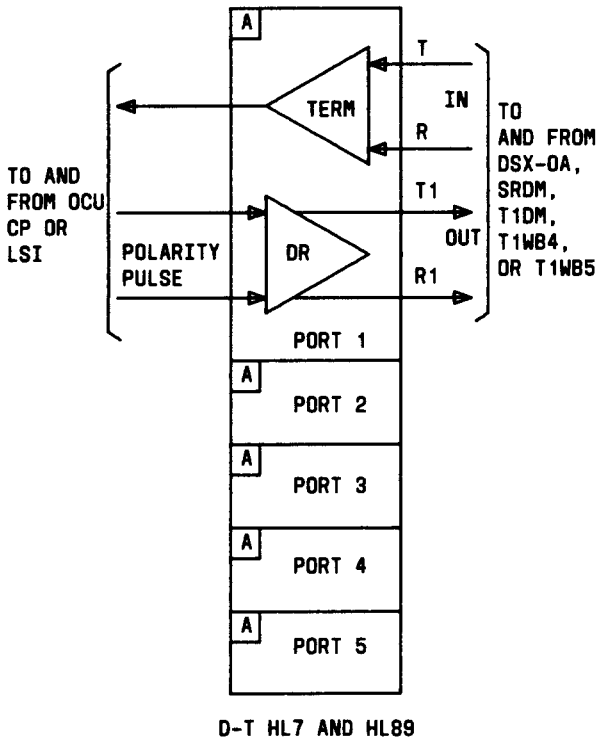



Fig. 16—Block Diagram of D-T

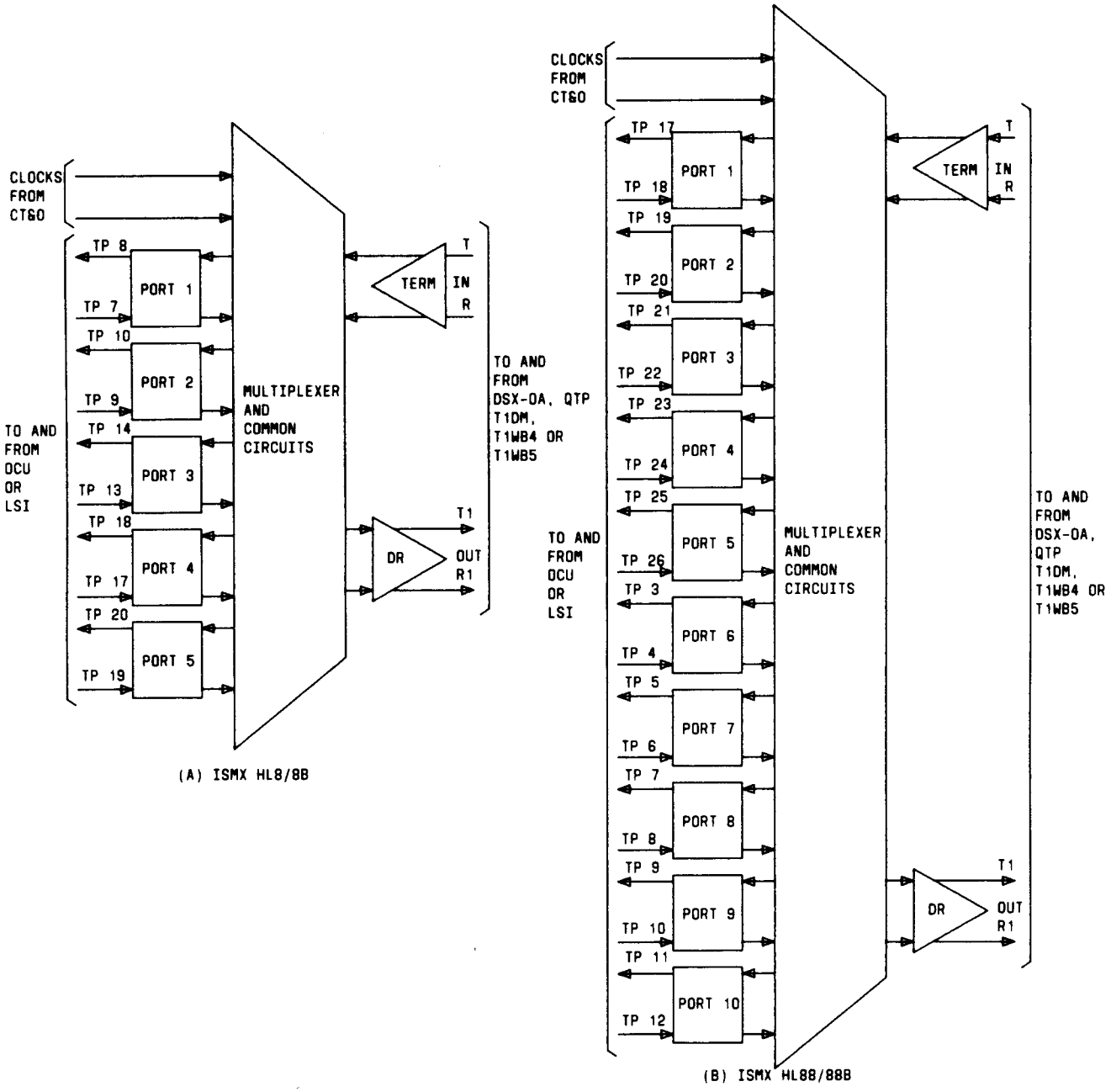



**Fig. 17—Block Diagram of ISMX HL8/HL8B and HL88/HL88B**

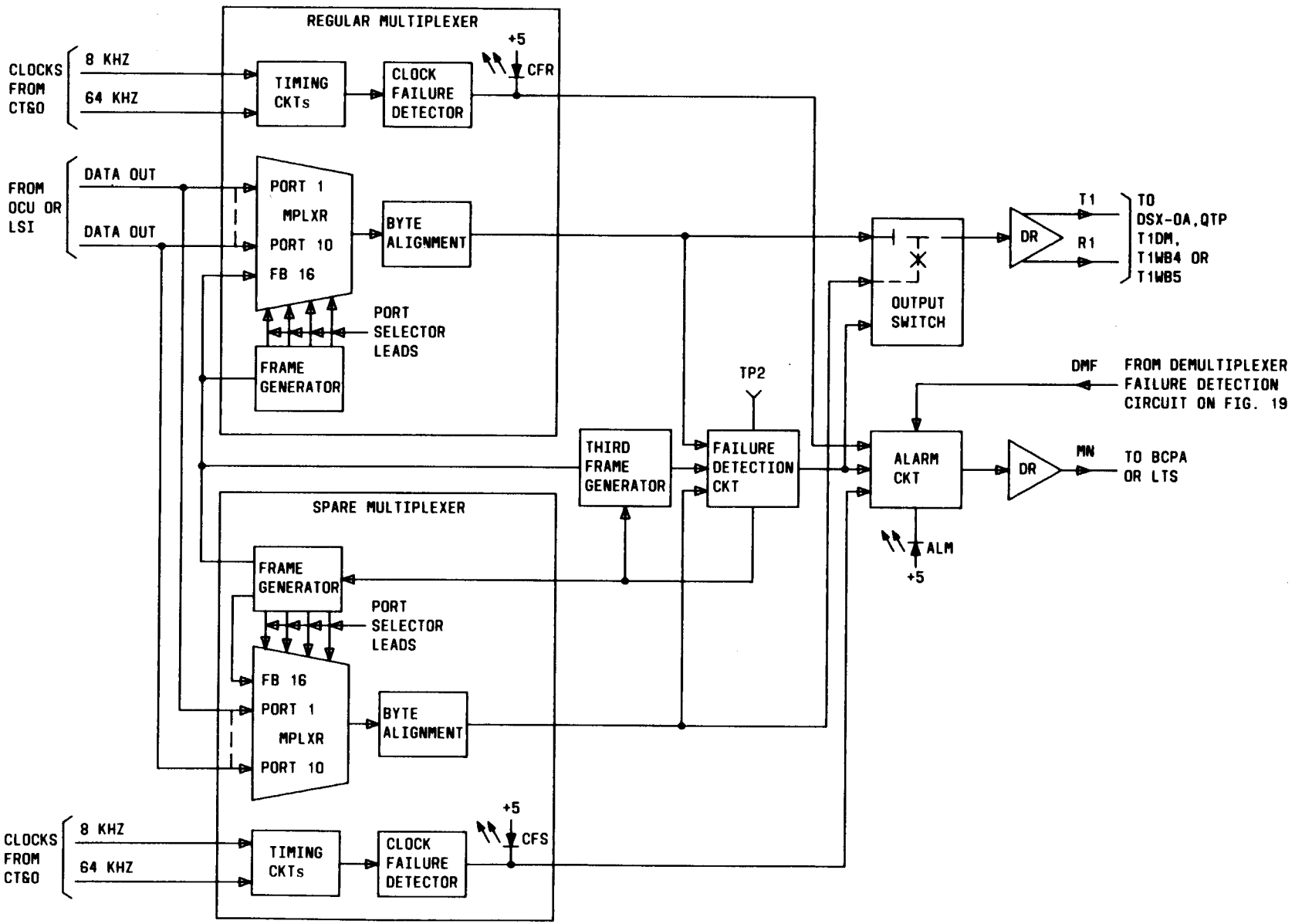



**Fig. 18—Block Diagram of HL88/HL88B ISMX Multiplexer and Failure Detection Circuit**

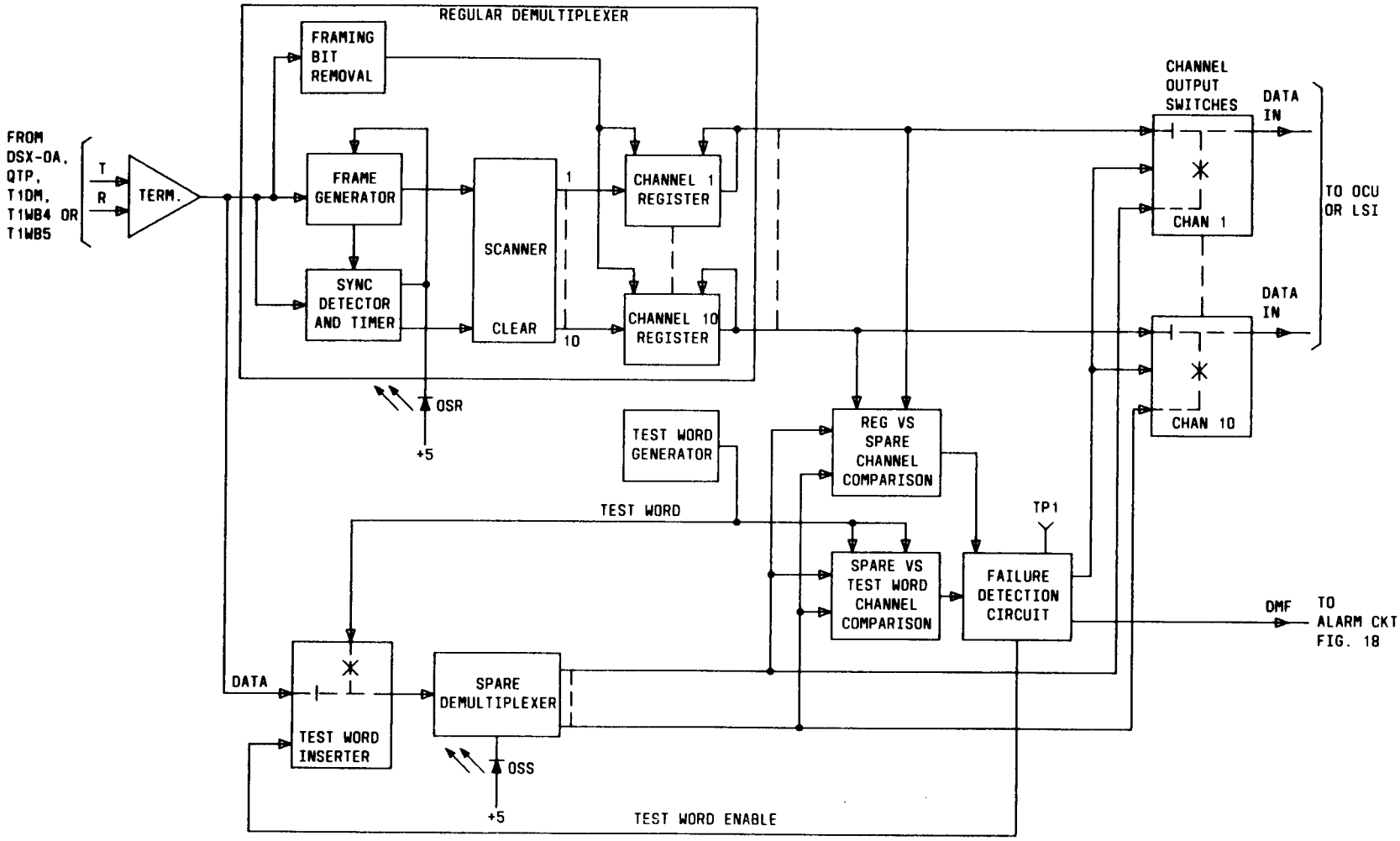



**Fig. 19—Block Diagram of HL88/HL88B ISMX Demultiplexer and Failure Detection Circuit**

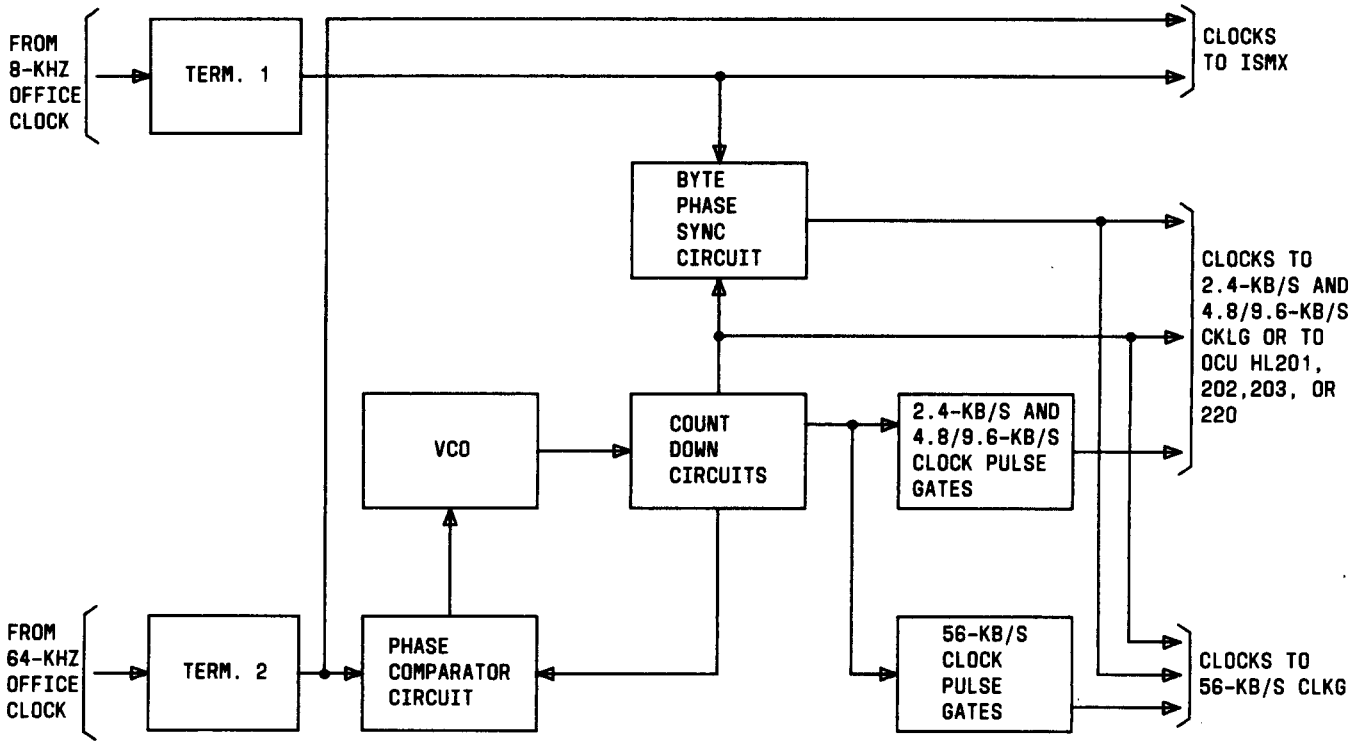



Fig. 20—Block Diagram of CT&O

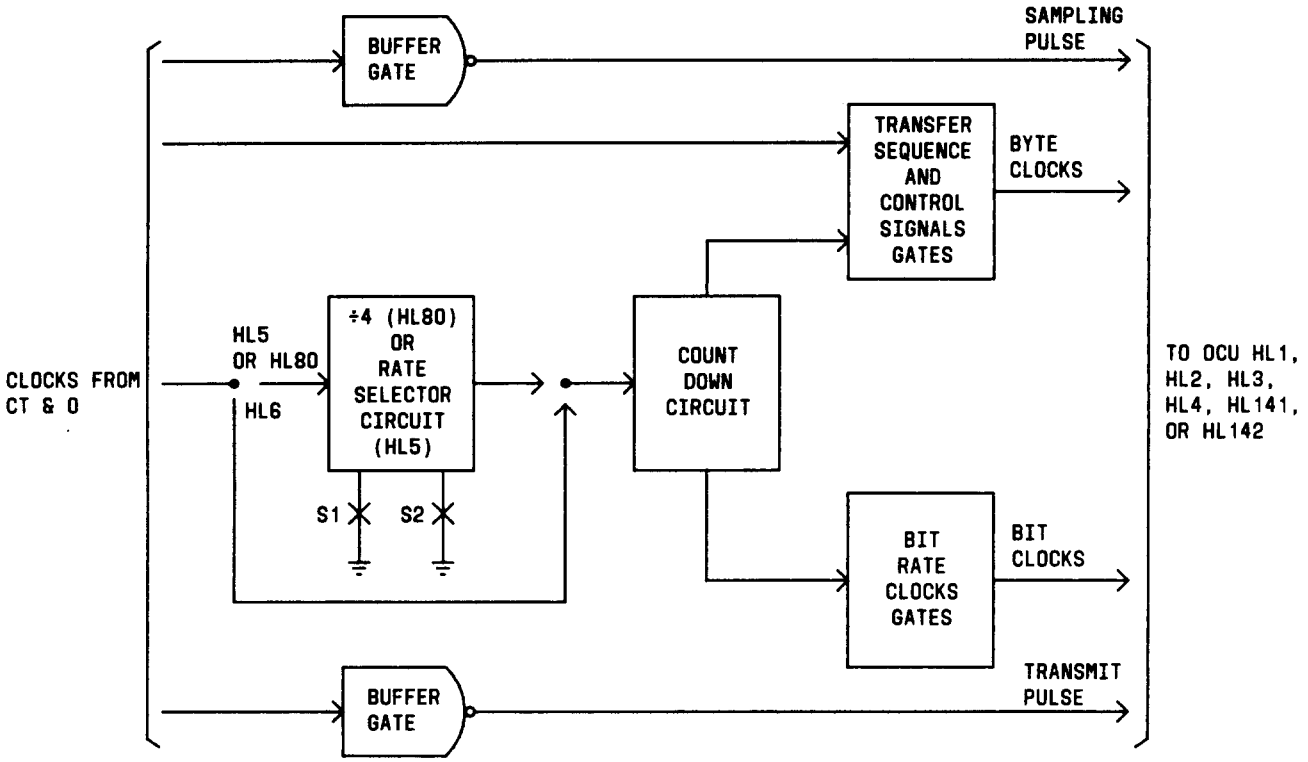



**Fig. 21—Block Diagram of CLKG**

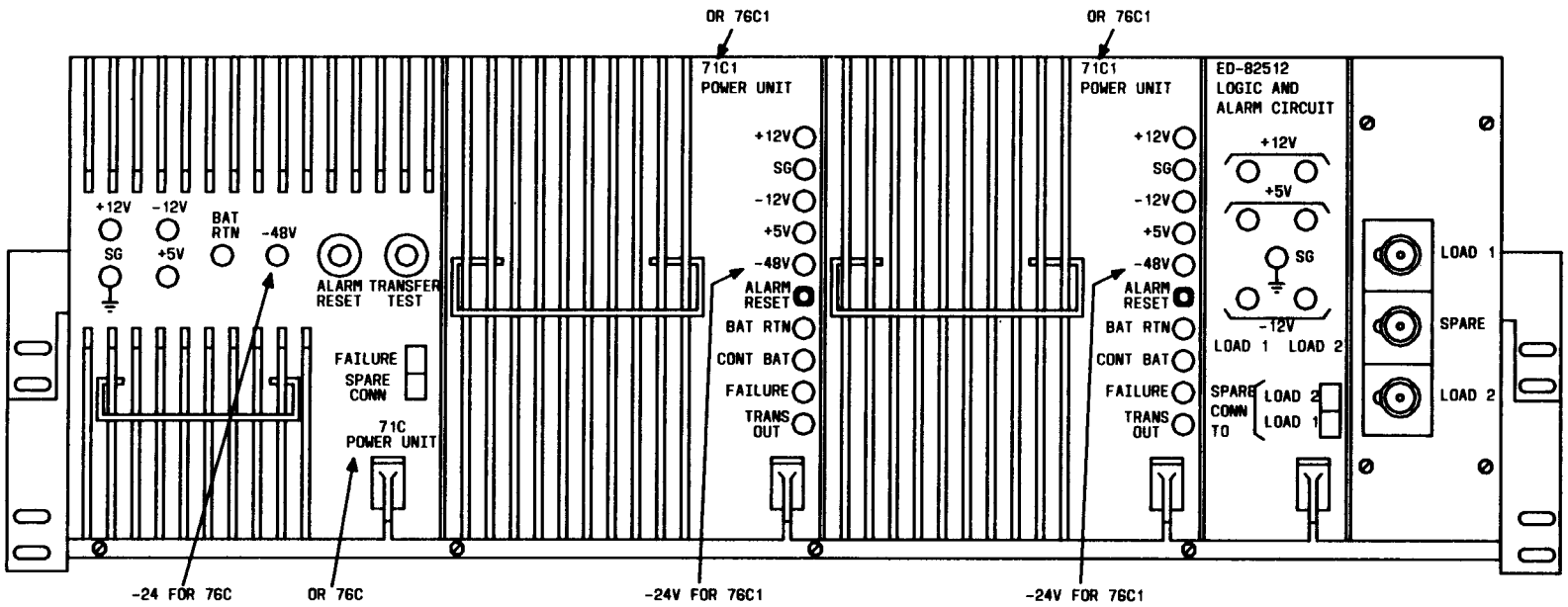



**Fig. 22—Power Supply Shelf of a 3-Shelf OCU Assembly Containing Two 71C1 or 76C1 and One 71C or 76C Power Units**