SUBRATE DATA MULTIPLEXER
DESCRIPTION
DIGITAL DATA SYSTEM

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1. GENERAL

1.01 This practice describes the SRDM (subrate data multiplexer) used for first stage multiplexing in the DDS (Digital Data System).

1.02 This practice is reissued for the following reasons:

(a) To add new terms throughout the practice

(b) To add circuit pack HL37B to replace HL37 (Mfg Disc). Circuit pack HL37B is to be used with the DDS secondary channel service. The HL37B may be used in place of the HL37 with normal DDS service (without secondary channel capability), regardless of the condition of the SRDM-PM (performance monitor).

Revision arrows are used to indicate the more significant changes.

1.03 The SRDM is used in DDS hub offices and in some local offices. In addition to SRDM shelves, each SRDM bay contains an SPM (subrate performance monitor) shelf, including an SPM and an adaptive spare SRDM. In local offices with relatively few circuits, a 5- or 10-channel ISMX (integral subrate multiplexer) mounted in an OCU (office channel unit) shelf should be used instead of an SRDM. The 5-channel ISMX can multiplex a maximum of any five subrate DS-0A (Digital Signal-Zero Level- A Signal) channels onto one DS-0B (Digital Signal-Zero Level - B Signal) channel. Although it will accept any subrate data stream (2.4, 4.8, or 9.6 kb/s), all five channels must operate at the same rate. It does not have a performance monitor or a spare. The 10-channel ISMX can multiplex ten 2.4- or 4.8-kb/s (or five of each) DS-0A channels onto one DS-0B channel, but the rates can be mixed. It is protected by internal duplication and by alarms. The 5- and 10-channel ISMXs are described in Practice 314-910-100.

1.04 The SRDM is used to perform the required multiplexing and demultiplexing functions for the transmission of signals from five 9.6-kb/s, ten 4.8-kb/s, or twenty 2.4-kb/s synchronous data channels over one 64-kb/s (DS-0) bit stream. The data streams on both the multiplexed and the nonmultiplexed sides of the SRDM are at the 64-kb/s rate, divided into 8-bit bytes that are repeated at an 8-kHz rate. The data from each subrate channel is converted to a byte-stuffed 64-kb/s format before it arrives at the SRDM.

1.05 The SRDM is byte oriented. Multiplexing is accomplished by sequentially scanning the subrate channels (ports), collecting one byte from each, and transmitting them in sequence at the 64-kb/s rate to a second stage multiplexer. The SRDM can be arranged to operate at any one of the three subrates (2.4, 4.8, or 9.6 kb/s). In the 64-kb/s stuffed format, each 9.6-kb/s subrate channel repeats each data byte five times; therefore, single bytes from five channels can be multiplexed with no loss of information (9.6-kb/s SRDM operation).

1.06 A sequential scan of all channels is also required for demultiplexing the 64-kb/s data stream received from the second stage multiplexer. The framing bits inserted into the bytes by the SRDM at the far-end allow the demultiplexer to identify the byte of each channel. With 9.6-kb/s SRDM operation, the multiplexed data stream contains data bytes for five channels in sequence. The data for each channel is delivered to the proper port, where each byte is repeated five times at the 8-kHz rate. The 64-kb/s stuffed format is thus restored in each subrate channel.

1.07 Each data byte in the stuffed format of a 4.8-kb/s subrate channel is repeated ten times, permitting single bytes from ten channels to be multiplexed with no information loss (4.8-kb/s SRDM operation). In the demultiplexing direction, the 64-kb/s data stream carrying data for ten 4.8-kb/s channels in sequence is demultiplexed to deliver the data for each channel to the proper one of ten ports. Each data byte is then repeated ten times to restore the 64-kb/s stuffed format to each channel.

1.08 Similarly, each data byte in the stuffed format of a 2.4-kb/s subrate channel is repeated 20 times, and single bytes from 20 channels are multiplexed in sequence for 2.4-kb/s SRDM operation. In the demultiplexing direction, the data stream carrying data for twenty 2.4-kb/s channels is demultiplexed to deliver the data for each channel to the proper one of 20 ports. Each byte is then repeated 20 times to restore the 64-kb/s stuffed format.

1.09 All input and output data streams on both the multiplexed and nonmultiplexed sides of the SRDM are aligned in time. The bits are aligned by the 64-kHz office timing supply; the bytes, by the 8-kHz office timing supply.

2. FUNCTIONAL DESCRIPTION

2.01 Figure 1 is a block diagram of an SRDM as used with an associated SPM and spare

SRDM. The normal signal path is indicated by heavy lines. The data is processed in the SP (subrate port) circuits and in the common logic (C) circuit. The operation of the SRDM is monitored by the SPM via the TA (test access) circuit. If a failure occurs in a single SRDM, all data channels served by that SRDM are switched to the spare SRDM. The switch is accomplished by the PS (port switch) and CMS (common switch) circuits, and service is transferred via the port bus and common bus leads.

A. Subrate Port Circuits (HL36B)

2.02 Figure 2 is a functional diagram of the SP circuits. The circuits required to combine the data from five subrate channels are contained in one subrate port CP (circuit pack). The same subrate port is used for any of the three subrates (2.4, 4.8, or 9.6 kb/s). The number of channels accommodated by an SRDM and the data rates allowable on each channel are limited by the operating rate of the SRDM. When an SRDM is arranged for 9.6-kb/s operation, one SP serves a maximum of five subrate channels. Any one of the five channels may be used for 9.6-, 4.8-, or 2.4-kb/s service. When a 9.6-kb/s channel is assigned to 4.8-kb/s service, each data byte entering the SP has been repeated ten times. The 9.6-kb/s SRDM multiplexes every fifth byte, placing two identical samples of each new data byte on the multiplexed line. In the demultiplexing direction, each of the duplicate bytes delivered to the SP is repeated five times, producing a series of ten identical bytes for each new data byte. The correct stuffed format for 4.8-kb/s service is thus restored. Similarly, when a 9.6-kb/s channel is assigned to 2.4-kb/s service, each data byte entering the SP has been repeated 20 times. Multiplexing every fifth byte places four identical samples of each new data byte on the multiplexed line. In the demultiplexing direction, each of the four identical bytes delivered to the SP is repeated five times, producing a series of 20 identical bytes for each new data byte and restoring the correct stuffed format for 2.4-kb/s service.

2.03 When an SRDM is arranged for 4.8-kb/s operation, a maximum of ten channels may be accommodated with two SPs. Channel usage is limited to 4.8- or 2.4-kb/s service. With 4.8-kb/s SRDM operation, every tenth byte in each subrate channel is multiplexed. These channels cannot be used for 9.6-kb/s service because every fifth byte in the 9.6-kb/s stuffed format is a new data byte and only one-half of the data bytes would reach the multiplexed line. When a 4.8-kb/s channel is assigned to 2.4-kb/s service, two samples of each new data byte are multiplexed. In the demultiplexing direction, each of the duplicate bytes delivered to the SP is repeated ten times, producing a series of 20 identical bytes for each new data byte and restoring the correct stuffed format for 2.4-kb/s service.

2.04 When an SRDM is arranged for 2.4-kb/s operation, a maximum of 20 subrate channels can be accommodated with four SPs. Channel usage is limited to 2.4-kb/s service. With 2.4-kb/s SRDM operation, only one of every 20 bytes in each subrate channel is multiplexed; therefore, only one-fourth of the data bytes from 9.6-kb/s service or one-half of the data bytes from 4.8-kb/s service would reach the multiplexed line.

2.05 The data received from an OCU or from a port of another SRDM appears, via a bridged connection, at the PS circuit and at the line receiver in one of the five port circuits contained in the SP. The port multiplexer combines the outputs of the five line receivers. Under control of the address register, the data from all five ports is transmitted to the C circuit over lead $\overline{\text{RD}}$ where it is multiplexed with data from other port boards when the SRDM speed is 2.4 or 4.8 kb/s.

2.06 In the other direction of transmission, the multiplexed data from the C circuit is received over the PXD lead for distribution to the five data ports. Under control of the address register, the data for each port is sent to the proper recirculating register one byte at a time. The byte contained in each recirculating register is sent to its associated line driver and is repeated at the 8-kHz clock rate until a new byte is received. Thus, each line driver transmits a stuffed 64-kb/s data stream.

2.07 The address register receives addresses over lead PG at exact times determined by lead $\overline{\text{PRC}}$. The address in the register causes the data from each line receiver to be multiplexed by the port multiplexer and allows the distribution of received data to the correct port as each byte appears on the PXD lead.

2.08 The test signal multiplexer samples the signals at the input to each line driver and at the output of each line receiver. Under control of the SPM and the test access circuit, the test signal multiplexer places on the PB lead signals from the five line

drivers and five line receivers in a sequential fashion. The state of the five ST leads determines which one of the five port signals is appearing on the PB lead. The state of the FP and $\overline{FP}$ leads determines whether the signal on the PB lead will be from the line driver or the line receiver of the chosen port. The SPM uses the signals applied to the PB lead in determining the working condition of the SRDM.

2.09 When the SPM detects a failure in an SRDM port circuit, the failure is indicated by a ground on the $\overline{PL}$ lead, causing illumination of the fault LED (light-emitting diode) on the faceplate of the SP.

B. Common Logic Circuit ▶(HL37/HL37B)◀

2.10 The C circuit, shown in Fig. 3, multiplexes the signals from the port circuits for transmission to a T1 data multiplexer (T1DM), T1WB4 data-voice multiplexer, or T1WB5 data-voice multiplexer. It also demultiplexes the signal received from the second stage multiplexer (T1DM, T1WB4, or T1WB5).

2.11 The signals from the port circuits are received at the common logic multiplexer over the $\overline{RD}$ leads. The number of active $\overline{RD}$ leads is determined by the number of SPs used in the SRDM. The contents of one or more of these leads are multiplexed together, a framing pattern is added, and the multiplexed signal is sent to the 8-bit delay register for alignment with the 8- and 64-kHz clocks. The signal is then sent to the line driver and transmitted, via the CMS circuit, to the second stage multiplexer.

2.12 In the other direction of transmission, the multiplexed signal from the second stage multiplexer is received at the line terminator, sent to the 1-bit data register for clock alignment, and then transmitted to the port circuits over the PXD lead.

2.13 A sample of the multiplexed line signal is taken at the line driver and sent to the SPM over the LMT lead. Similarly, a sample of the line signal to be demultiplexed is taken at the line terminator and sent to the SPM over the LDT lead.

2.14 A manually operated loop switch is provided to permit opening the connections to the second stage multiplexer and connecting the line-driver output to the input of the line terminator for maintenance operations.

2.15 Since the multiplexed signal is composed of data bytes from a number of different channels, a framing pattern must be added to the transmit multiplexed signal so that each channel byte can be identified and delivered to the correct port at the distant SRDM. Each byte received at the multiplexer contains a zero in bit position 1 to allow the addition of a framing pattern. ▶The new SRDM common logic circuit pack (HL37B) will place a one in the first bit position.◀ The framing pattern is a specific sequence of bits inserted into bit position 1 of each byte of the multiplexed signal. The pattern is generated in the 10-bit framing register and in the sync pattern generator according to the speed of operation for which the SRDM is arranged. For 2.4-kb/s operation, a maximum of 20 ports may be assigned; therefore, the framing pattern contains 20 bits arranged in the sequence 01100101001110000100. For 4.8-kb/s operation, a maximum of ten ports may be assigned and the framing pattern contains ten bits. The first ten bits of the 2.4-kb/s framing pattern are used. Thus, the pattern is 0110010100. Similarly, for 9.6-kb/s operation, only five ports are available, the first five bits of the 2.4-kb/s framing pattern are used, and the pattern is 01100. The first bit of the framing pattern is inserted into the multiplexed stream as bit number 1 in the byte corresponding to port 1, so that the succeeding framing bits are aligned with the succeeding bytes in correct sequence as the ports are multiplexed.

2.16 The 10-bit framing register and the sync pattern generator also produce the framing sequence for the receiving direction. The receiving sequence is identical to, but independent of, the transmitting sequence. The resync circuit compares the framing sequence contained in the signal received from the second stage multiplexer with the receiving sequence produced in the 10-bit framing register. If they match, the SRDM is in sync. If not, the sync pattern generator matches its timing to the incoming framing pattern to bring the SRDM into sync. The framing pulses are sent to the port group decoder that generates address information for the port circuits. Transmitting and receiving addresses are time-shared and delivered to the correct port circuit over the four PG leads.

2.17 The clock buffers furnish 64-kHz clock pulses to the four PCLK leads for use in the port circuits. The pulse doubler furnishes the pulses required for time sharing in the 10-bit framing register and in

the address registers in the port circuits (via the four $\overline{PRC}$ leads).

2.18 The display logic responds to information received from the SPM. A 7-element alphanumeric LED on the faceplate of the C circuit pack provides visible indications of the operating condition of the SRDM. The alphanumeric characters and their meanings are listed in Table A. If a failure is detected in the SRDM, the appropriate character is formed on the LED display. If the failure is in a port circuit, the failure LED on the faceplate of the SP containing the affected port circuit is also lighted. The spare SRDM, if idle, is set for a matching data speed and the service is switched to the spare. When the switch is completed, the 7-element LED display on the failed SRDM flashes at about half-second intervals. When the SRDM is again operational, the LED display changes to a flashing "H" but the SRDM is not restored to service until the SPARE RELEASE switch on the SPM is manually operated.

2.19 An office minor alarm is initiated whenever a working SRDM is switched to the spare. If a failure is detected in a second SRDM while the spare is in use, a major alarm is operated and the appropriate character displayed on the common logic circuit of the second SRDM, but the display does not flash.

2.20 The faceplate of the C circuit pack contains a manually operated, 2-position MODE switch (not shown in Fig. 3). The function of the MODE switch is to prevent switching a particular SRDM to the spare SRDM and to prevent office alarms if a fault is detected in that SRDM. By operating the MODE switch to the NO ALM position, maintenance can be performed on a specific SRDM without affecting the switching and alarm protection for other SRDMs in the bay. When this switch is in the NO ALM position, a steady "H" is displayed on the common logic LED. If the SPM detects a failure, the display is changed to the appropriate character, but no alarm is generated and no switch occurs.

2.21 ***SRDM Secondary Channel (HL37B):*** In the DDS Network a minimum "ones" density is required to maintain T1 repeatered line synchronization. The SRDM, in some instances, may be connected to a dataport where the "ones" density was assured by the eighth bit, the control bit, being one in the data mode. Since in the secondary channel mode, the eighth bit is shared with the secondary channel bit, which may be zero, another approach to maintaining the "ones" density was needed.

2.22 A function of the HL37 common logic circuit pack was to strip the network framing pattern (found in bit 1 of each byte) from the data stream (network-to-loop direction) and replace it with a zero. A modification to the HL37 changes that function to provide a one in the first bit position. Thus, in the network-to-loop direction of transmission, there will always be a one in the first bit position when using the HL37B, the modified code. This satisfies the T1 ones-density requirement when the channel is subsequently applied to a DS-0 to DS-1 MUX. Thus, the HL37B is needed for secondary channel capability only if the drop side of the SRDM is not connected to an OCU or a tandem subrate multiplexer. The spare HL37 must be changed to an HL37B when any one of the HL37s is changed.

2.23 In the loop-to-network direction of transmission, the ones-density can be satisfied only by limiting secondary channel capability to those SRDM channels which have a one in the subrate framing pattern. The following channels are used:

- 2.4-kb/s channels 2, 3, 6, 8, 11, 12, 13, and 18
- 4.8-kb/s channels 2, 3, 6, and 8
- 9.6-kb/s channels 2 and 3.

An abnormal condition occurs with the HL37B circuit pack in the SRDM bay. In the network-to-loop direction of transmission, complete loss of input signal to the SRDM (line open) will cause the visual display on the HL37B circuit pack to indicate "no incoming framing" rather than "no incoming signal." This is caused by the forced one in bit 1 position being detected by the performance monitor. Since either indication still signifies an incoming trouble, the performance monitor is not modified to correct for the condition in an effort to keep the costs of implementing the secondary channel to a minimum. The HL37B may be used in place of HL37 with normal DDS service.

C. Test Access Circuit (HL38)

2.24 The TA circuit, shown in Fig. 4, provides the means for SPM testing of transmitting and receiving signals from a maximum of four SRDMs on

a single shelf. Address information for selecting the test signals for testing is received from the SPM over leads AI, BI, CI, DI, EI, and FI and via the C circuits over leads $\overline{SN1}$, $\overline{SN2}$, $\overline{SN3}$, and $\overline{SN4}$. The selected test signals from individual port circuits are sent to the SPM over leads CPTSA and CPTSB and from the multiplexed line over leads CLTSA and CLTSB.

2.25 The 5-line decoder selects an individual port circuit in each SP over the five ST leads. The selection of the transmit or receive signals from each port is made over leads FP and $\overline{FP}$. The multiplexed test signals from a maximum of eight SPs are received at the port multiplexer over the PB leads. These signals are multiplexed according to address information from the 4-line decoder to select a maximum of four SPs in each SRDM and according to enabling signals from the $\overline{SN}$ leads to select a maximum of four SRDMs in sequence.

2.26 The line multiplexer receives line test signals from a maximum of four SRDMs over the LDT and LMT leads. The signals are multiplexed together using enabling signals from the $\overline{SN}$ leads to select the individual SRDMs in sequence.

D. Common Switch Circuit (HL39)

2.27 The CMS circuit contains four relays, each used to transfer the leads of the multiplexed side of one SRDM to the adaptive spare. The R-C (resistor-capacitor) networks are provided to terminate the receive multiplexed line. Contacts are provided to operate the port switch relays via leads that pass through the C circuit and to inform the SPM whenever any of the relays are operated. One CMS circuit may serve a maximum of four SRDMs; no more than one, however, is switched at any one time. The connections for one SRDM between the CMS circuit and the adaptive spare SRDM are included in Fig. 5.

2.28 The common switch relays are operated individually under control of the SPM. The received signal remains connected to the faulty SRDM, and the spare is added on a bridged connection when the relay is operated. Even though service is transferred to the spare, the data signal is still supplied to the faulty SRDM for use in SPM testing and for efficient restoration when a trouble condition is corrected. Relay operation opens the transmitting side of the switched SRDM so that the output of only the spare SRDM is supplied to the second stage multiplexer.

E. Port Switch Circuit (HL35)

2.29 The PS circuit transfers the service on ten subrate channels to the spare SRDM. Figure 5 shows the connections for switching one channel. The PS circuit contains four relays which are operated in pairs. Each pair of relays transfers the service from the five ports of one SP. One 2.4-kb/s SRDM requires two complete PS circuits, whereas each 4.8-kb/s SRDM requires one-half of two PS circuits. One PS circuit may serve two 9.6-kb/s SRDMs, each using one-half of the CP. The PS circuit also provides R-C terminating networks for the receive port pairs.

2.30 Operation of the common switch relay associated with an SRDM results in operation of the port switch relays required to transfer all ports of the same SRDM. The receiving side of each port remains connected, and bridged connections are established to the spare when the SRDM is switched. Even though all service is transferred to the spare, the data signal is still supplied to all ports of the faulty SRDM for use in SPM testing and for efficient restoration when a trouble condition is corrected. Relay operation opens the transmitting side of all ports in the affected SRDM so that the output of only the spare SRDM is supplied to the subrate channels.

3. EQUIPMENT ARRANGEMENTS

A. Circuit Packs

3.01 The circuits required in the SRDM, as described in Part 2, are mounted on five varieties of plug-in CPs. The faceplate of each CP is marked with the apparatus code and with an abbreviation of the circuit title, as indicated in Table B.

3.02 Identical CPs are used for any SRDM regardless of the subrate data speed or the number of customers served. Flexibility is achieved by variation in the number of certain CPs used, by their positioning in the SRDM shelf, and by interconnections contained in the universal shelf wiring.

B. Shelf Arrangements

3.03 The SRDM shelves are manufactured with two identical shelves adjoined one above the other. A front view of the 2-shelf subrate data assembly (J70177AM) is shown in Fig. 6; a rear view, in Fig. 7. The 2-shelf unit is 23 inches wide, 12 inches deep,

and 18-1/2 inches high. Each SRDM shelf is 23 inches wide, 12 inches deep, and 8 inches high. Two additional inches of height are required for a fuse and connector panel serving the 2-shelf unit, and one-half inch of height is required for an upper shelf cover. The 2-shelf unit weighs 39 pounds empty and 73 pounds fully equipped. The unit is divided into quadrants identified as shelf A (lower), group 1 (left) and group 2 (right); and shelf B, groups 1 and 2. Figure 6 shows shelf B, group 2, equipped with CPs for one SRDM operating at 2.4 kb/s, with 20 ports available.

3.04 Each shelf contains CP connectors, guide slots to position the CPs on the shelf, and universal wiring. The face of each shelf is marked to indicate the correct positions for the various CPs. Each position is marked with the same circuit title abbreviation that appears on the faceplate of the type of CP to be inserted and with a shelf position number corresponding to the location of the CP connector. Figure 8 shows the association between CPs and shelf positions.

3.05 Each shelf uses one TA HL38 CP and one CMS HL39 CP to serve a maximum of four SRDMs on the shelf. The shelf positions used for other varieties of CPs are divided into two groups, each to be equipped independently. The connected dots in Fig. 8 indicate the association of shelf positions and circuit packs for the various possible arrangements in each shelf group. The PS position 1 is interconnected with SP positions 1 and 3; therefore, an HL35 CP must be furnished in PS position 1 any time a subrate port circuit, HL36B CP, is used in either SP position 1 or 3, or both. Similarly, PS position 2 is associated with SP positions 2 and 4. The C position 11 (or 21) is associated with SP positions 1 and 2, and C position 12 (or 22) is associated with SP positions 1, 2, 3, and 4.

3.06 Table C gives additional information for equipping shelf groups. Each SRDM requires one ◗HL37 or HL37B CP◖. Insertion of an HL37 CP into C position 10 or 20 limits the shelf group to one SRDM and sets the SRDM speed at 2.4 kb/s. In this position, the ◗HL37 or HL37B CP◖ is associated with all four SP positions; however, the HL36B CP and associated HL35 CPs may be supplied only as needed for the number of ports being activated. A 2.4 SRDM fully equipped for 20 ports uses C position 10 or 20; SP positions 1, 2, 3, and 4; and PS positions 1 and 2.

3.07 When C position 10 or 20 is not used, C positions 11 and 12, or 21 and 22, respectively, may both be used, permitting the shelf group to be equipped with two SRDMs. An ◗HL37 or HL37B◖ CP in C position 11 or 2l is associated with SP positions 1 and 2. In this arrangement, the SRDM speed is determined by the status of SP position 2. If this position is unequipped, the SRDM operates at 9.6 kb/s. If an HL36B CP is inserted into this position, the SRDM speed is 4.8 kb/s. The same relationship exists between C position 12 or 22 and SP positions 3 and 4. The SRDM speed is 9.6 kb/s when SP position 4 is blank and 4.8 kb/s when SP position 4 is equipped.

3.08 ***Caution: Insertion of an HL36B CP into SP position 2 or 4 of a 9.6 SRDM will change the SRDM rate to 4.8 kb/s. Similarly, removal of the HL36B CP from SP position 2 or 4 of a 4.8 SRDM will change the SRDM rate to 9.6 kb/s. With working SRDMs, either of these actions results in service interruption of all channels and causes a switch and probable major alarm at both ends of the DS-0 channel. Even when an SRDM is out of service, the switch and probable major alarm occur at the distant end of the DS-0 channel. Careful attention to the maintenance procedures given in Practice 314-911-502 is essential.*** The SP position 2 or 4 is never used with a 9.6 SRDM. A 4.8 SRDM may be partially equipped for five ports by leaving SP position 1 or 3 blank, but SP position 2 or 4 must be equipped to establish the SRDM speed. Thus, a partially equipped 4.8 SRDM has ports 6 through 10 available for service.

3.09 A shelf group equipped for two 9.6 SRDMs uses C positions 11 and 12 or 21 and 22; SP positions 1 and 3; and PS position 1. A shelf group equipped for two fully equipped 4.8 SRDMs uses C positions 11 and 12 or 21 and 22; SP positions 1, 2, 3, and 4; and PS positions 1 and 2. A shelf group may also be equipped for one 4.8 and one 9.6 SRDM, but this arrangement does not result in efficient use of HL35 CPs.

3.10 For record purposes, the location of any SRDM is designated by an equipment address, as shown in Fig. 9. The half- or quarter-shelf location is specified in the partial-shelf portion of the address according to the following:

10—2.4-kb/s SRDM in the left half-shelf

11—4.8- or 9.6-kb/s SRDM in the first (left) quarter-shelf

12—4.8- or 9.6-kb/s SRDM in the second quarter-shelf

20—2.4-kb/s SRDM in the right half-shelf

21—4.8- or 9.6-kb/s SRDM in the third quarter-shelf

22—4.8- or 9.6-kb/s SRDM in the fourth (right) quarter-shelf.

For example, a circuit layout record card showing a 9.6-kb/s SRDM at equipment address 0102.8.3.11 indicates a location at floor 01, aisle 02, bay 8, shelf 3, first (left) quarter-shelf.

3.11 A 3-shelf SRDM and SPM assembly (J70177AL) is provided in each bay. The 3-shelf unit is 23 inches wide, 12 inches deep, and 27 inches high. The unit weighs 57 pounds empty and 105 pounds fully equipped. The SPM and spare SRDM are accommodated by a shelf located above two standard SRDM shelves.

3.12 The 2-inch high fuse and connector panel located above the B shelf in the 2-shelf SRDM assembly and in the 3-shelf SRDM and SPM assembly contains separate fuses to accommodate each SRDM, the SPM, and the spare SRDM.

3.13 The rear of each 2-shelf SRDM assembly and 3-shelf SRDM and SPM assembly contains connectors (see Fig. 7) to accommodate power and ground wires; wires to the T-Carrier Administration System; a timing cable; two cables for the protection bus; and, in the 2-shelf unit, a performance monitor cable. In addition, each SRDM shelf is equipped with four 50-pin connectors and with one 24-pin connector. The association between these connectors and the CPs used in each shelf group is shown in Fig. 8. The 50-pin connectors provide the means for attaching external cabling to connect the nonmultiplexed side of a maximum of four SRDMs to the DSX-0 (digital signal cross-connect zero level) bay in a hub office or to the SM-JCP (subrate data multiplexer jack and connector panel) in an end or intermediate office. The 24-pin (center) connector is used to connect the multiplexed side of a maximum of four SRDMs on the shelf to the DSX-0 bay in a hub office or to the M-JCP (multiplexer jack and connector panel) in an end or intermediate office. The DSX-0 is described in Practice 314-914-100. The M-JCP and the SM-JCP are described in Practice 314-970-100.

C. Bay Arrangements

3.14 The SRDM and SPM shelves are mounted in 23-inch, unequal flange, duct-type bays with heights of 11 feet 6 inches or 7 feet. The 11-foot 6-inch bay accommodates a maximum of 40 SRDMs. Two 7-foot bay arrangements are available:the initial bay which accommodates a maximum of 16 SRDMs and the expansion bay which accommodates a maximum of 32 SRDMs and contains no other equipment. Each 11-foot 6-inch bay and each 7-foot initial bay contain an SPM and an adaptive spare SRDM shelf (described in Practice 314-983-110); a 5V PSS 5-volt power supply shelf (described in Practice 314-970-101); and a BCPA (bay clock, power, and alarm) shelf (described in Practice 314-916-100). This equipment in the 7-foot initial bay also serves the SRDMs in one 7-foot expansion bay if the expansion bay is provided. The bays may be ordered partially equipped; here, some of the SRDM assemblies are omitted and may be added as required. Figure 10 shows the bay arrangements for 11-foot 6-inch and 7-foot SRDM bays and for the 7-foot SRDM expansion bay.

3.15 In local offices using ISMXs in the OCU shelves, the multiplexed side of the ISMXs is cabled to an M-JCP for connection to T1DM, T1WB4, or T1WB5 ports. These offices may later be expanded to use regular SRDM and SPM equipment in SRDM bays. Here, an SM-JCP may also be provided for use between the OCUs and SRDMs. When the SRDM equipment is placed in service, each D-T (driver-terminator) CP (replacing the ISMX) in the OCU bay may be cabled to the SM-JCP instead of to the M-JCP, and the multiplexed side of the SRDM is cabled to the M-JCP.

D. 2.4-kb/s Splitting Cable

3.16 When an SRDM shelf is arranged for 2.4-kb/s service in both shelf groups, only two multiplexed 4-wire lines appear at connector J7 (see Fig. 8). In local offices, the M-JCP connectors accommodate T1DM, T1WB4, or T1WB5 ports in groups of four. To overcome this inefficiency, a splitting cable, ED-73435-22, G8, is available for use at local offices only when both SRDM shelves are arranged for 2.4-kb/s service in a 2-shelf SRDM assembly or in a 3-shelf SRDM and SPM assembly. The splitting cable is 2 feet long with a single 24-pin connector, P1, at one

end and two 24-pin connectors, J1 and J2, at the other end. The single connector, P1, plugs into any of the M-JCP connectors, J3 through J8. The four quads that connect to the four T1DM, T1WB4, or T1WB5 ports are divided between connectors J1 and J2 for cabling to connectors J7A and J7B in the SRDM shelf assembly. The SRDMs on both shelves A and B are cabled to one M-JCP connector; thus, using all four T1DM, T1WB4, or T1WB5 ports.

3.17 The 2.4-kb/s splitting cable cannot be used if any shelf group in a 2-shelf assembly is arranged for 4.8- or 9.6-kb/s service, unless the shelf group is limited to one SRDM and the ▶HL37/HL37B◀ CP occupies C position 11 or 21. Thus, for connection to an M-JCP, 2.4-kb/s service must be grouped into separate assemblies to permit use of all T1DM, T1WB4, or T1WB5 ports.

4. POWER SUPPLY

4.01 The SRDM circuitry operates from +5 volts obtained from a 5V PSS that is furnished in each 11-foot 6-inch SRDM bay or 7-foot 2-bay SRDM arrangement. The power supply shelf uses a maximum of three plug-in power units, either 71D units for operation from a standard −48 volt power source or 76D units for operation from a standard −24 volt source. Two of either type of power unit are used to supply the +5 volt power for a maximum of 48 SRDMs, the SPM and adaptive spare SRDM, and the BCPA shelf in one 11-foot 6-inch SRDM bay or in one 7-foot SRDM bay and one 7-foot SRDM expansion bay. The third power unit is a spare which may or may not be furnished.

4.02 The outputs of all three power unit positions on the shelf are multipled together; therefore, the failure of any one unit does not affect service when the spare unit is furnished and switched to the defective SRDM.

Caution: When a single-unit failure occurs in a shelf equipped with a spare unit, the output of the faulty unit will be replaced by that of the spare unit and a minor alarm will be activated. In the event that a second power unit fails, the logic and alarm circuit will activate a major alarm in the LTS (local timing supply) or BCPA shelf except in the case where the second power unit failure occurs in the spare power unit while the first power unit that has failed is removed from the shelf. It is imperative that the failed power unit be replaced with a working power unit as soon as possible to prevent interruption of customer service and erroneous alarm indications.

4.03 Options should be provided in the BCPA shelf so that the first single-unit failure operates a minor alarm when the spare unit is furnished. Otherwise, a unit failure should operate a major alarm. Whenever an alarm is operated, a FAILURE indicator is also lighted on the faceplate of the failed power unit. The indicator is a single LED that is lighted whenever the output voltage of the unit falls below 4.94 volts.

4.04 Each 2-shelf SRDM assembly receives +5 volt power over a separate fused bus from the power shelf. The SPM and adaptive spare SRDM are also powered from a separate fused bus. In addition, each SRDM, the SPM, and the adaptive spare SRDM are fused separately in the SRDM shelf assemblies.

4.05 Switching relays in the SRDM port switch and CMS circuit packs are operated from either a −24 volt or −48 volt standard power source via power leads from the BCPA shelf. Each of these CPs contains two screw switches, S1A and S1B, that must be positioned according to the voltage of the power source. For −48 volt operation, switches S1A and S1B in all PS and CMS circuit packs must be turned to the counterclockwise (open) position, leaving voltage-dropping resistors in series with the power circuit. For −24 volt operation, all S1A and S1B switches in all PS and CMS circuit packs must be turned to the fully clockwise (closed) position to bypass these resistors.

5. MAINTENANCE FEATURES

5.01 Continuous monitoring of all SRDMs in a bay by the SPM and automatic switching to the spare SRDM result in almost immediate service restoration for nearly all SRDM failures. An office minor alarm is operated any time an equipment failure occurs and service is restored. When a failure occurs and service is not restored, for example, when the spare SRDM is already in use, a major alarm is operated. The LED display on the C circuit pack of each SRDM facilitates the rapid location and correction of nearly all troubles affecting the SRDM.

5.02 The KS-20908 DTS (data test set) receiver and the KS-20909 DTS transmitter may be used at test points on SRDMs. The data signal may be monitored at the input to the line terminator (IN) and at the output of the line driver (OUT) on each port of each SP and at the same points of the multiplexed line on the C circuit pack. At the C circuit pack test points, the transmitting and receiving framing pattern for the SRDM and the 8-bit data pattern for each channel may be determined.

5.03 ***Caution: Operate BAY DEFEAT key in the SPM to the DEFEAT position to prevent switching to spare SRDM when performing maintenance operations.*** Maintenance operations in an SRDM bay are normally performed with the BAY DEFEAT key on the SPM operated to the DEFEAT position, permitting continued SPM testing of all SRDMs but preventing any SRDM alarms or switches in the bay. The same conditions may be duplicated in a single SRDM by operating the MODE switch to the NO ALM position. The SPM continues testing all SRDMs and only the affected SRDM is excluded from alarms or switches to the spare. Maintenance may be performed on the affected SRDM only. Any failure detected by the SPM is indicated on the 7-element LED display of the ◗HL37 or HL37B CP.◖

6. GLOSSARY OF TERMS

6.01 Most of the acronyms and abbreviations (terms) are explained when they are first used in the practice. However, the following list is provided as a quick reference.

TERM	DEFINITION
BCPA	Bay Clock, Power, and Alarm
CMS	Common Switch Circuit
CP	Circuit Pack
DDS	Digital Data System
DS-0A	Digital Signal - Zero Level - A Signal
DS-0B	Digital Signal - Zero Level - B Signal
DSX-0	Digital Signal Cross-Connect - Zero Level
D-T	Driver Terminator
DTS	Data Test Set
ISMX	Integral Subrate Multiplexer
LTS	Local Timing Supply
OCU	Office Channel Unit
PM	Performance Monitor
PS	Port Switch
R-C	Resistor-Capacitor
SM-JCP	Subrate Data Multiplexer - Jack and Connector Panel
SP	Subrate Port
SPM	Subrate Performance Monitor
SRDM	Subrate Data Multiplexer
TA	Test Access
T1DM	T1 Data Multiplexer

7. REFERENCES

7.01 Additional information is provided in the following drawings.

NUMBER	TITLE
SD-73080-01	Subrate Data Multiplexer
SD-73081-01	Subrate Data Multiplexer Performance Monitor
SD-73082-01	Bay Clock, Power, and Alarm Circuit

NUMBER	TITLE
SD-73088-01	Multiplexer Jack and Connector Panel and Subrate Data Multiplexer Jack and Connector Panel Circuit
SD-73089-01	5-Volt Power Supply Shelf
J70177D	11-Foot 6-Inch Subrate Data Multiplexer Bay
J70177K	7-Foot Subrate Data Multiplexer Bay
J70177L	7-Foot Subrate Data Multiplexer Expansion Bay
J70177AC	Multiplexer Jack and Connector Panel
J70177AJ	Bay Clock, Power, and Alarms Shelf
J70177AK	5-Volt Power Supply Shelf
J70177AL	Subrate Data Multiplexer and Performance Monitor Assembly
J70177AM	Two-Shelf Subrate Data Multiplexer Assembly
J70177AR	Subrate Data Multiplexer Jack and Connector Panel

7.02 Additional information is provided in the following practices.

PRACTICE	TITLE
107-600-100	Digital Data System — KS-20909 Data Test Set (Transmitter)— Description and Operation
107-601-100	Digital Data System — KS-20908 Data Test Set (Receiver)— Description and Operation
314-910-100	Digital Data System — Office Channel Unit and Auxiliary Circuits—Description
314-912-100	Digital Data System — T1 Data Multiplexer—Description
314-913-100	Digital Data System — Master Timing Supply Interface—Description
314-913-110	Digital Data System — Nodal Timing Supply—Description
314-913-120	Digital Data System — Local Timing Supply—Description
314-914-100	Digital Data System — DSX-0 Cross-Connect—Description
314-915-100	Digital Data System — T1WB4 Data-Voice Multiplexer—Description
314-915-110	Digital Data System — T1WB5 Data-Voice Multiplexer—Description
314-917-100	Digital Data System — Multipoint Junction Units and Auxiliary Circuits—Description
314-970-100	Digital Data System — Multiplexer Jack and Connector Panel and Subrate Data Multiplexer Jack and Connector Panel—Description
314-970-101	Digital Data System — Central Office — 5-Volt Power Supply Shelf—Description, Maintenance, and Testing
314-983-100	Digital Data System — T1 Data Multiplexer Performance Monitor —Description

PRACTICE	TITLE
314-983-110	Digital Data System — Subrate Data Multiplexer Performance Monitor—Description
807-610-181	Performance Requirements for Digital Data System — Five-Volt Power Supply Shelf—Subrate Data Multiplexer and Subrate Data Multiplexer Performance Monitor
880-600-010	Engineering and Implementation Methods System for the Digital Data System and the Switched Digital Data System
880-603-102	Digital Data System — Central Office Engineering—Hub Office Layout

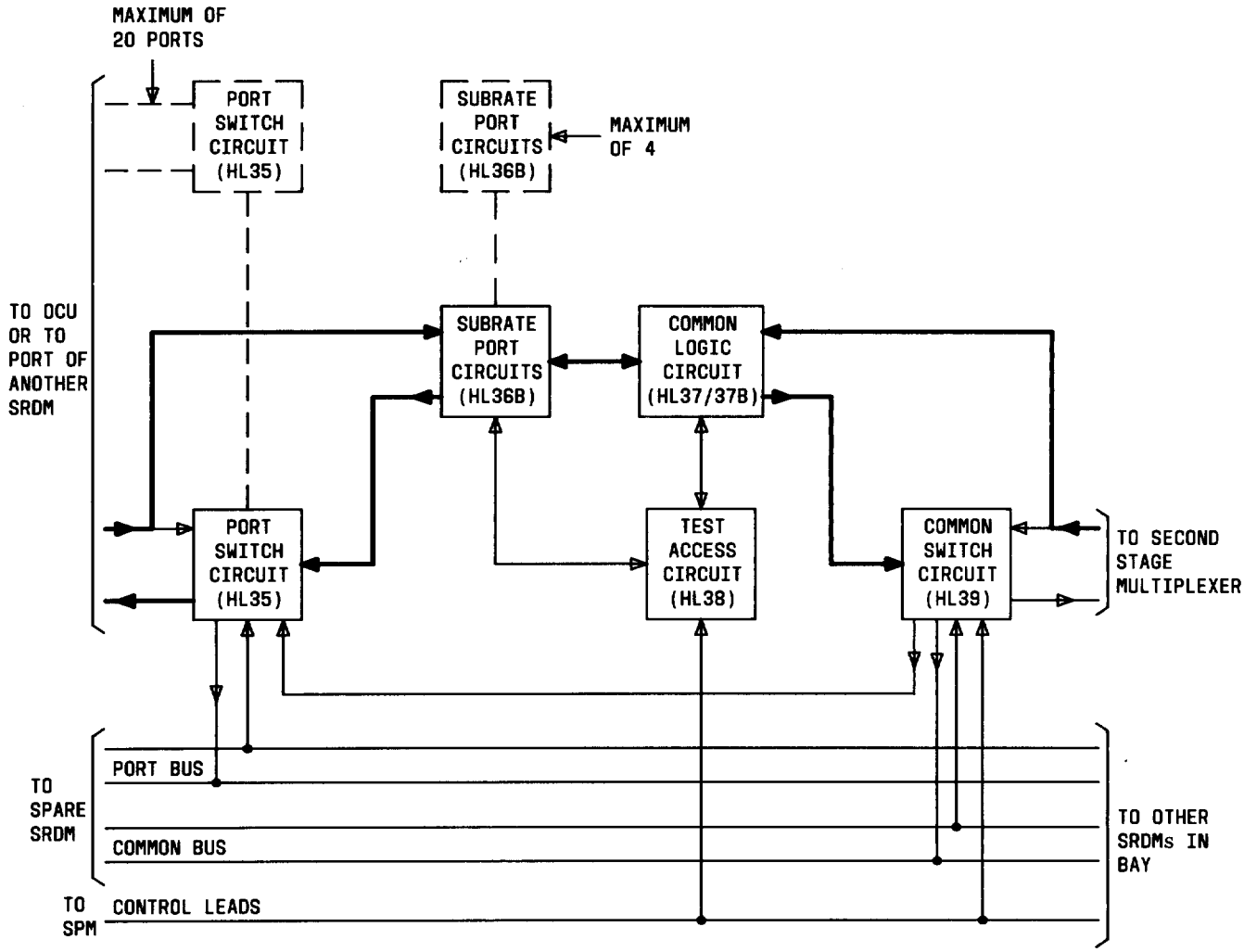

Fig. 1—Subrate Data Multiplexer Block Diagram

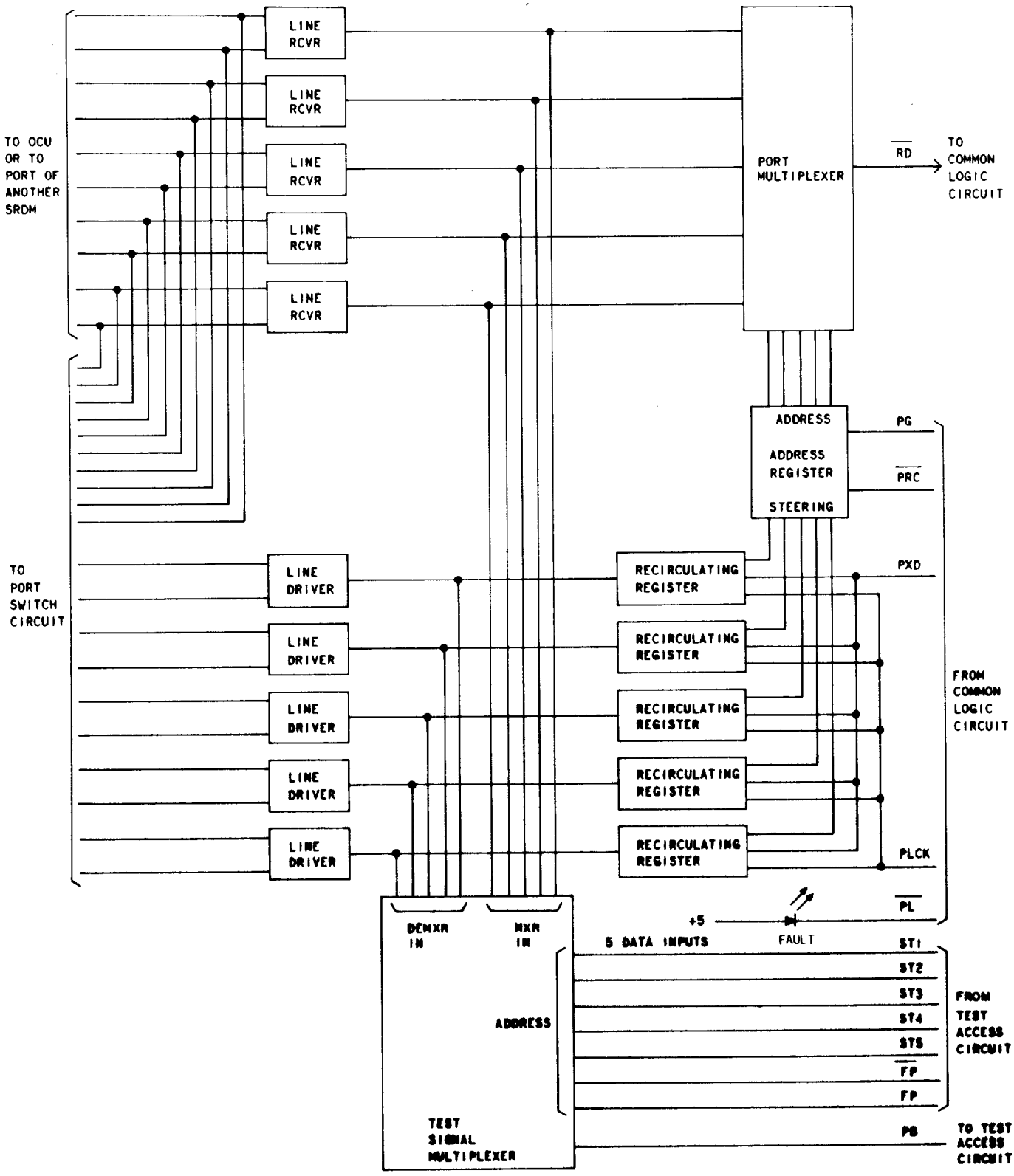

Fig. 2—Subrate Data Port (HL36B) Functional Block Diagram

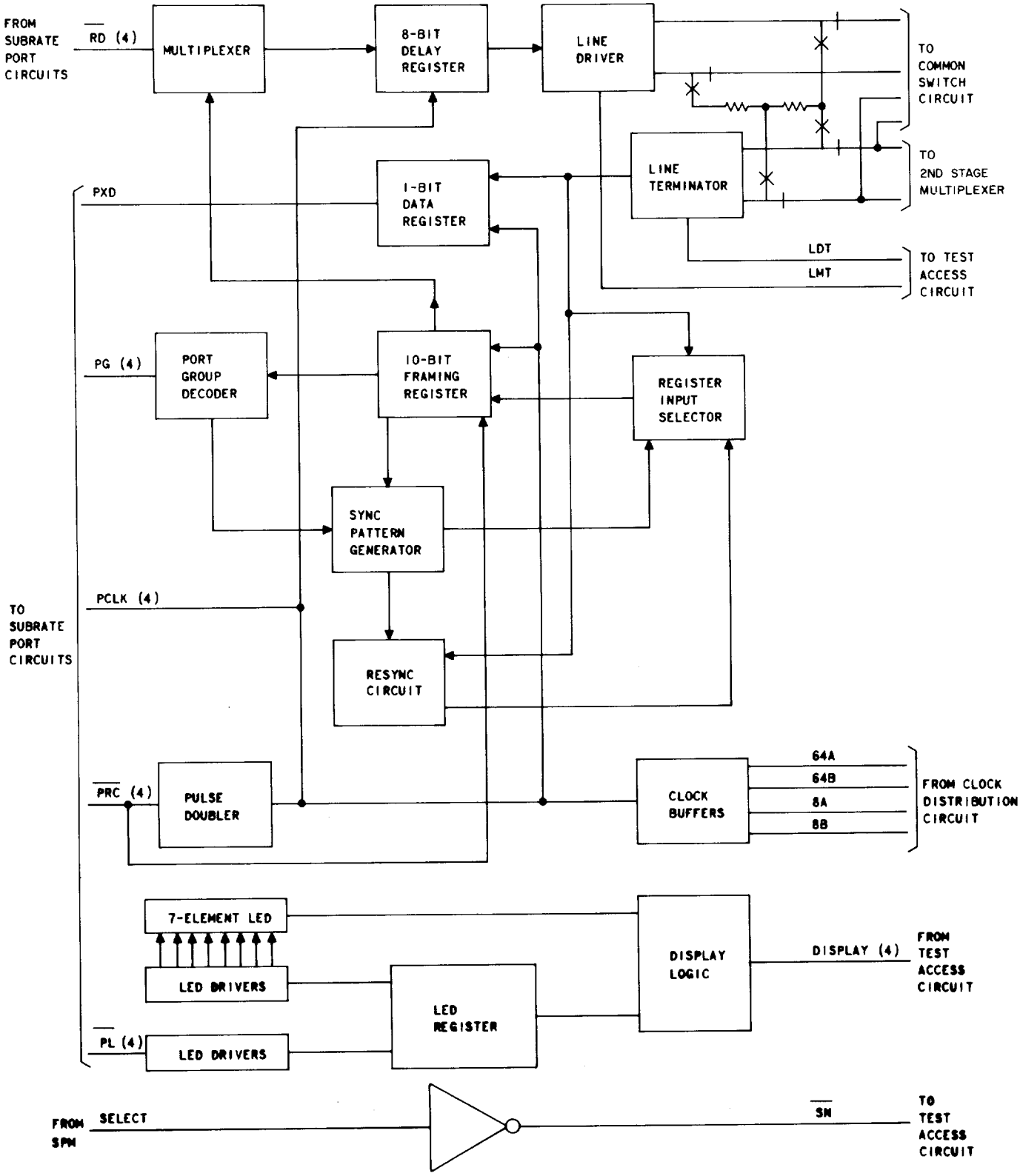

Fig. 3—Common Logic Circuit (HL37/HL37B) Functional Block Diagram

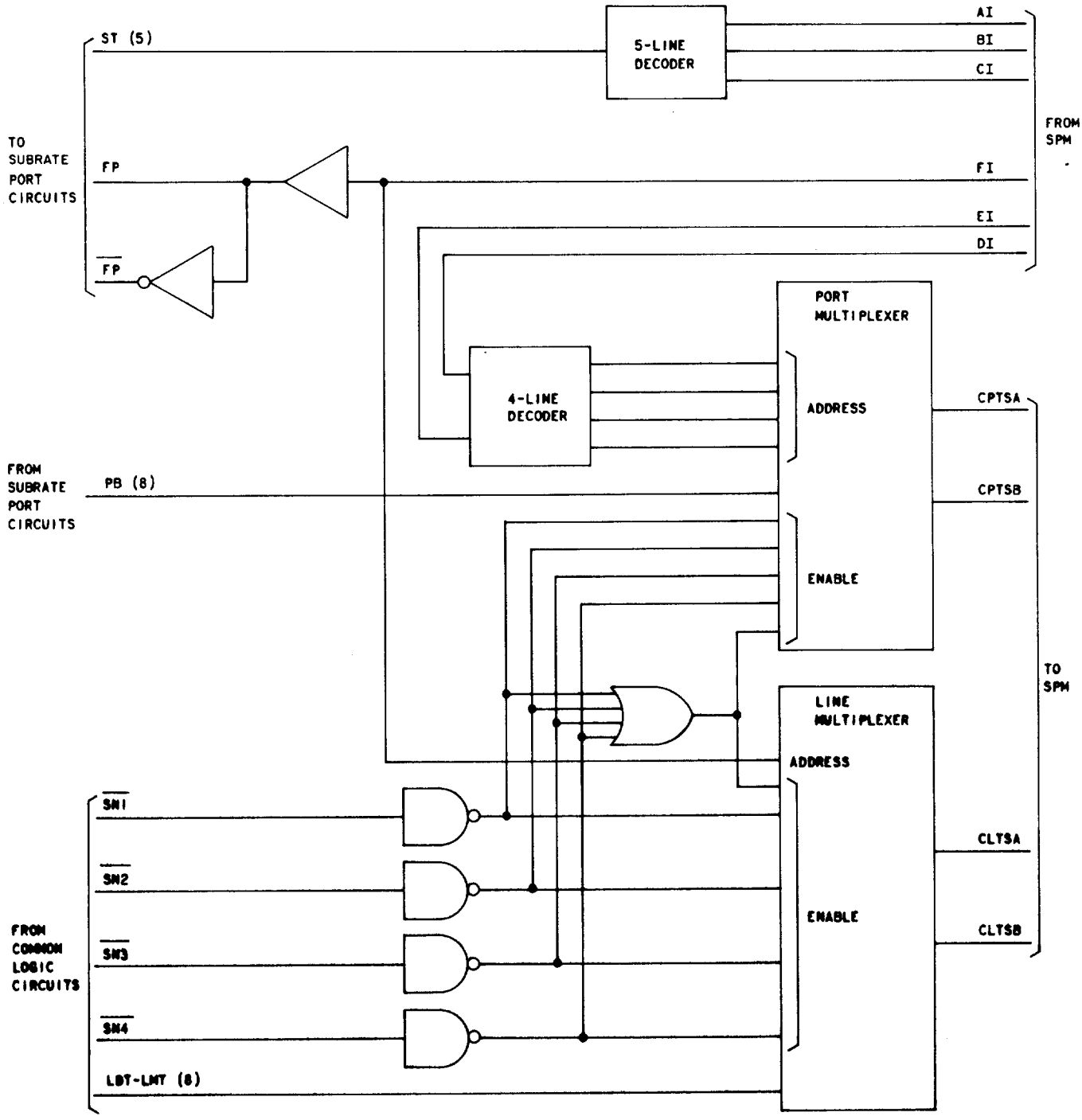

Fig. 4—Test Access Circuit (HL38) Functional Block Diagram

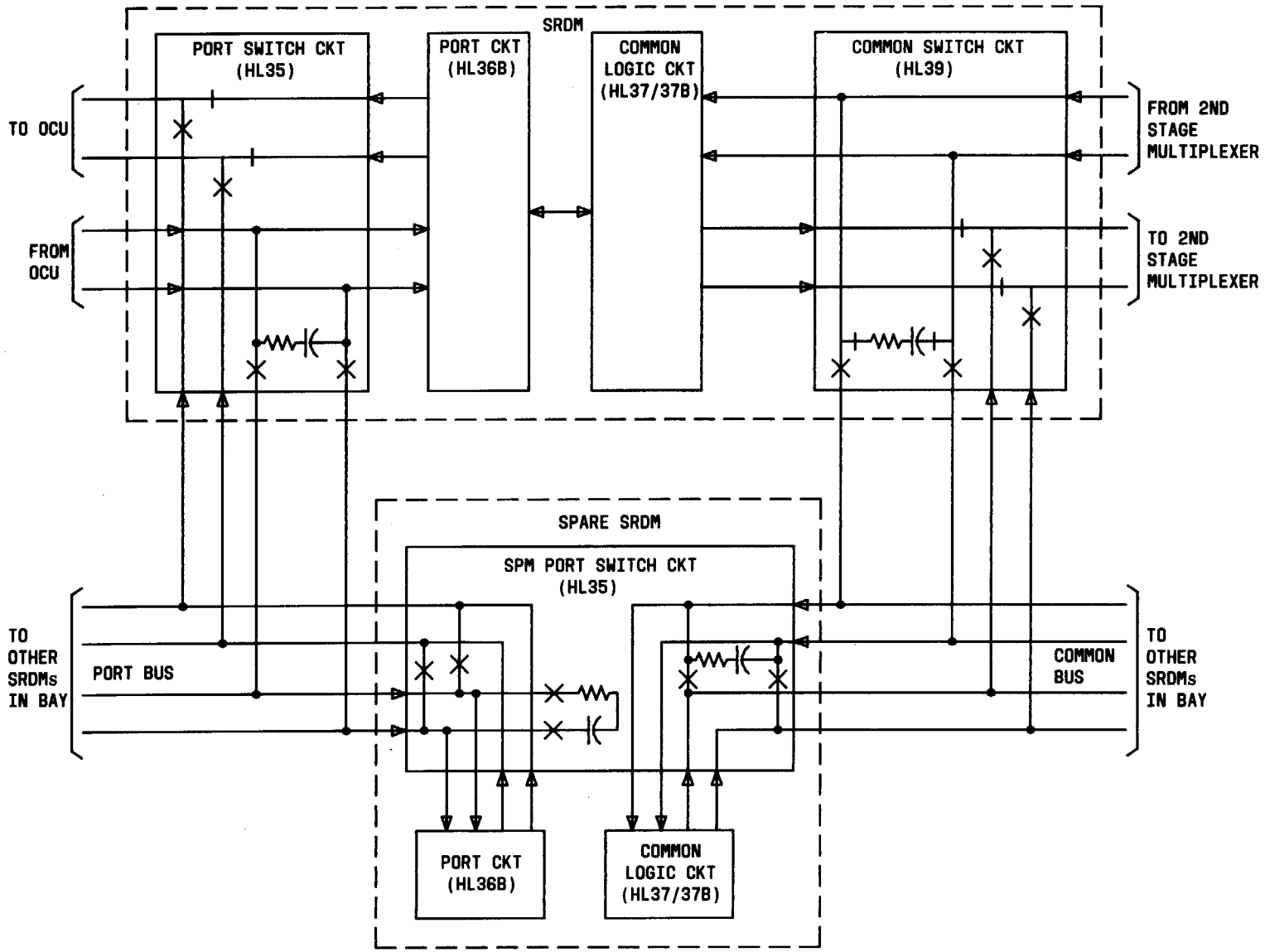

Fig. 5—Port Switch and Common Switch Connections to Spare SRDM

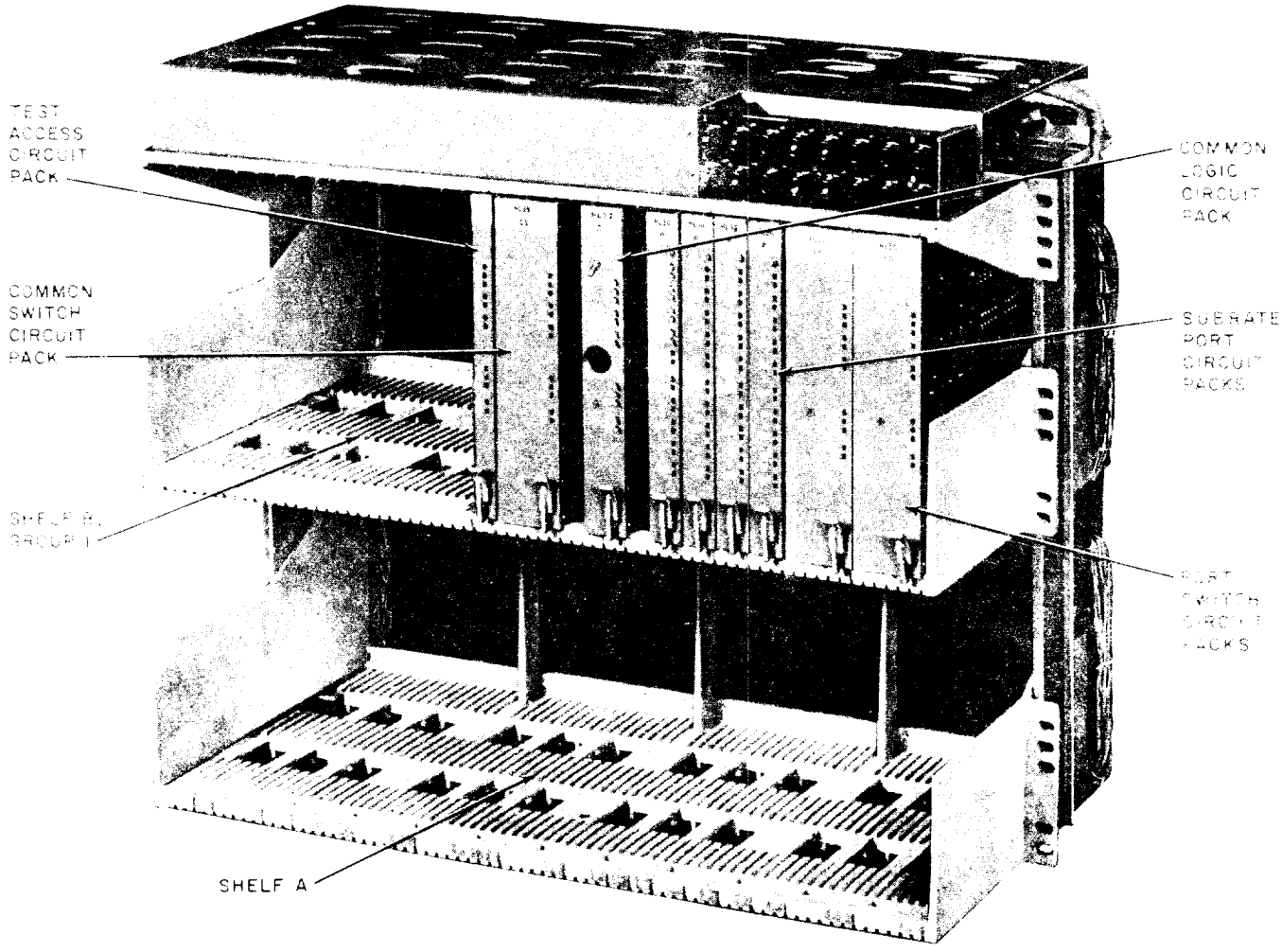

Fig. 6—2-Shelf Subrate Data Multiplexer Assembly (J70177AM)—Front View

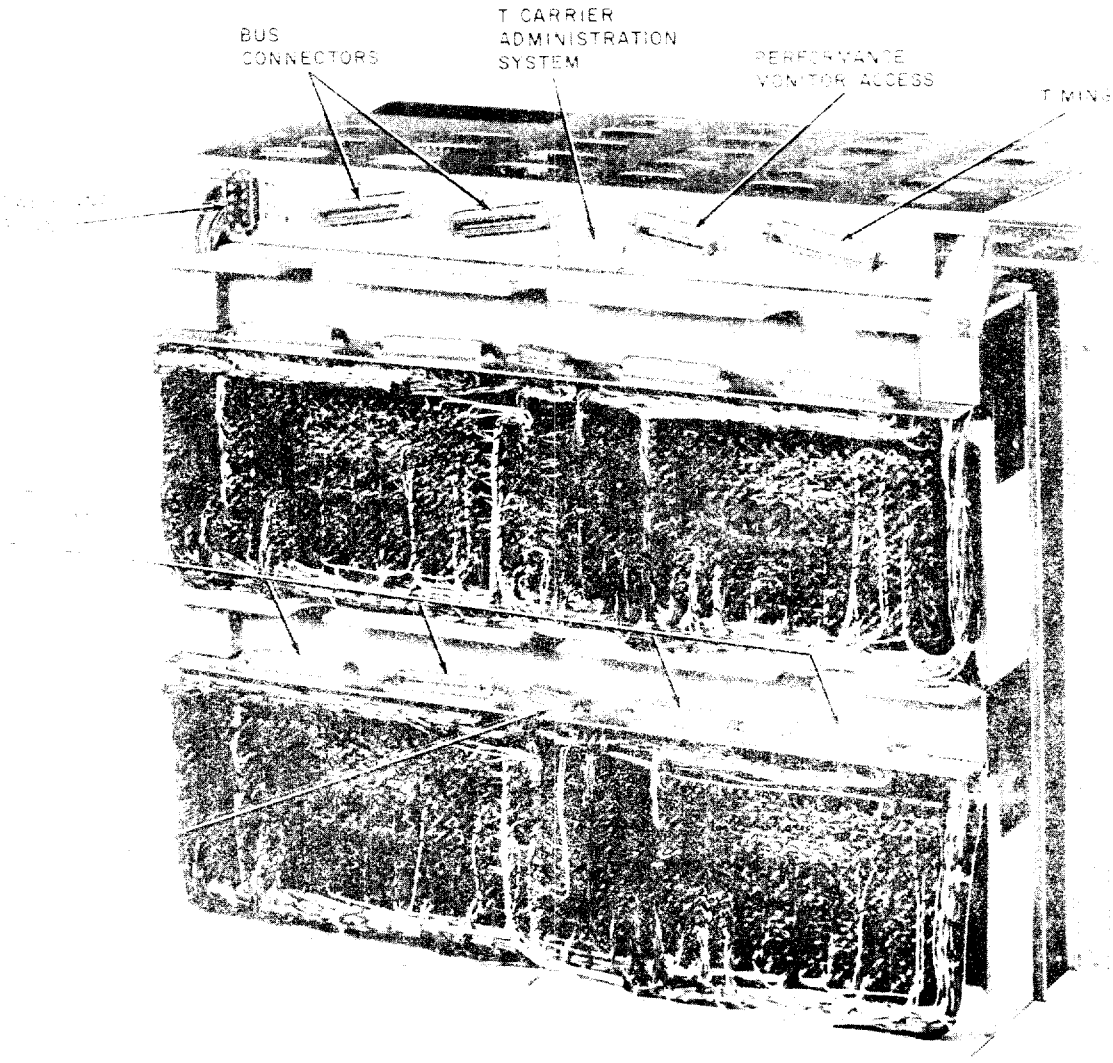

Fig. 7 — 2-Shelf Subrate Data Multiplexer Assembly (J70177AM) — Rear View

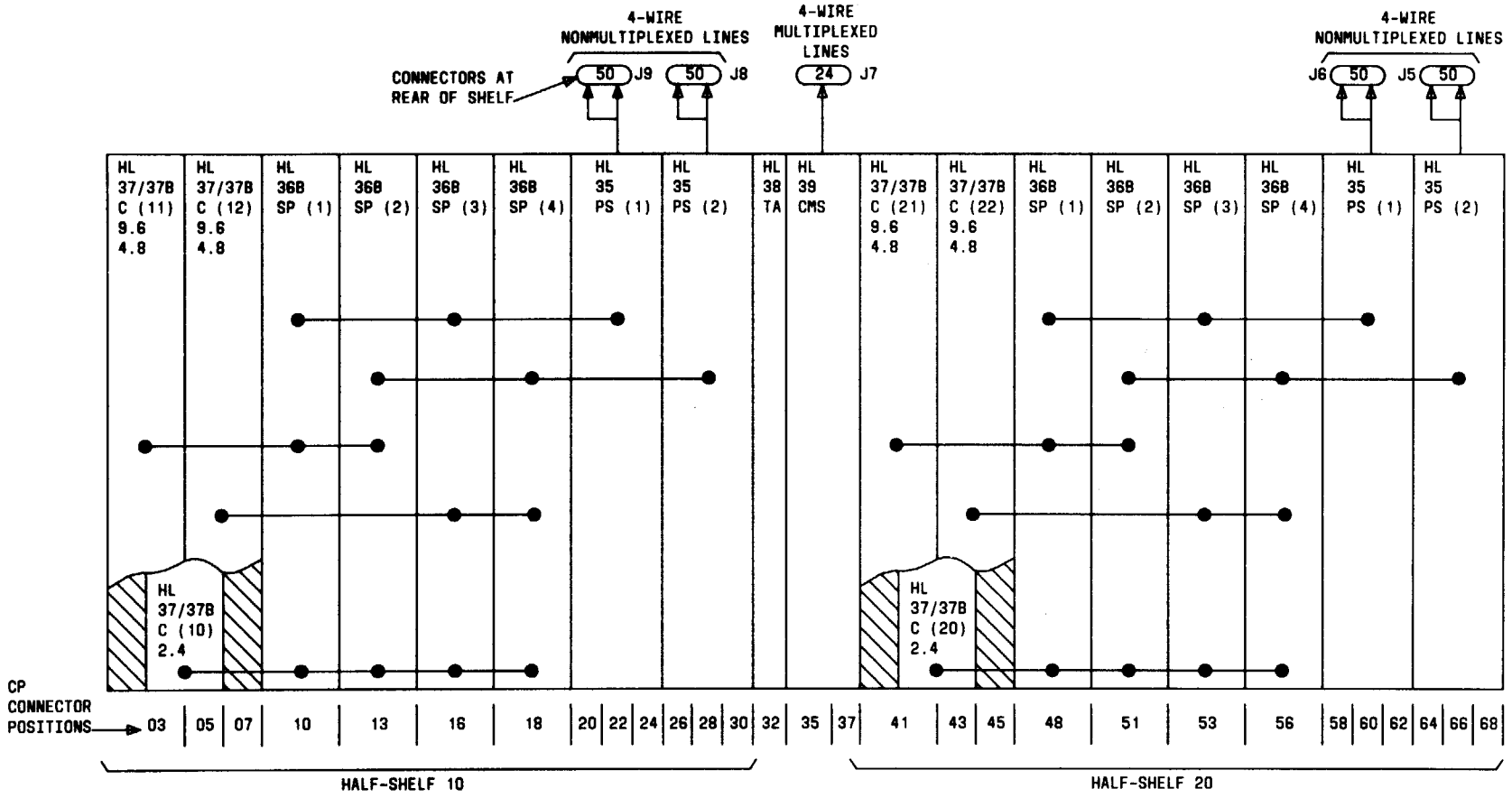

Fig. 8—Shelf Positions and Interconnections of SRDM Circuit Packs

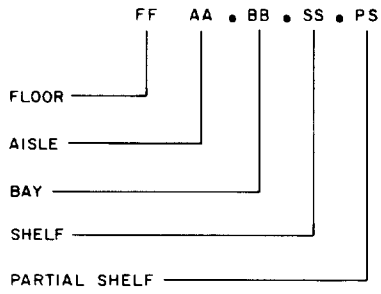

Fig. 9—SRDM Equipment Addressing Format

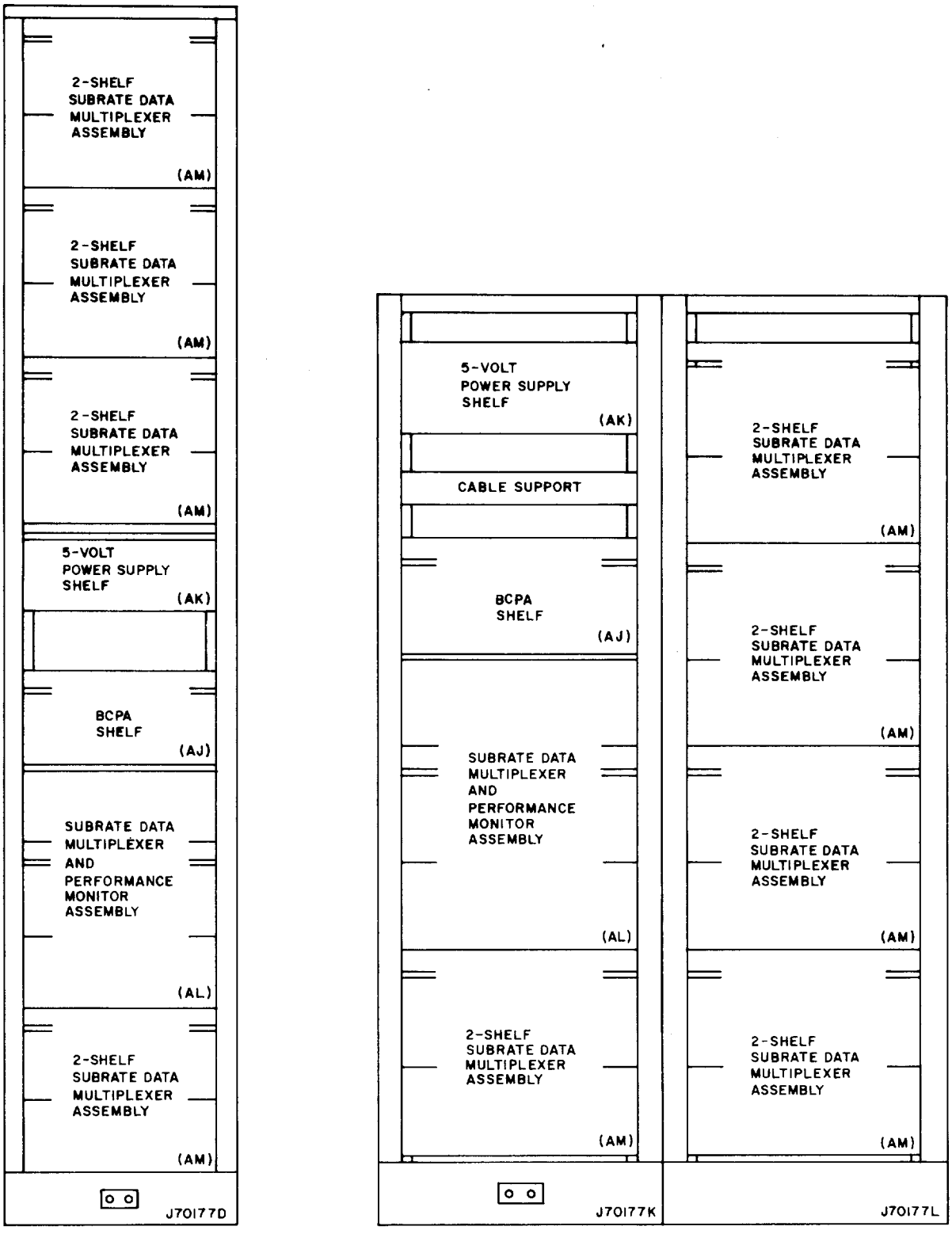

Fig. 10—Subrate Data Multiplexer Bay Arrangements

◆TABLE A◀

SRDM ALPHANUMERIC DISPLAYS (HL37/HL37B CP)

ALPHANUMERIC CHARACTER	INDICATION	ALARM (NOTE)	
		YES	NO
1.2.3.4*	Single port failure on subrate port circuits circuit pack indicated	✓	
8	Test pattern for display LED		✓
C*	Failure on common logic circuit pack	✓	
.0	Transmission failure. Incoming 64-kb/s multiplexed signal does not contain framing pattern but contains some 1s		✓
.U	Unequipped, i.e., SRDM receiving all 0s on incoming multiplexed line		✓
L*	Loss of 64-kHz and/or 8-kHz clock detected by SRDM	✓†	
H	MODE switch in NO ALARM position		✓
.	Failure of SRDM to detect incoming framing sync		✓
H‡	SRDM operational but not returned to service	✓	
Blank	Normal operation		✓

Note:

1. A single SRDM failure results in a minor alarm and in a switch to the spare SRDM. Two or more detected failures result in a major alarm. If the first failure is in the spare SRDM, a minor alarm results but no switch occurs.

* If flashing, service has been switched to spare SRDM

† Alarm occurs only if a legitimate signal with framing is being received from the second stage multiplexer

‡ Flashing

TABLE B

SRDM CIRCUIT PACKS

CIRCUIT PACK MARKING		
APPARATUS CODE	CIRCUIT TITLE	ABBR
HL35	Port Switch	PS
HL36	Subrate Port Circuits	SP
HL37/37B	Common Logic	C
HL38	Test Access	TA
HL39	Common Switch	CMS

TABLE C

SHELF GROUP
SRDM CIRCUIT PACK REQUIREMENTS

SRDM RATE (KB/S)	SRDMS PER SHELF GROUP	HL37/37B IN C POSITION	HL35 IN PS POSITION	NUMBER OF DATAPORTS ACTIVATED	HL36B IN SP POSITION	AVAILABLE PORT NUMBERS
2.4	1	10 or 20	1	5	1	1-5
				10	1, 3	1-5, 11-15
			1, 2	15	1, 2, 3	1-15
				20	1, 2, 3, 4	1-20
4.8	2	11 or 21	2	5	2	6-10
			1, 2	10	1, 2	1-10
		12 or 22	2	5	4	6-10
			1, 2	10	3, 4	1-10
9.6	2	11 or 21	1	5	1	1-5
		12 or 22		5	3	1-5