DIGITAL DATA SYSTEM

MASTER TIMING SUPPLY INTERFACE

DESCRIPTION

CONTENTS PAGE

1. GENERAL

1.01 This section describes the interface units (F59449) used with the master timing supply (MTS), which is part of the Digital Data System (DDS).

1.02 The MTS is identical to the nodal timing supply (NTS) except that two F59449 interface units are substituted for the two HL65 interface units used in the NTS. Also, the input reference signals to the MTS interface units are different (Fig. 1).

1.03 This section describes the operation of only the interface units for the MTS; operation of the common circuits (phase-locked loops, output circuits, etc) between the MTS and the NTS is discussed in Section 314-913-110.

> ***Note:*** The input selector (IS) switch on the display and control unit of the NTS serves no function in the MTS. Switching of the interface units, normally performed by manual operation of the IS switch in the NTS, is automatic in the MTS.

2. FUNCTIONAL DESCRIPTION

2.01 The principal function of each timing supply interface unit (TSIU) is to convert a 2.048-MHz sine wave pilot signal to an 8-kHz square wave signal which is used by the phase-locked loops (PLLs).

2.02 Each TSIU (Fig. 2) receives the 2.048-MHz pilot signal from the Bell System reference frequency standard over separate transmission paths which are locally terminated in a distribution circuit. Connection to the MTS is over two 75-ohm coaxial cables and signals are received at a minimum level of −20 dBm. This redundant arrangement ensures signal continuity if either pilot signal path fails. The primary pilot signal is connected to TSIU-A; the secondary pilot signal, to TSIU-B.

2.03 Each TSIU is basically made up of three sections: the line circuit, the counter circuit, and the output circuit (Fig. 2). The line circuit amplifies and squares the incoming 2.048-MHz pilot signal and sends it to the counter circuit. In the counter circuit, the pilot signal is divided by 256 to form an 8-kHz square wave signal. This 8-kHz signal is sent to the output circuit, which then delivers it to the PLLs.

2.04 In addition to the circuits already described, each TSIU contains circuit logic for monitoring the pilot signal. Normally the working TSIU is TSIU-A. When errors occur in the pilot signal, the 8-kHz output signal of TSIU-A is turned off and is automatically replaced by the output signal of TSIU-B until the errors disappear. The signal-checking process involves sampling and storing the phase of the 8-kHz clock signal from the counter circuit. The sampled information is stored in a register which is updated approximately every second. Each sample is compared with the previous sample. If the comparison indicates a frequency check within approximately one part in two million, the signal is considered good. If the comparison is bad, the phase of the 8-kHz counter is reset to agree with the previously stored good sample. If two consecutive bad comparisons are registered, the phase of the counter circuit is reset to agree with the output phase of the other TSIU (provided that the other TSIU is working properly). If the other TSIU is also registering bad comparisons, the phase of the 8-kHz output is reset to agree with the 8-kHz output of the associated PLL. The

checking procedure continues until a good check is obtained.

2.05 Although both TSIUs produce an 8-kHz output signal, only one TSIU at a time supplies the 8-kHz signal to the PLLs. Under normal operating conditions, TSIU-A supplies the 8-kHz signal to the PLLs. If the signal from TSIU-A is lost or defective, the 8-kHz signal from TSIU-B is automatically sent to the output circuit of TSIU-A and to the PLLs. When the 8-kHz signal of TSIU-A becomes valid again, the PLLs automatically receive the 8-kHz signal from TSIU-A. If the 8-kHz signal from both TSIUs becomes defective, the PLLs automatically free-run as in the NTS.

2.06 TSIU-A also sends a status signal to the PLLs. This status signal indicates to the PLLs whether a valid 8-kHz signal is being sent.

3. REFERENCES

314-913-110	Digital Data System—Nodal Timing Supply—Description
314-913-300*	Digital Data System—Master Timing Supply—Maintenance and Troubleshooting
314-913-500	Digital Data System—Master Timing Supply—Tests
880-601-110*	Digital Data Systems—Synchronization Network
CD- & SD-73083-01	Digital Data System—Central Office Nodal Timing Supply
SD-73087-01	Digital Data System—Station and Central Office System Interconnection and Application Schematic
SD-99596-01	System Block Diagram—Digital Data Service

*This section may not have been issued yet; check the applicable index to determine whether it is available.

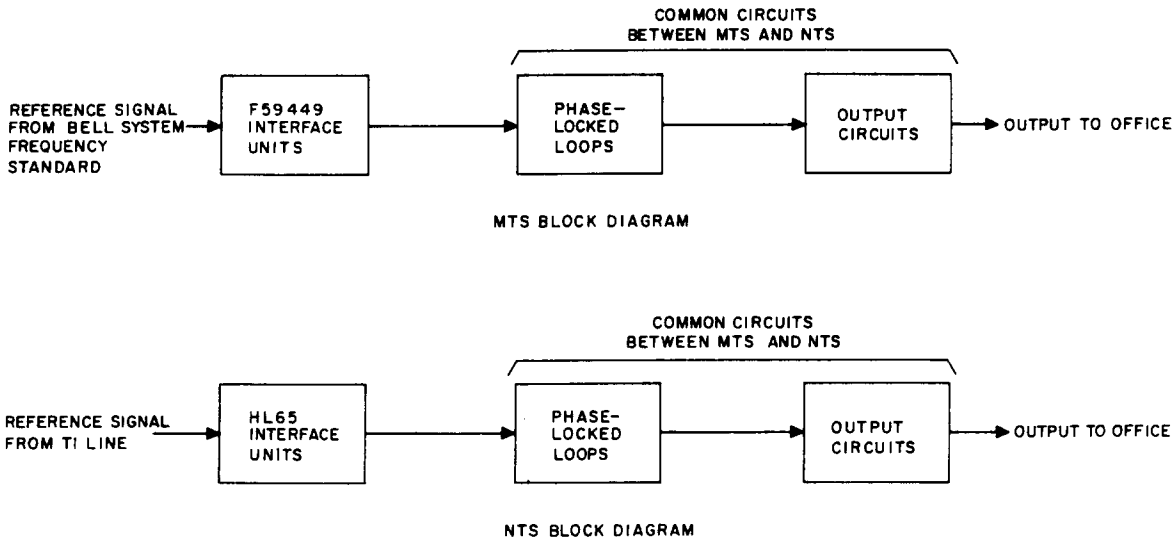

Fig. 1—Circuit Relationship Between MTS and NTS

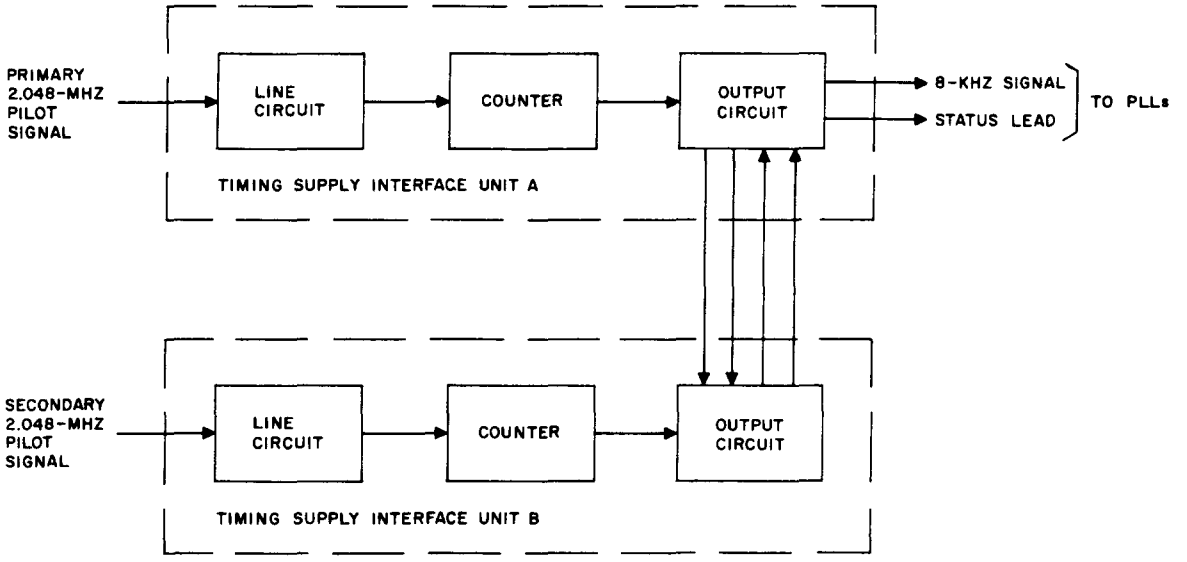

Fig. 2—Timing Supply Interface Units—Block Diagram