DIGITAL DATA SYSTEM
NODAL TIMING SUPPLY
DESCRIPTION

CONTENTS PAGE

1. GENERAL

1.01 This section describes the nodal timing supply (NTS) (J70177E or J70177M), which is part of the Digital Data System (DDS).

1.02 The discussions in this section assume a general knowledge of the fundamentals of digital transmission (see Section 365-010-100). A working knowledge of the T1 (DS-1) signal is helpful.

1.03 The DDS requires systemwide synchronization to preserve customer data. To establish uniform synchronization at all points in the system, a treelike structure has been established (see Fig. 1). Synchronizing information, or timing, is transmitted to all offices in the DDS via the DS-1 signal. The master timing supply (MTS), which is referenced to the Bell System frequency standard, is located at the base of the tree structure and sends timing information, via T1 data multiplexers (T1DMs), to the main branches or to the first NTSs in the tree structure.

1.04 The NTS phase-locks to the incoming master timing signal and internally generates a timing signal of the same frequency as that of the MTS. The NTS then distributes its timing signals to all DDS equipment in the office and, via T1DMs, to other timing supplies farther from the master timing reference. The timing signals can be sent to another NTS, to a secondary timing supply (STS), or to a local timing supply (LTS).

1.05 The STS phase-locks to the incoming signals and internally generates a signal of the same frequency as that of the preceding timing supply. The STS then distributes its timing signals to all DDS equipment in the office and, via T1DMs, to either another STS or an LTS.

1.06 The LTS phase-locks to the incoming signals and internally generates a signal of the same frequency as that of the preceding timing supply. The LTS then distributes its timing signals to all DDS equipment in the office.

1.07 Although the NTS, STS, and LTS perform the same functions, the NTS has the ability to free-run, or act as a master, without slips for several days, whereas the STS and the LTS can free-run without slips for only a few seconds.

1.08 To maintain the treelike timing configuration, timing information is extracted only from certain DS-1 lines in the DDS network.

1.09 Normally, the NTS is used in hub offices; however, the STS may be used in small hub offices or in offices that do not supply timing to other hub offices. The LTS is used in local offices.

1.10 The NTS is a highly stable timing source whose frequency is controlled by monitoring the framing bits of an incoming DS-1 signal. The NTS is, in effect, a secondary frequency standard. If timing on the incoming DS-1 line is lost or defective, the NTS will free-run, or act as the master reference, for all timing supplies that are farther from the MTS. The NTS also provides 8- and 64-kHz timing signals for all DDS equipment in its own office.

© American Telephone and Telegraph Company, 1974
Printed in U.S.A.

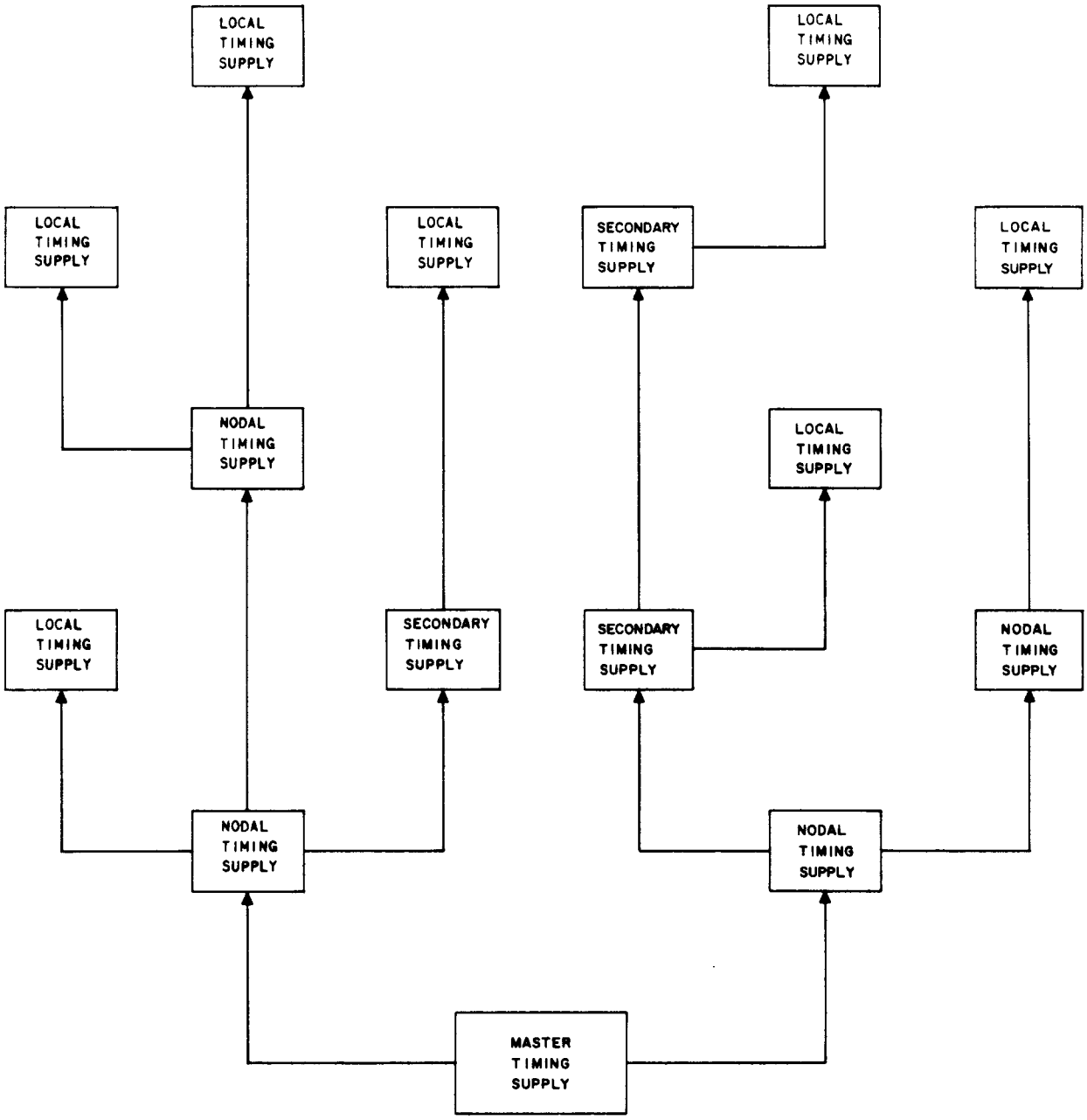

Fig. 1—DDS Synchronous Timing Network Tree

2. FUNCTIONAL DESCRIPTION

General Operation

2.01 The NTS is basically made up of three functional sections: (1) two interface units, (2) two phase-locked loops, and (3) two output circuits (Fig. 2). Other circuits involved in the operation are discussed later in this description. The redundancy in each section of the NTS ensures continuous operation if one circuit fails.

2.02 The principal function of each timing supply interface unit (TSIU) is to locate and extract the 193rd bit in each frame from the incoming DS-1 signal. The extracted framing pulses, which occur at an 8-kHz rate, are sent to both phase-locked loops (PLLs). Although both TSIUs are in

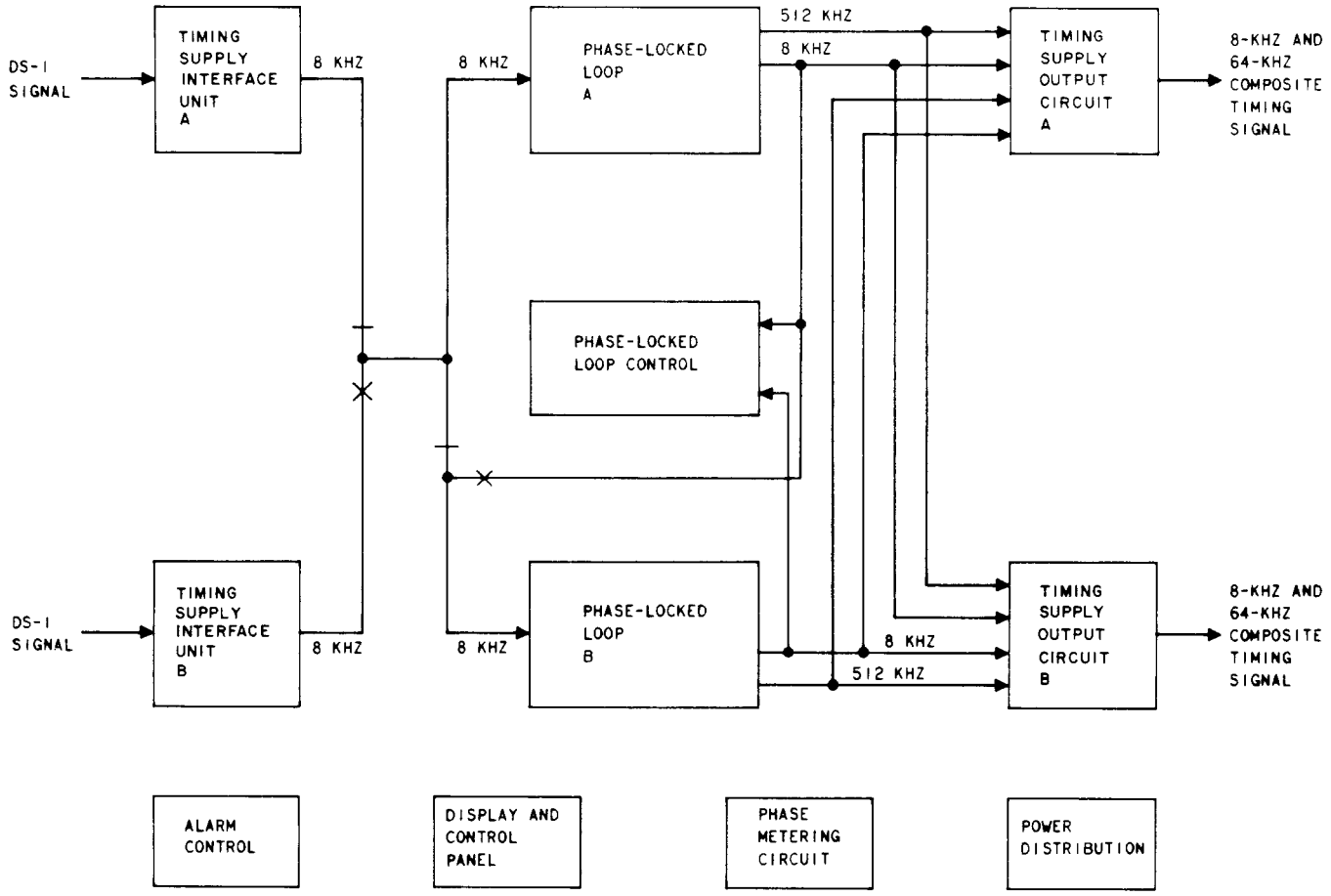

Fig. 2—Nodal Timing Supply Signal Paths—Block Diagram

simultaneous operation, only one TSIU at a time supplies the 8-kHz signal to the PLLs. Therefore, if one TSIU fails, the other TSIU can be manually switched into the circuit to supply the 8-kHz signal to the PLLs.

2.03 The two complete PLLs contained in the NTS are locked to only one TSIU during normal operation. Each PLL contains a highly stable oscillator that locks to the incoming 8-kHz signal. The oscillator output is counted down into the 512- and 8-kHz signals that are used by the timing supply output circuits (TSOCs). If the 8-kHz signal from the TSIU becomes defective or vanishes, the oscillator in phase-locked loop A (PLL-A) will free-run and the oscillator in phase-locked loop B (PLL-B) will lock to the output of PLL-A. As a result, the NTS can continue to provide proper timing signals.

2.04 The redundancy of circuits is again used in the TSOCs. Both TSOCs accept signals from only one PLL at a time. If one PLL fails, the TSOCs automatically accept the signals from the other PLL. The accepted 512- and 8-kHz signals are converted by the TSOCs into composite 8- and 64-kHz signals, which are sent to all bay clock, power, and alarms (BCPA) circuits in the office (see Section 314-916-100).

Timing Supply Interface Units

2.05 The TSIU, circuit pack (CP) HL65, receives its timing signals via the DS-1 signal, which is routed to the TSIU from the DSX-1 cross-connect (Section 365-200-110) or equivalent and then to the T1DM. The TSIU presents a high-input impedance to the DS-1 line. The connection between the DSX-1 and the T1DM should be no more than 655 feet of ABAM or 473 feet of 750-type cable.

The connection between the NTS input and the T1DM must be less than 50 feet of ABAM or 750-type cable. The signal amplitude at the DSX-1 must have a pulse height of 3.0 $\pm$0.3 volts and must meet the standard DS-1 pulse shape specifications. For maximum protection against failure, separate incoming DS-1 lines should drive each TSIU wherever possible. If only one DS-1 line is available for synchronization, both TSIUs should be driven by it.

2.06 Each TSIU is made up of three sections: the line circuit, the framing circuit, and the phase build-out circuit (Fig. 3). The line circuit converts the bipolar return-to-zero DS-1 signal to a unipolar nonreturn-to-zero signal and extracts a 1.544-MHz square wave clock signal. The framing circuit takes the data and clock signals and searches for the 193rd bit (F-bit) of each frame. When the F-bit has been found, the TSIU becomes locked to this position. This position is continuously monitored for the proper F-bit code sequence and if sufficient errors are found, the searching procedure is started over. The framing circuit, therefore, divides the 1.544-MHz signal by 193 to obtain the desired 8-kHz signal used by the PLLs.

2.07 Although both TSIUs produce an 8-kHz signal, only one TSIU supplies the signal to the PLLs. The selection of this TSIU is made by manually operating the input selector (IS) switch on the display panel. Since each TSIU produces an 8-kHz signal, these signals may be out of phase if the TSIUs are driven by separate DS-1 lines. A phase build-out circuit is incorporated to align the 8-kHz signal of both TSIUs in phase so that when switching occurs from one TSIU to the other, the PLLs will not see a large change in phase. Each 8-kHz signal can be phase-shifted in steps of one-twelfth of a frame by the phase build-out switch on the faceplate of each TSIU circuit pack.

2.08 The selected TSIU also sends a status lead to the phase-locked loop monitor (PLLC). This status lead indicates to the PLLC whether a valid F-bit is being sent.

Phase-Locked Loops

2.09 The NTS contains two independent, extremely narrowband PLLs, each consisting of a phase comparator, arithmetic unit, 39A voltage-controlled oscillator (VCO), countdown circuit, and slip detector (Fig. 4).

2.10 The principal component of each PLL is the 39A VCO. Each 39A VCO contains an extremely stable crystal oscillator mounted in a double oven. The input to the 39A VCO is converted to a voltage level by a digital-to-analog converter that varies the oscillator frequency. The output of the oscillator is a 5.12-MHz signal which is sent to the countdown circuit, CP HL60 and HL61.

2.11 The countdown circuit divides the 5.12-MHz signal into the 8- and 512-kHz signals used by the TSOCs. It also provides a 4-kHz signal to the phase comparator circuit and other frequencies to other circuits in the NTS.

2.12 The phase comparator, CP HL64, measures the difference in phase between every other incoming 8-kHz F-bit signal and the 4-kHz reference signal from the countdown circuit. The output of the phase comparator is a signal that is proportional to the phase difference of the two inputs. The output is sent to the arithmetic unit. The phase comparator also examines the 8-kHz F-bit signal and notifies the PLLC when no input is detected.

2.13 The signal sent to the arithmetic unit is averaged over an 8.192-second period. The average phase error is fed to the integral register on CP HL62 and is added in the sum register to the output of the integral register. The result is then sent to the 39A VCO by means of a 14-bit parallel digital input which updates the frequency of the oscillator. The integral register, which maintains a perpetual running sum of the phase error, gives the arithmetic unit the ability to remember the past input frequency averaged over a period of 3 days. If the input to the PLL vanishes or becomes defective, the oscillator will free-run at a frequency offset proportional to the accumulated phase error stored in the integral register. Although both PLLs can free-run separately, PLL-A will free-run and PLL-B will lock to the output of PLL-A when this condition occurs.

2.14 The arithmetic unit integral register has the ability to correct the drift of the oscillator. In correcting the drift, however, it may exceed either of its extreme limits, making the PLL unable to phase-lock to the incoming signal. When the ability of the integral register to correct oscillator drift reaches more than half of either extreme limit, an end-of-range (EOR) indication is given.

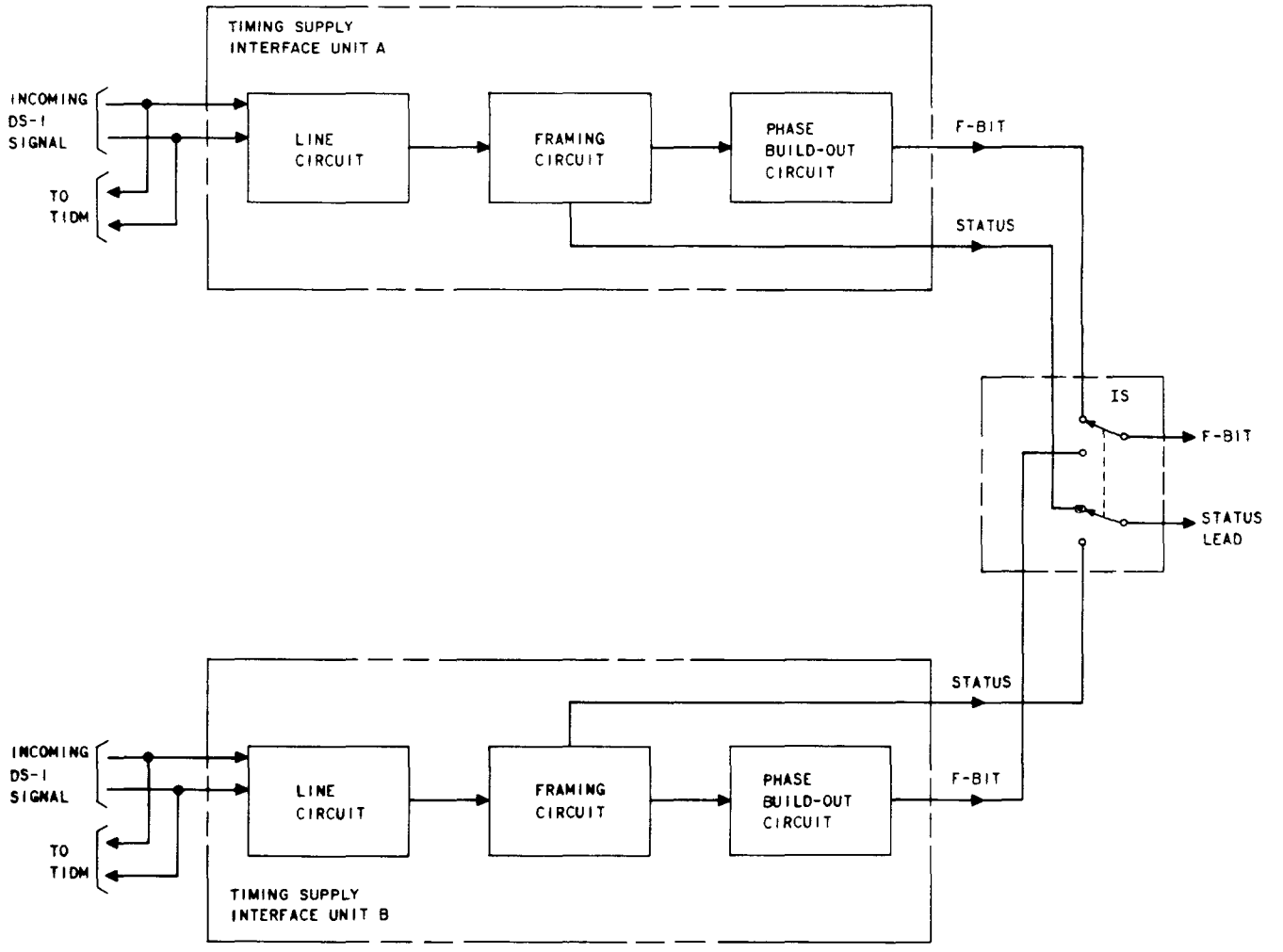

Fig. 3—Timing Supply Interface Units—Block Diagram

2.15 Since the PLL has a very narrow bandwidth (32.5 μHz) in normal operation, it may require several days to lock initially to the incoming signal or it may fail to lock at all. Therefore, a fast-start (FST) switch is incorporated to widen the bandwidth of the circuit and to allow the PLL to lock to the incoming signal in less than 1 hour. This switch is useful after a trouble has occurred and it is desired to restart the PLL quickly. The FST switch has two positions, normal (NORM) and fast start (FST), and is located on the faceplate of CP HL62.

2.16 The slip detector on CP HL63 in each PLL looks for the absence of locking by observing when the phase difference between the two signals presented to the phase comparator progresses through more than one-half cycle. The slip detector informs the PLLC when a slip has occurred in that PLL.

Phase-Locked Loop Control

2.17 The PLLC, CP HL56, controls the inputs and outputs of both PLLs in a manner that ensures continuous operation of the NTS. The PLLC contains a tracking detector and a switching algorithm (Fig. 5).

2.18 The tracking detector measures the phase difference between the 8-kHz outputs of both PLLs. If the two outputs differ in phase by more than one-eighth of a cycle, a NO TRACK signal is given to the switching algorithm circuit.

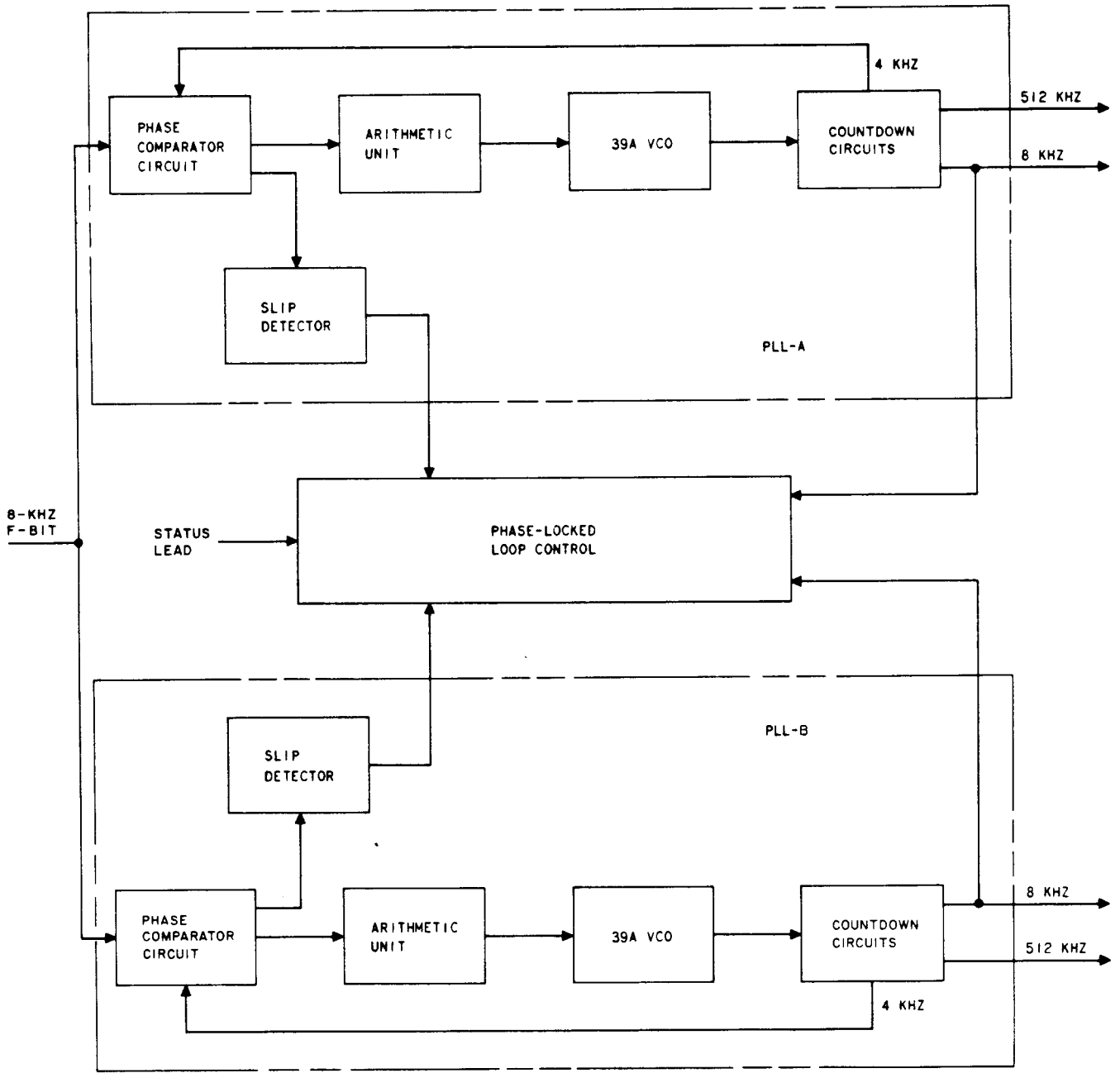

Fig. 4—Phase-Locked Loop—Block Diagram

2.19 The principal function of the switching algorithm is to determine, based on the presence of slips and the output of the tracking detector, whether the input F-bit or either PLL output should be rejected. Three examples follow. First, when the status lead indicates a failure of the incoming F-bit and both PLLs are operating properly, the PLLC causes PLL-A to free-run and PLL-B to lock to the output of PLL-A. In this free-run state, if a SLIP indication is received from PLL-B, both PLLs will free-run independently. The output will continue to be supplied by the same PLL that supplied it before the slip occurred. Second, when a slip signal is received from either PLL, but the status lead indicates a valid F-bit and the tracking detector indicates that the PLLs are tracking, the input F-bit is rejected and again PLL-A free-runs and PLL-B locks to PLL-A. Third,

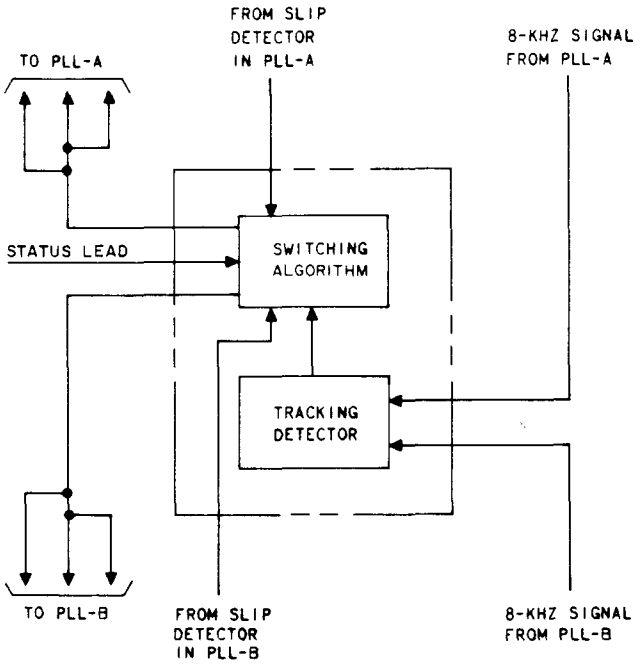

Fig. 5—Phase-Locked Loop Control—Block Diagram

when a slip signal is received from one PLL and the tracking detector indicates a lack of tracking (NO TRACK), the output of the loop that slipped will be inhibited and the other PLL will supply the TSOCs. In this state, if the incoming F-bit is lost, the remaining PLL will free-run. If this PLL then detects a slip, a major alarm is actuated but the output is not inhibited.

Timing Supply Output Circuits

2.20 The signals from both PLLs enter the TSOCs, CP HL59, and go to the clock switching circuits, which make up a common flip-flop switch (Fig. 6). Although signals from both PLLs enter the TSOCs, the clock switching circuits select the signals from only one of the PLLs by monitoring the incoming 8-kHz signal from each PLL. The selected 512- and 8-kHz signals are sent to both the 8- and 64-kHz byte sync framing circuits. If the 8-kHz signal from the selected PLL circuit is interrupted for any reason, the clock switching circuits automatically switch to the signals from the other PLL circuit, which then remains in that condition until the 8-kHz signal is interrupted.

2.21 The 8- and 64-kHz byte sync framing circuits accept the 8- and 512-kHz signals, and convert them into the required 64-kHz bit clock and 8-kHz byte clock formats (Fig. 7A and 7B). These signals are then sent to the line driver circuits.

2.22 Two line drivers, one in each TSOC, provide redundant transmission of the timing signals to each BCPA circuit in the office. The 8- and 64-kHz signals are transmitted to each line via a single line driver that is arranged to transmit bipolar signals. Only one line driver and its associated pair of line leads are used to transmit both the 64-kHz bit clock and 8-kHz byte clock signals. This is accomplished by transmitting only the 64-kHz clock signals and causing a one-pulse violation in the bipolar signal to denote the location of the byte signal (Fig. 7C). The second of the two successive 64-kHz pulses that occur with the same polarity defines the beginning of a byte. Therefore, the first 64-kHz pulse of a byte has the same polarity as the eighth 64-kHz pulse of the previous byte. The byte signal may be easily recognized and extracted from the composite signal at the BCPA circuits in the office. The violations alternate in polarity, and therefore, the signal has no dc component.

2.23 Each TSOC contains six line drivers for distribution of the timing signal. When more timing supply line drivers (TSLDs) are needed, additional CPs HL58, each containing 16 line drivers, may be installed in the NTS. The timing signals from both output circuits must be sent to the same BCPA circuit to have redundancy of operation if one TSOC fails. Therefore, when extra TSLDs are installed with one TSOC, they must also be installed with the other TSOC. Up to five pairs of HL58 circuit packs may be installed for a maximum capability of 86 pairs of timing signal lines.

Alarm Control

2.24 The NTS has a major alarm which indicates a timing supply outage, a minor alarm which indicates an equipment failure that is not serious enough to cause an outage, and an abnormal light which indicates that the timing supply has been manually placed into some irregular condition. The alarms are operated by the timing supply alarm logic (TSAL), CP HL55, which receives signals from all parts of the NTS and from power unit relay contacts that operate when a power unit fails.

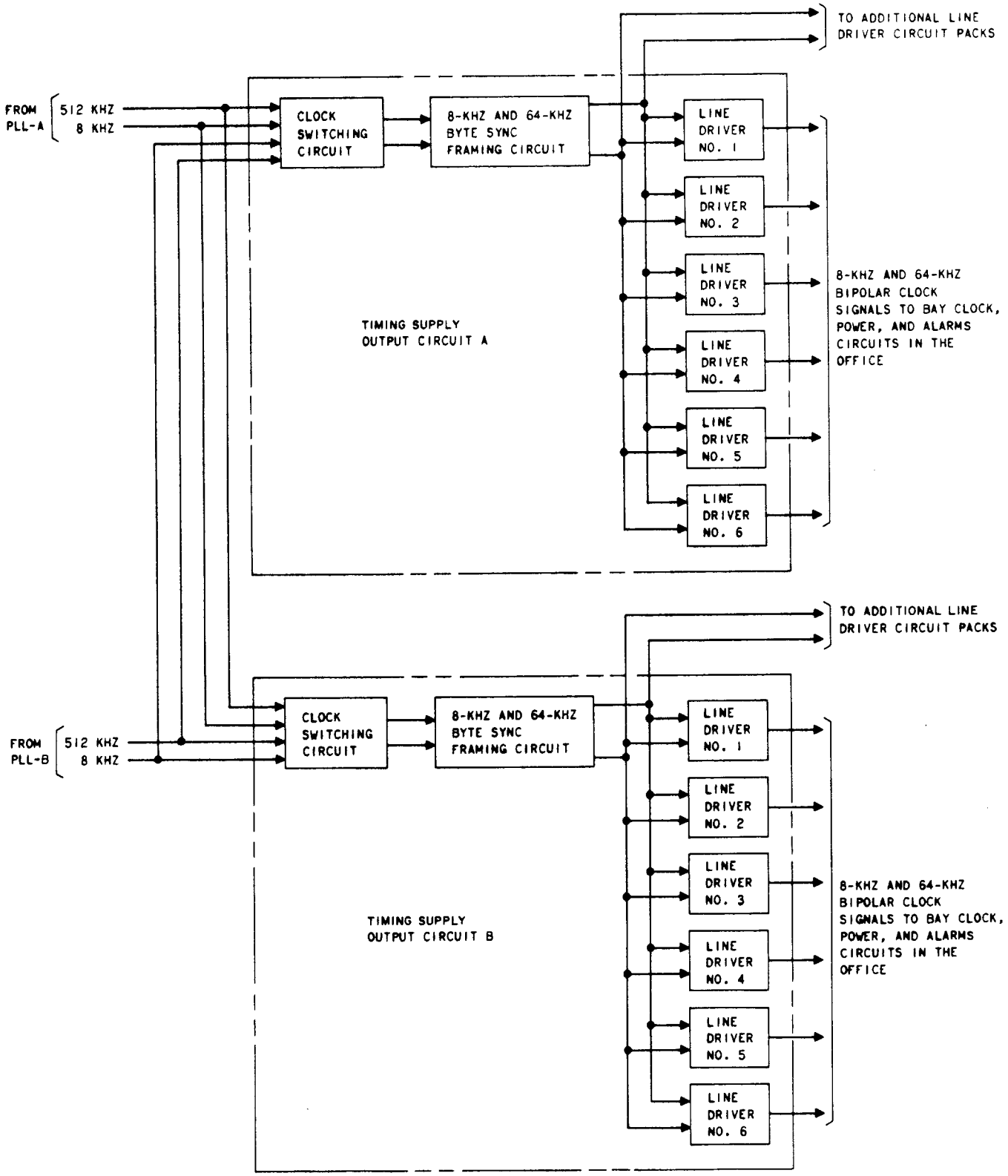

Fig. 6—Timing Supply Output Circuits—Block Diagram

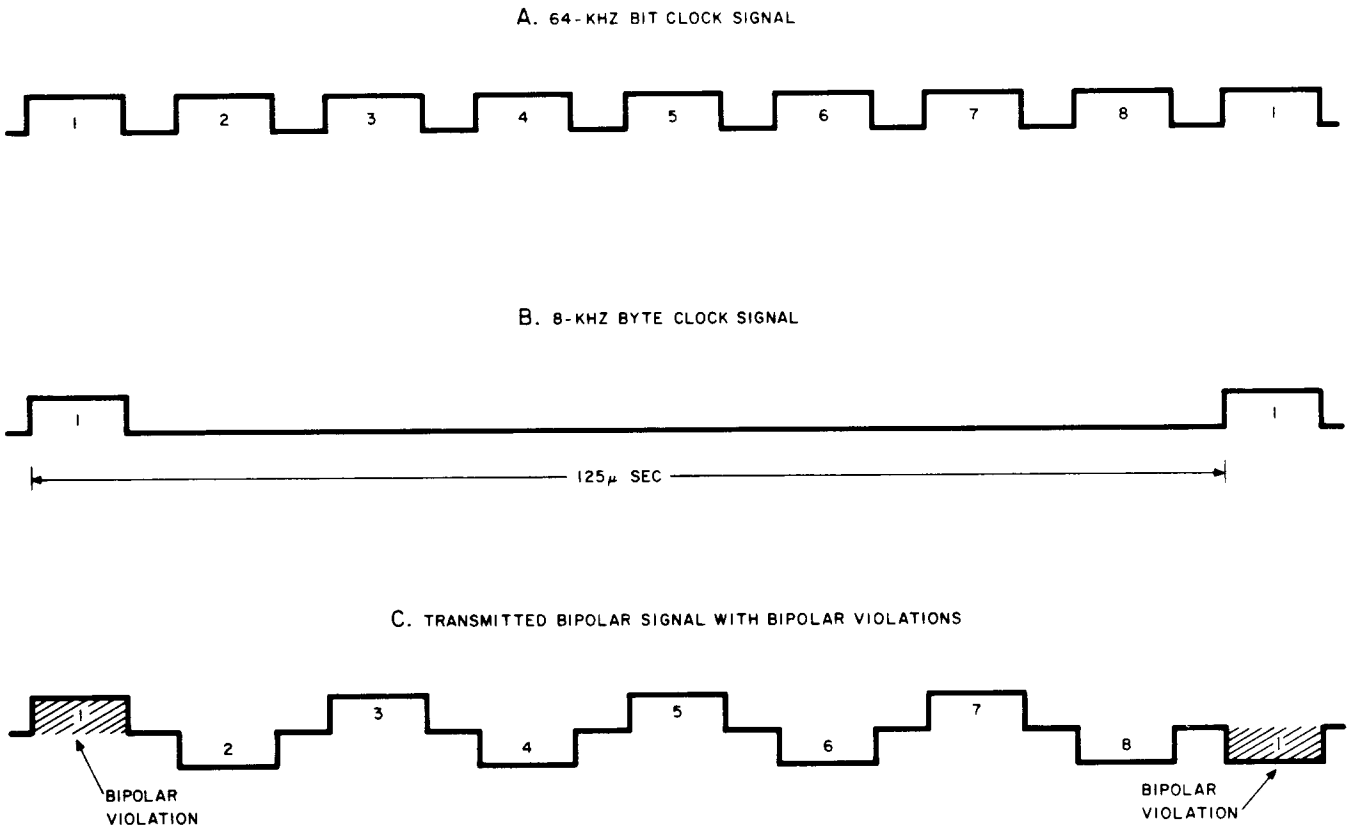

Fig. 7—Clock Waveforms of Output Circuits

2.25 A major alarm is given if:

(a) The PLLC has detected trouble in both PLLs.

(b) The outputs of both PLLs are faulty.

(c) Both TSOCs are faulty.

(d) Both an A power unit and a B power unit fail.

A minor alarm is generated if:

(a) One or both TSIUs cannot find framing.

(b) One or both PLLs give an EOR indication.

(c) A slip is detected in one PLL.

(d) The output of one PLL is faulty.

(e) One TSOC is faulty.

(f) Any power supply fails.

An abnormal indication is given if:

(a) The NTS is free-running because the FREE RUN control key has been operated.

(b) The output of either PLL is inhibited because an INH control key has been operated.

(c) One or both PLLs are in the FST mode.

2.26 The TSAL controls the alarm lights on the display and control unit and generates office audible and visual alarm signals and signals for the T Carrier Administration System.

Display and Control Unit (J70177AN)

2.27 The display and control unit accepts signals from various circuits in the NTS and gives a visual indication of the status of these circuits. The unit contains the major, minor, and abnormal

lamps and the control keys for the NTS. A numerical display for the phase metering circuit is also contained in the unit.

2.28 The display and control unit markings show the three functional sections of the NTS and their interconnecting signal paths (Fig. 8). Each functional section and the signal paths contain lights that indicate the status of each functional section. Table A gives the designation and color of each light on the display and control unit.

2.29 The control keys force certain conditions on the NTS. The IS switch, as described in 2.07, selects the TSIU that supplies the F-bit to the PLLs. The control key on the display and control unit consist of six keys, four of which are interlocking and two of which are momentary contact. Table B gives each key designation and function.

2.30 The display and control unit also contains the major (MJ), minor (MN), and abnormal (ABN) lamps. These lamps, as described in 2.24, are activated by certain conditions of the NTS.

Phase Metering Circuit

2.31 The phase metering circuit (PMC), CP HL57, measures the phase difference between any two selected 8-kHz digital signals. The measured phase is given as a number between 00 (0 degrees of phase difference) and 64 (360 degrees of phase difference). The phase difference is displayed as a decimal number on two 7-segment display units mounted on the display and control unit (Fig. 8). Measurements are taken at a rate of one a second.

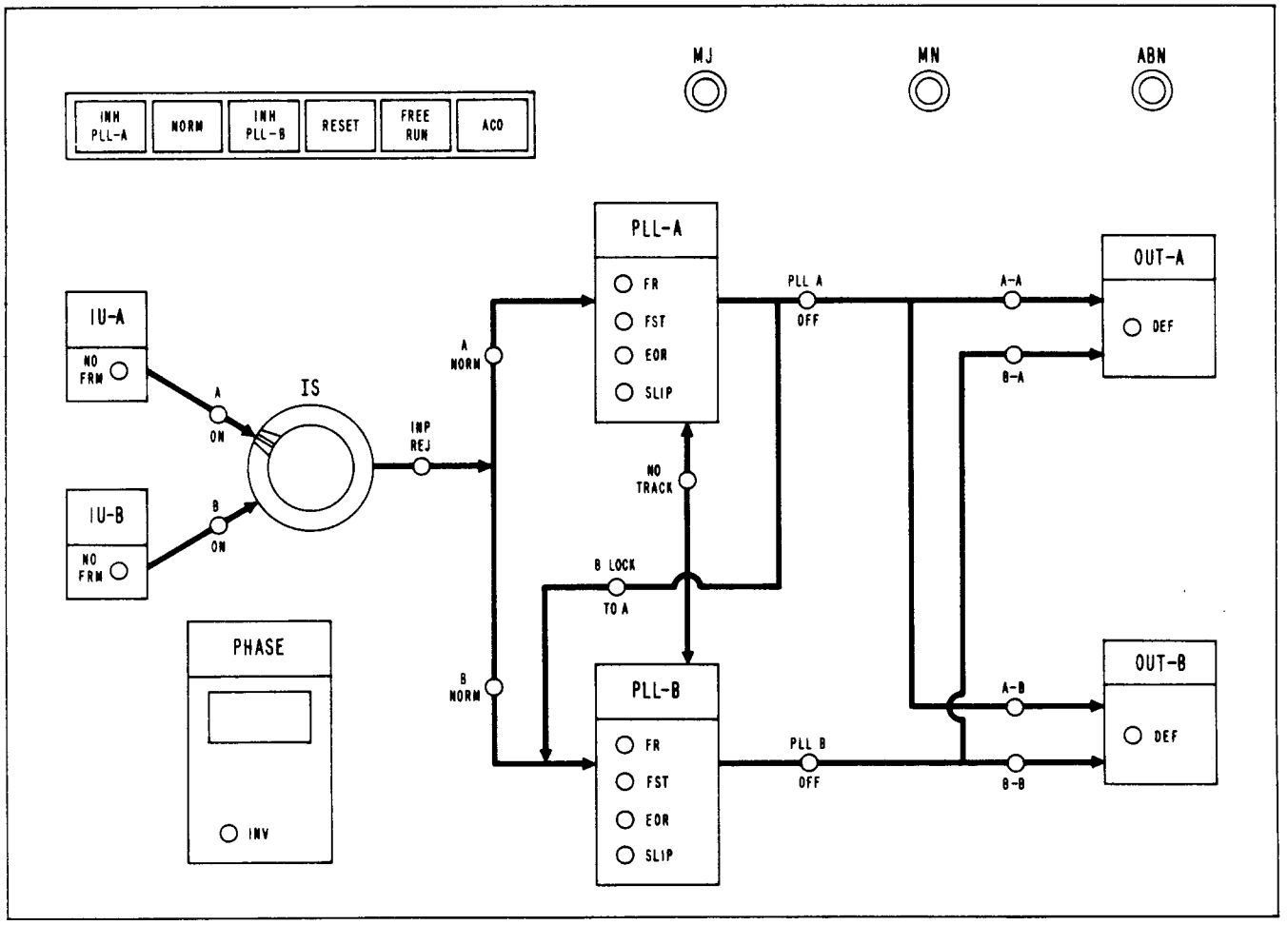

Fig. 8—Nodal Timing Supply Display and Control Unit

TABLE A

LIGHT DESIGNATION	MEANING
NO FRM	The red NO FRAMING light indicates that the respective TSIU cannot lock to the incoming DS-1 signal.
A ON	This green light indicates that TSIU-A is supplying the F-bit to both PLLs.
B ON	This green light indicates that TSIU-B is supplying the F-bit to both PLLs.
A NORM	The green A NORMAL light indicates that there is a normal input to PLL-A.
B NORM	The green B NORMAL light indicates that there is a normal input to PLL-B.
INP REJ	The red INPUT REJECTED light will light if the PLLC has found that the incoming F-bit is faulty, even though the TSIU indicates that it is valid.
FR	The red FREE RUN light indicates that the respective PLL is free-running.
FST	The red FAST START light indicates that the respective PLL is in the fast-start mode.
EOR	The red END OF RANGE light will light when the respective VCO has drifted to half of its range.
SLIP	This red light indicates that a cycle has slipped between the respective PLL and its input.
NO TRACK	This red light indicates that the 8-kHz outputs of the two PLLs differ by more than one-eighth of a cycle.
B LOCK TO A	This red light will light when PLL-B is locked to the output of PLL-A.
PLL A OFF	This red light will light when the output of PLL-A has been inhibited or is defective.
PLL B OFF	This red light will light when the output of PLL-B has been inhibited or is defective.
A-A	This green light will light when PLL-A is providing timing signals to TSOC-A.
B-A	This green light will light when PLL-B is providing timing signals to TSOC-A.
A-B	This green light will light when PLL-A is providing timing signals to TSOC-B.
B-B	This green light will light when PLL-B is providing timing signals to TSOC-B.
DEF	The red DEFECTIVE light indicates that the respective TSOC is faulty.
INV	The red INVALID light indicates that one of the two inputs to the phase metering circuit is not at an 8-kHz rate or is absent.

2.32 The phase difference can be measured between either the positive or negative transition of one input and between either the positive or negative transition of the other input. The transitions used are selected by switches associated with each input. The inputs to the PMC are made via test points 1 (IN1) and 7 (IN2) on the faceplate of the circuit pack.

2.33 When the PMC is not in use, the output display is in a blank condition. Also, when one of the inputs does not have a repetition rate

TABLE B

CONTROL KEY DESIGNATION	FUNCTION
NORM	The NORMAL key is used to release the other interlocking keys, thereby placing the NTS in normal operation.
INH PLL A	The INHIBIT PLL A interlocking key forces the input to the TSOCs from PLL-A to be turned off.
INH PLL B	The INHIBIT PLL B interlocking key forces the input to the TSOCs from PLL-B to be turned off.
FREE RUN	This interlocking key causes PLL-A to free-run and PLL-B to lock to the output of PLL-A.
ACO	The ALARM CUT OFF key is used to turn off the office audible alarms.
RESET	This key resets the PLLC and alarms to a normal state.

of 8 kHz or is absent, a single light located on the display indicates an invalid (INV) input and the numerical display is blanked.

Power Distribution

2.34 The NTS contains four power units for converting office battery to the proper regulated voltages (Fig. 9). Each 39A oscillator is partially powered by a separate +24 volt power unit (OSC-A and OSC-B). All circuit packs in TSIU-A, PLL-A, TSOC-A, and the 39A oscillator of PLL-A receive +5 and −12 volts from logic power unit A. All circuit packs in TSIU-B, PLL-B, TSOC-B, the 39A oscillator of PLL-B, and the PMC receive +5 and −12 volts from logic power unit B.

2.35 The PLLC, the alarm control, and most of the display and control unit lights normally obtain +5 volts power from logic power unit A; if logic power unit A fails, however, logic power unit B automatically supplies power to these circuits via a relay.

2.36 The office battery supplied to the power units may be −48 or −24 volts. Two 74A-type and two 71E-type power units are required when −48 volts is used. When −24 volts is used, two 78A-type and two 76E-type power units are required. For either office battery, two office battery lines are brought into the power units, each supplying one set of power units. The two lines are coupled to the alarm relays via diodes so that the alarm circuitry remains operative if either office battery line fails.

3. EQUIPMENT DESIGN

Bay Arrangement and Markings

3.01 The NTS can be contained in either an 11-foot 6-inch bay or a 7-foot bay. It is arranged in a 5-shelf unit, shown in Fig. 10. The first and second shelves contain oscillators B and A used in the respective PLL. The third shelf contains logic power unit B and circuit packs HL58 though HL65. The fourth shelf contains logic power unit A and circuit packs HL55 through HL65. The fifth shelf contains the display and control unit and the power units for both oscillators.

3.02 Each circuit pack is labeled on the faceplate with an HL number and the function of the circuit pack. Each HL number also has a certain shelf position number in the bay in which it must be installed. Table C gives the HL number, function, and shelf position number of each circuit pack in the NTS.

4. REFERENCES

4.01 The following descriptive sections provide additional information.

314-900-100 Digital Data System—Private Line Service—Overall Description

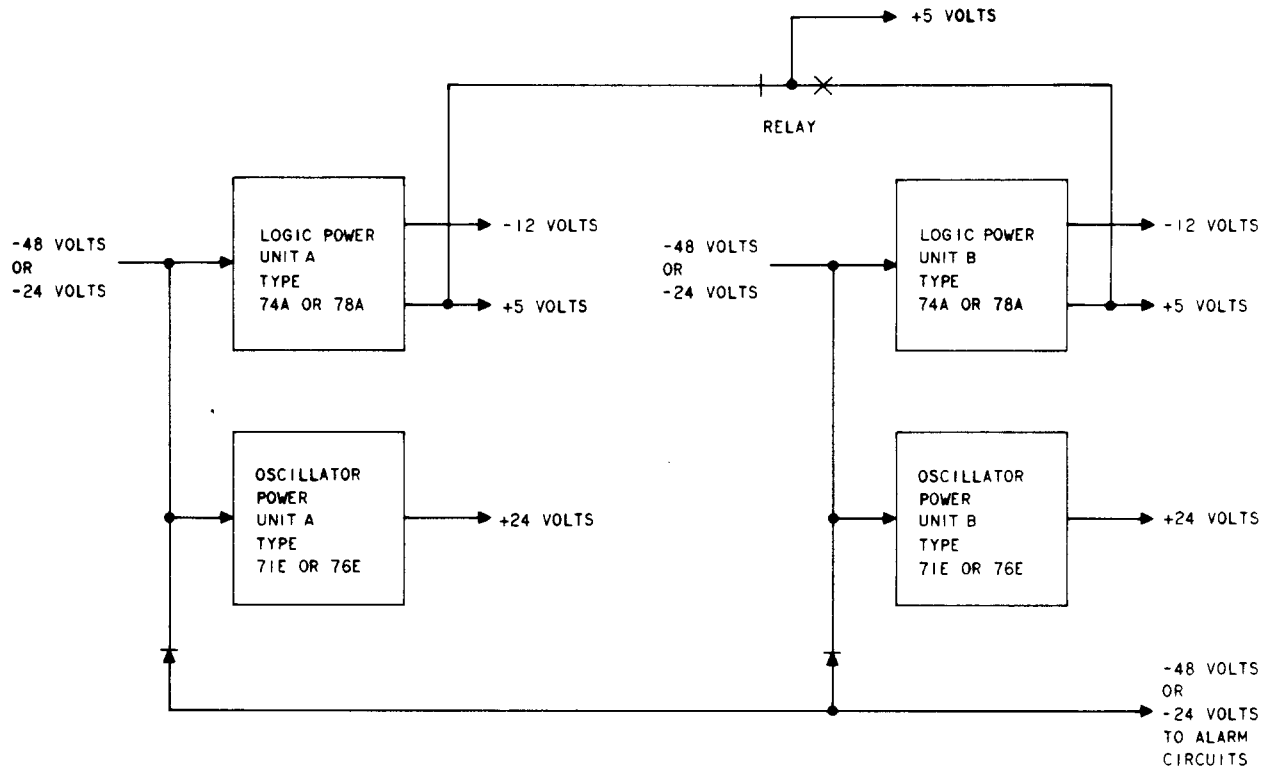

Fig. 9—Nodal Timing Supply Power Distribution

314-912-100 Digital Data System—T1 Data Multiplexer—Description

314-913-310 Digital Data System—Nodal Timing Supply—Maintenance and Trouble-shooting

314-913-510 Digital Data System—Nodal Timing Supply—Tests

314-916-100 Digital Data System—Bay Clock, Power, and Alarms Circuit—Description

365-010-100 Fundamentals of Digital Transmission

365-200-110 DSX-1 Patch and Cross-Connect—Description

886-100-110 Digital Data Systems—Synchronization Network

4.02 Detailed schematics and circuit information are contained in the following SDs and CDs.

CD- & SD-73082-01 Digital Data System—Central Office Bay Clock, Power, and Alarms Circuit

CD- & SD-73083-01 Digital Data System—Central Office Nodal Timing Supply

SD-73087-01 Digital Data System—Station and Central Office System Interconnection and Application Schematic

CD- & SD-99503-01 DSX-1 Patch and Cross-Connect

SD-99596-01 System Block Diagram—Digital Data Service

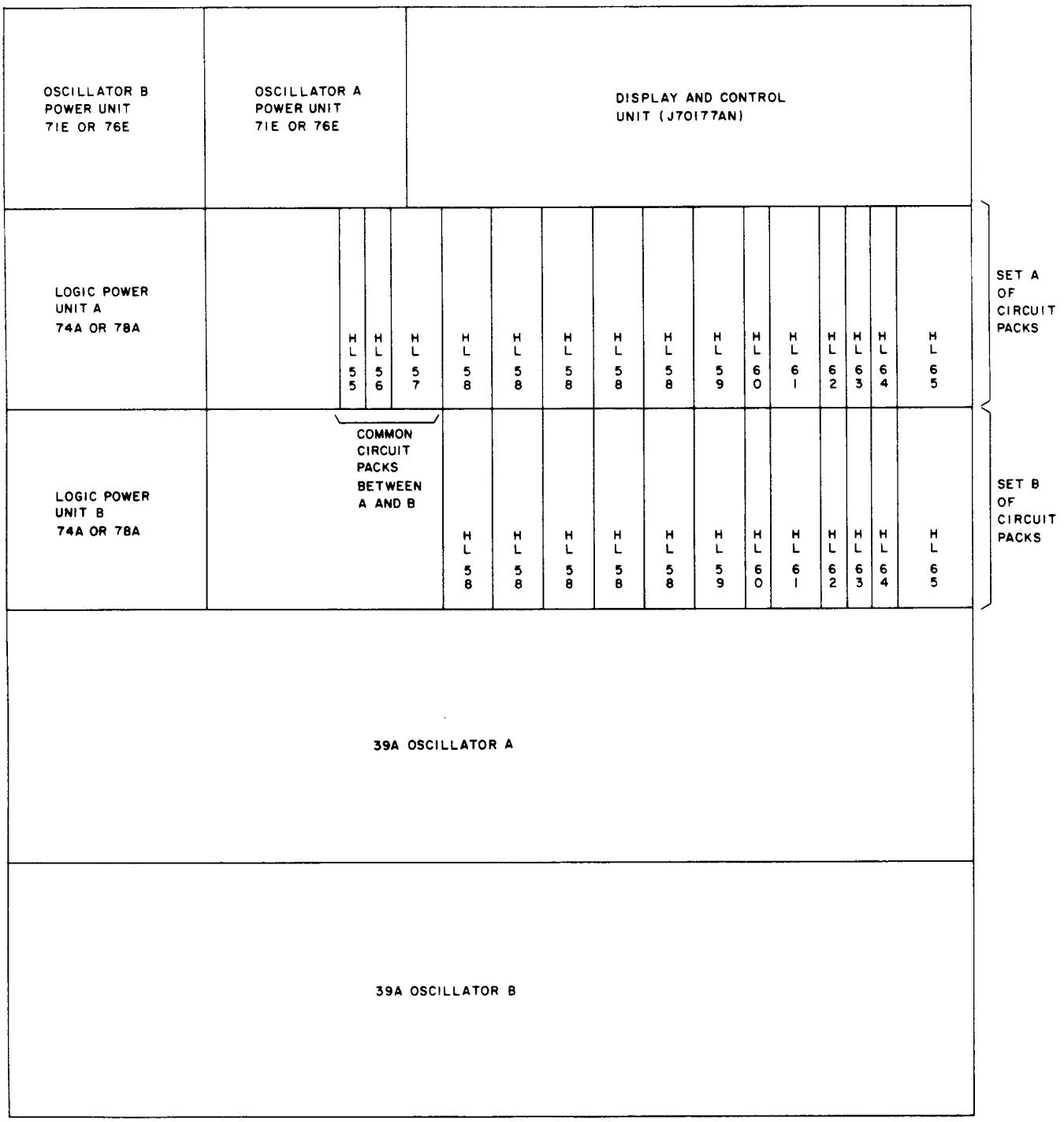

Fig. 10—Shelf Arrangement for the Nodal Timing Supply

TABLE C

HL NUMBER	FUNCTION	SHELF POSITION NUMBER	
		SET A	SET B
55	Timing Supply Alarm Logic (TSAL)	32	
56	Phase-Locked Loop Control (PLLC)	34	
57	Phase Metering Circuit (PMC)	36	
58	Timing Supply Line Drivers (TSLD)	39	39
58	Timing Supply Line Drivers (TSLD)	42	42
58	Timing Supply Line Drivers (TSLD)	45	45
58	Timing Supply Line Drivers (TSLD)	48	48
58	Timing Supply Line Drivers (TSLD)	51	51
59	Timing Supply Output Circuit (TSOC)	53	53
60	High-Frequency Countdown Circuit (HFC)	55	55
61	Low-Frequency Countdown Circuit (LFC)	58	58
62	Integral and Sum Registers (ISR)	60	60
63	Accumulator and Slip Detector (ASD)	62	62
64	Phase Comparator (PC)	64	64
65	Timing Supply Interface Unit (TSIU)	68	68