DIGITAL DATA SYSTEM
SECONDARY TIMING SUPPLY
DESCRIPTION

CONTENTS PAGE

1. GENERAL

1.01 This section describes the secondary timing supply (STS), J70177E or J70177M, which is part of the Digital Data System (DDS). A general knowledge of the fundamentals of digital transmission (Section 365-010-100) is required for a complete understanding of this section. A working knowledge of the T1 (DS-1) signal is helpful.

1.02 If this section is reissued, the reason for reissue will be given in this paragraph.

1.03 The DDS requires systemwide synchronization to preserve customer data. To establish uniform synchronization at all points in the system, a treelike structure has been established (Fig. 1). Synchronizing information, or timing, is transmitted to all offices in the DDS via the DS-1 signal. The master timing supply (MTS), which is referenced to the Bell System frequency standard, is located at the base of the tree structure and sends timing information, via T1 data multiplexers (T1DMs), to the main branches or to the first nodal timing supplies (NTSs) in the tree structure.

1.04 The NTS phase-locks to the incoming master timing signals and internally generates a timing signal of the same frequency as that of the MTS. The NTS then distributes its timing signals to all DDS equipment in the office and, via T1DMs, to other timing supplies farther from the MTS. The timing signals can be sent to another NTS, to an STS, or to a local timing supply (LTS).

1.05 The STS phase-locks to the incoming signals and internally generates a signal of the same frequency as that of the preceding timing supply. The STS then distributes its timing signals to all DDS equipment in the office and, via T1DMs, to either another STS or an LTS.

1.06 The LTS phase-locks to the incoming timing signals and internally generates a signal of the same frequency as that of the preceding timing supply. The LTS then distributes its timing signals to all DDS equipment in the office.

1.07 Although the NTS, STS, and LTS perform the same functions, the NTS has the ability to free-run, or act as a master, for several days without slips, whereas the STS and the LTS can free-run for only a few seconds without slips.

1.08 To maintain the treelike timing configuration, timing information is extracted only from certain DS-1 lines in the DDS network.

Secondary Timing Supply

1.09 The STS delivers 8- and 64-kHz timing signals to all DDS equipment in the office in which it is installed. It maintains synchronization by phase-locking onto the framing bits of the incoming DS-1 signal from an office that is nearer the MTS in the tree structure. If the incoming signal is lost or defective, the STS will free-run at its natural frequency with a loss of accuracy.

1.10 The STS is used in certain hub offices that do not need the highly stable NTS because their synchronization requirements are less critical. If future needs require an NTS, however, the STS can be converted into an NTS (see Section 314-913-215).

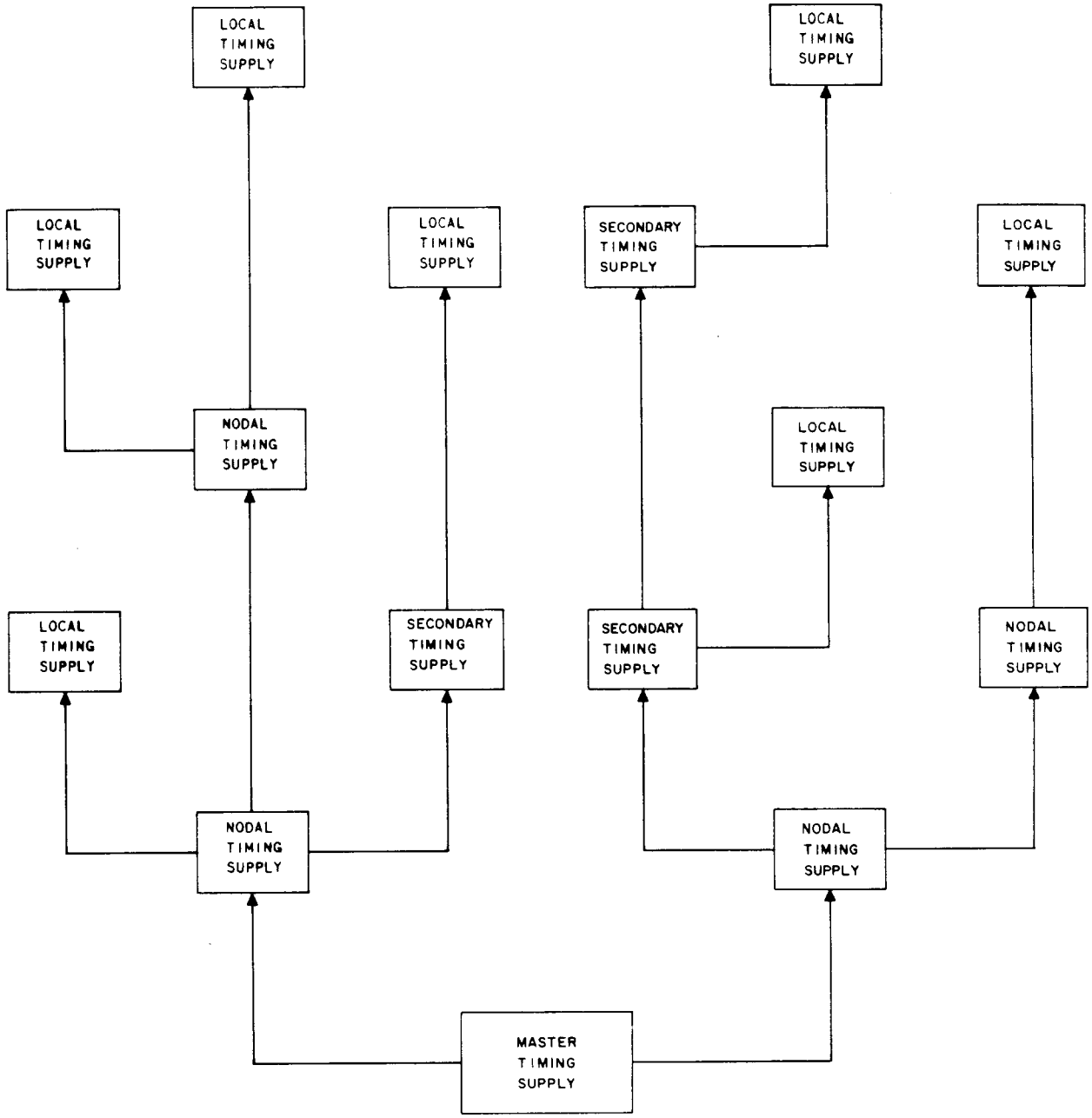

Fig. 1—DDS Synchronous Timing Network Tree

2. FUNCTIONAL DESCRIPTION

General Operation

2.01 The STS is basically made up of three functional sections (Fig. 2): (a) two interface units, (b) two phase-locked loops and two phase-locked loop monitors, and (c) two output circuits. Other circuits involved in the operation are discussed later in this section. The redundancy in each section of the STS ensures continuous operation if one circuit fails.

2.02 The prinicipal function of each timing supply interface unit (TSIU) is to locate and extract the 193rd bit in each frame from the incoming DS-1 signal. The extracted 8-kHz signal is sent to both phase-locked loops (PLLs). Although both

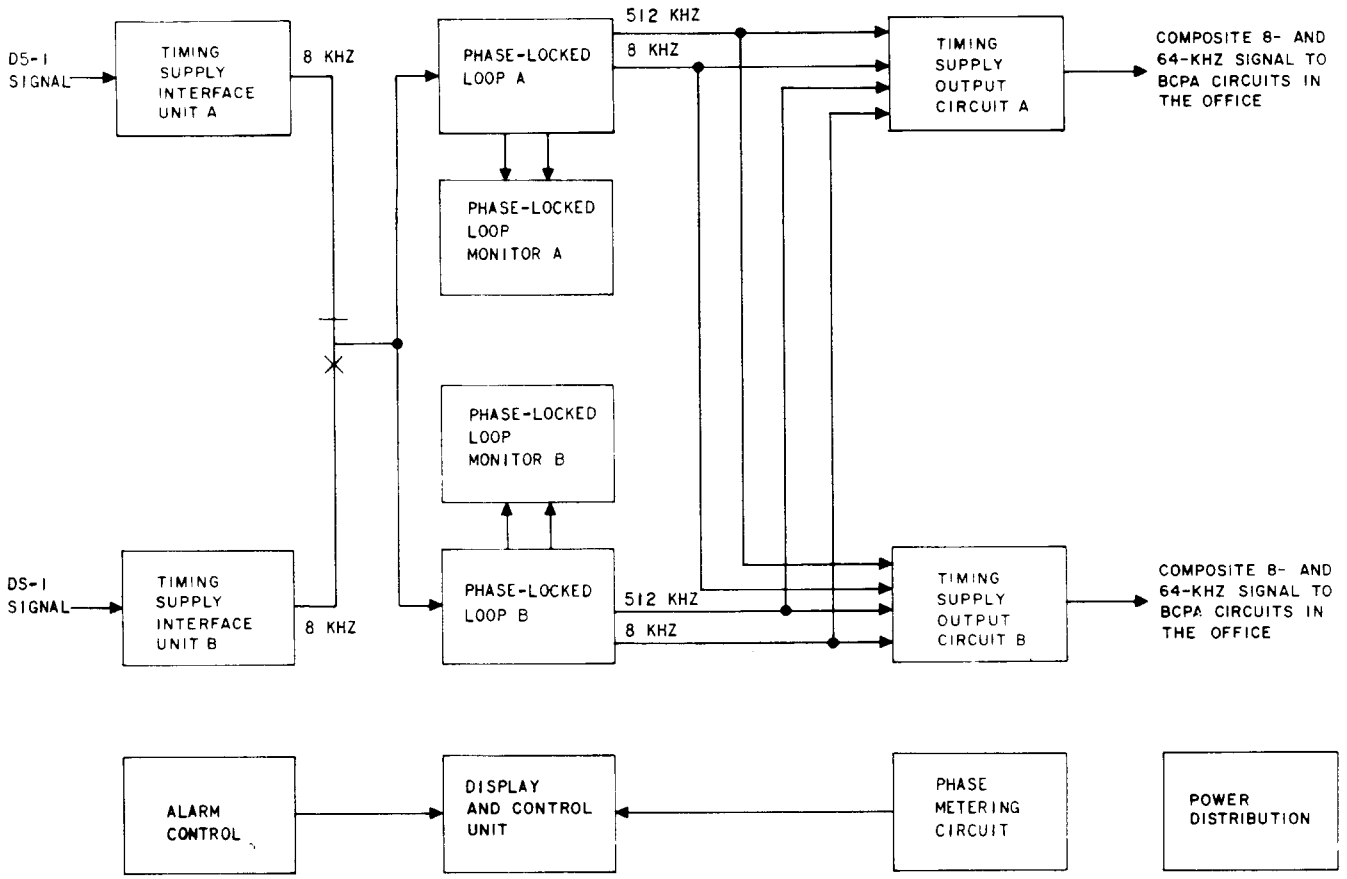

Fig. 2—Secondary Timing Supply Signal Paths—Block Diagram

TSIUs are in simultaneous operation, only one TSIU at a time supplies the 8-kHz signal to the PLLs. Therefore, if one TSIU fails, the other TSIU is automatically switched into the circuit to supply the 8-kHz signal to the PLLs. The TSIUs can be manually switched if required.

2.03 The two complete PLLs contained in the STS are locked to only one TSIU during normal operation. Each PLL contains an oscillator that locks to the incoming 8-kHz signal. The oscillator output is counted down into 512- and 8-kHz signals that are used by the timing supply output circuits (TSOCs). If the 8-kHz signals from both TSIUs become defective or vanish, the oscillators in phase-locked loop A (PLL-A) and in phase-locked loop B (PLL-B) will free-run at their natural frequency. As a result, the STS can continue to provide timing signals but with degraded precision.

2.04 The two TSOCs in the STS automatically accept signals from only one PLL at a time. If one PLL fails, the TSOCs accept signals from the other PLL. The accepted 512- and 8-kHz signals are converted into 8- and 64-kHz composite bipolar signals, which are sent to all bay clock, power, and alarms (BCPA) circuits in the office (see Section 314-916-100).

Timing Supply Interface Units

2.05 The TSIU, circuit pack (CP) HL65, receives its timing signals via the DS-1 signal, which is routed to the TSIU by the DSX-1 cross-connect (Section 365-200-110), or equivalent, before it reaches the T1DM. Each TSIU is bridged onto an incoming DS-1 line. The total connection between the DSX-1 and the T1DM on which the STS is bridged should be no more than 655 feet of ABAM or 473 feet of 750-type cable. The connection between the STS input and the T1DM must be less than 50 feet of ABAM or 750-type cable. The signal amplitude at the DSX-1 must have a pulse height of 3.0 $\pm$0.3 volts and must meet the standard

DS-1 pulse shape specifications. For maximum protection against failure, separate incoming DS-1 lines should drive the two TSIUs wherever possible. If only one DS-1 line is available for synchronization, both TSIUs should be driven by it.

2.06 Each TSIU is made up of four sections (Fig. 3): the line circuit, the framing circuit, the phase build-out circuit, and the selector circuit. The line circuit of each TSIU converts the bipolar return-to-zero DS-1 signal to a unipolar nonreturn-to-zero signal and extracts a 1.544-MHz square wave clock signal. The framing circuit takes the data and clock signals and searches for the 193rd bit (F-bit) of each frame. When the F-bit has been found, the TSIU becomes locked to this position. This position is continuously monitored for the proper F-bit code sequence and if sufficient errors are found, the searching procedure is started over. The framing circuit, therefore, divides the 1.544-MHz signal by 193 to obtain the desired 8-kHz signal used by the PLLs.

2.07 Although both TSIUs produce an 8-kHz signal, the 8-kHz signal produced by only one TSIU is supplied to both PLLs through the selector circuits. The input selector (IS) switch on the display and control unit controls the selection of the TSIU to supply the 8-kHz signal to the PLLs. The IS switch may be set in either the automatic (AUTO) or manual position. In the AUTO position, if one TSIU fails, the selector circuit on each TSIU automatically switches to supply the 8-kHz signal produced by the other TSIU to the PLLs. In the manual position (IU-A or IU-B), if one TSIU fails, the IS switch must be manually switched to cause the selector circuit to supply the 8-kHz signal produced by the other TSIU. The AUTO position is normally used for maximum protection against failure.

2.08 Since each TSIU produces an 8-kHz signal, these signals may be out of phase if the TSIUs are driven by separate DS-1 lines. A phase build-out circuit is incorporated to align the 8-kHz signal of both TSIUs in phase so that when switching occurs from one TSIU to the other, the PLLs will not see a large change in phase. Each 8-kHz signal can be phase-shifted in steps of one-twelfth of a frame by the phase build-out switch on the faceplate of each TSIU circuit pack.

2.09 The selected TSIU also provides a status lead to the PLLs and to the phase-locked

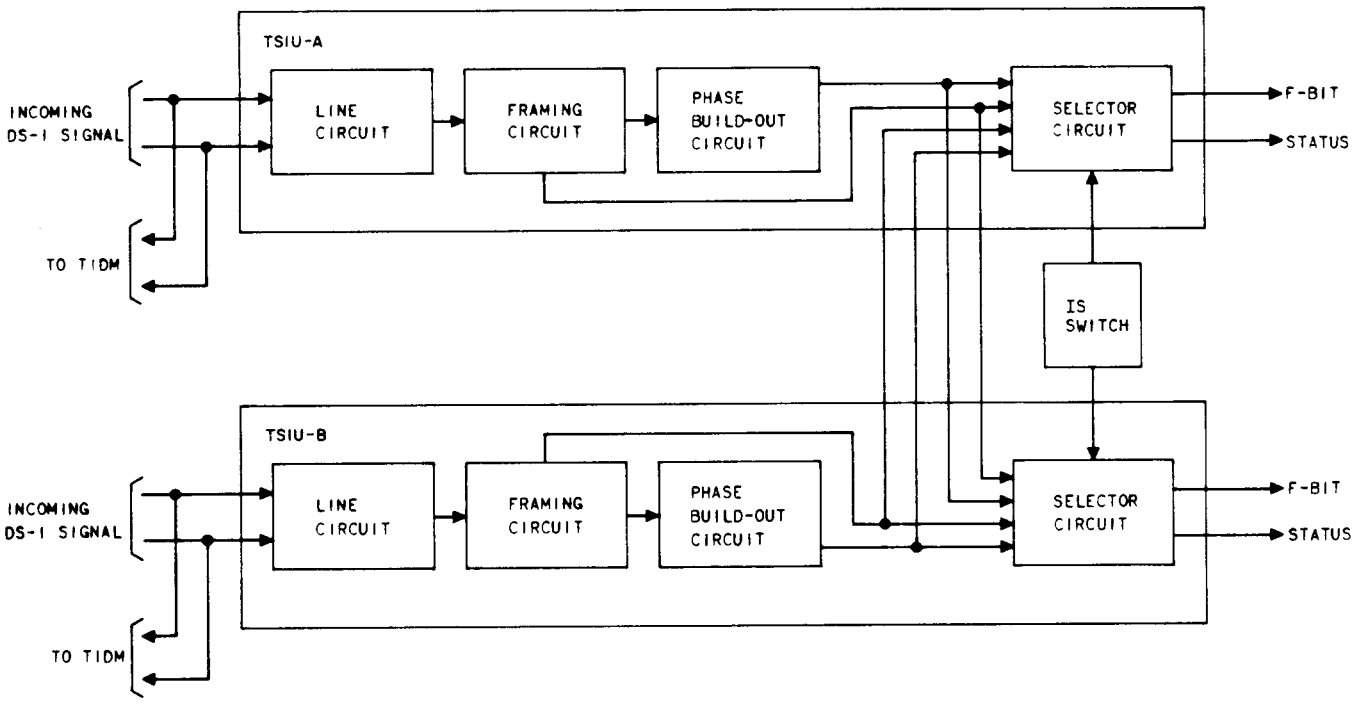

Fig. 3—Timing Supply Interface Units—Block Diagram

loop monitors (PLLMs). This status lead indicates to the PLLs and to the PLLMs whether a valid F-bit is being sent.

Phase-Locked Loops

2.10 Each PLL, CP HL53, consists of an 89A voltage-controlled oscillator (VCO), a phase comparator, a level shifter and amplifier, and a filter circuit (see Fig. 4).

2.11 The principal component of each PLL is the 89A VCO. Each VCO is a temperature-compensated unit. Its output is a 2.56-MHz signal which is sent to the divider circuit.

2.12 The divider circuit counts down the 2.56-MHz signal into the 8- and 512-kHz signals used by the TSOCs. It also provides an 8-kHz signal to the phase comparator circuit and signals of other frequencies to other circuits in the STS.

2.13 The phase comparator measures the difference in phase between the incoming 8-kHz F-bit signal and the 8-kHz reference signal from the divider circuit. Its output is a signal that is proportional to the phase difference of its two inputs. The output is sent to the level shifter and amplifier. The phase comparator also examines the status lead from the TSIU. If the status lead indicates that a valid F-bit is not being transmitted to the PLL, the F-bit is inhibited, allowing the VCO to free-run.

2.14 The level shifter and amplifier contains circuits that convert the output of the phase comparator to a 4-volt, peak-to-peak signal whose duty cycle is identical to that of the phase comparator. This signal is sent to the filter circuit.

2.15 The filter circuit converts the signal into a dc voltage proportional to the duty cycle of the incoming signal. This dc voltage is used to control the frequency of the VCO.

Phase-Locked Loop Monitor

2.16 Each PLLM, CP HL54 (MFR DISC) or CP HL54B, checks the PLL and the TSIU supplying the F-bit for malfunctions (Fig. 5). In

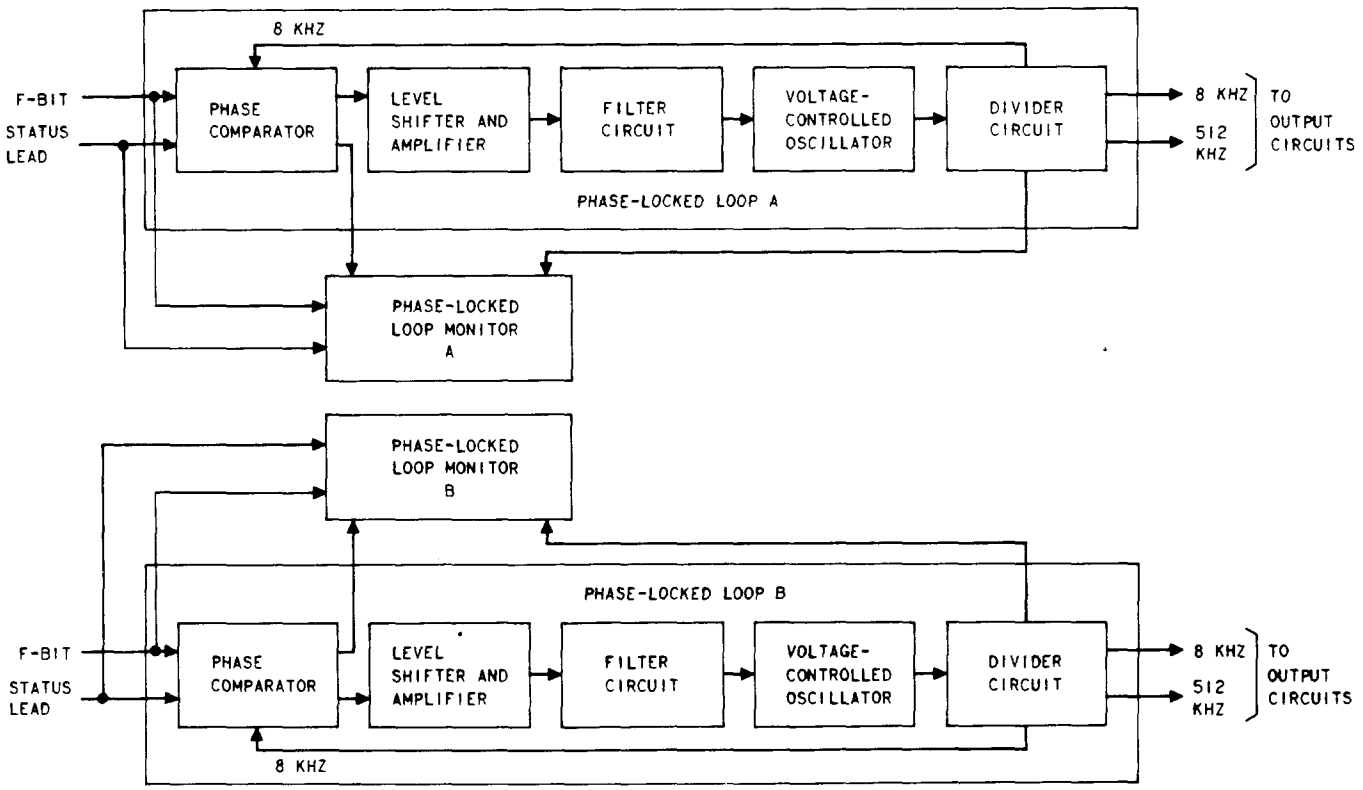

Fig. 4—Phase-Locked Loops A and B—Block Diagram

addition, the PLLM contains a reset generator which generates a reset pulse approximately every second. This pulse is used primarily to reset the alarm indications except for those alarms that must be manually reset.

2.17 The PLLM contains a slip detector and an end-of-range detector, which measure the relative phase of the 8-kHz signal supplied by the TSIU and the 8-kHz signal generated by the VCO via the divider circuit. These circuits also require a 64-kHz signal from the PLL. If the phase difference is a large positive or negative value due to the drift of the VCO, the end-of-range detector gives an end-of-range (EOR) alarm. If the phase difference changes abruptly from a large positive value to a large negative value, or vice versa, the slip detector indicates that a slip has occurred.

2.18 The miscellaneous fault detectors check circuits in the PLL and the TSIU supplying the F-bit, as well as some circuits in the PLLM, and give a malfunction (MALF) alarm.

2.19 The framing alarm delay circuit is used to check the status lead from the TSIU. When framing has been lost for approximately 4 seconds, an alarm signal is given.

Timing Supply Output Circuits

2.20 The signals from both PLLs enter the TSOCs, CP HL59, and are sent to the clock switching circuits, which make up a common flip-flop switch (Fig. 6). Although signals from both PLLs enter the TSOCs, the clock switching circuits select the signals from only one PLL by monitoring the incoming 8-kHz signal of each PLL. The selected 512- and 8-kHz signals are sent to both 64-kHz clock and 8-kHz byte sync framing circuits. If the 8-kHz signal from the selected PLL circuit is interrupted for any reason, the clock switching circuits automatically switch to the signals from the other PLL circuit and remain in this condition until the 8-kHz signal is interrupted.

2.21 The 64-kHz clock and 8-kHz byte sync framing circuit accepts the 8- and 512-kHz signals and converts them into the required 64-kHz

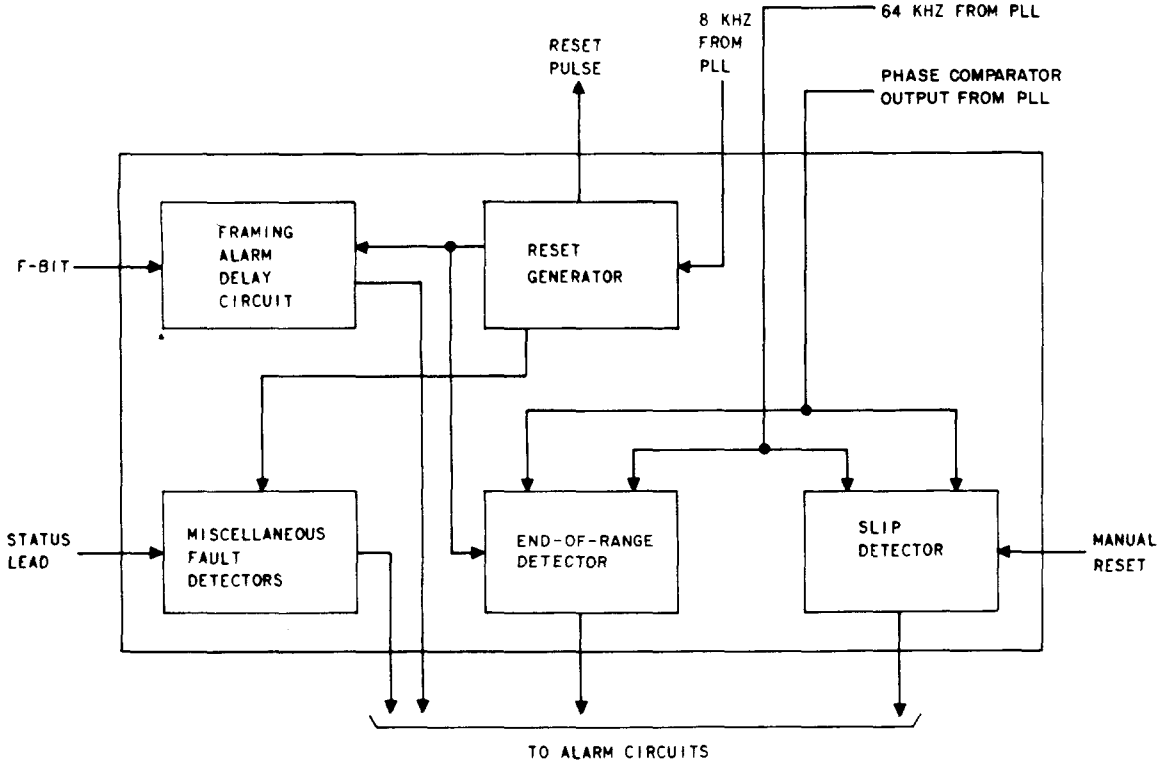

Fig. 5—Phase-Locked Loop Monitor—Block Diagram

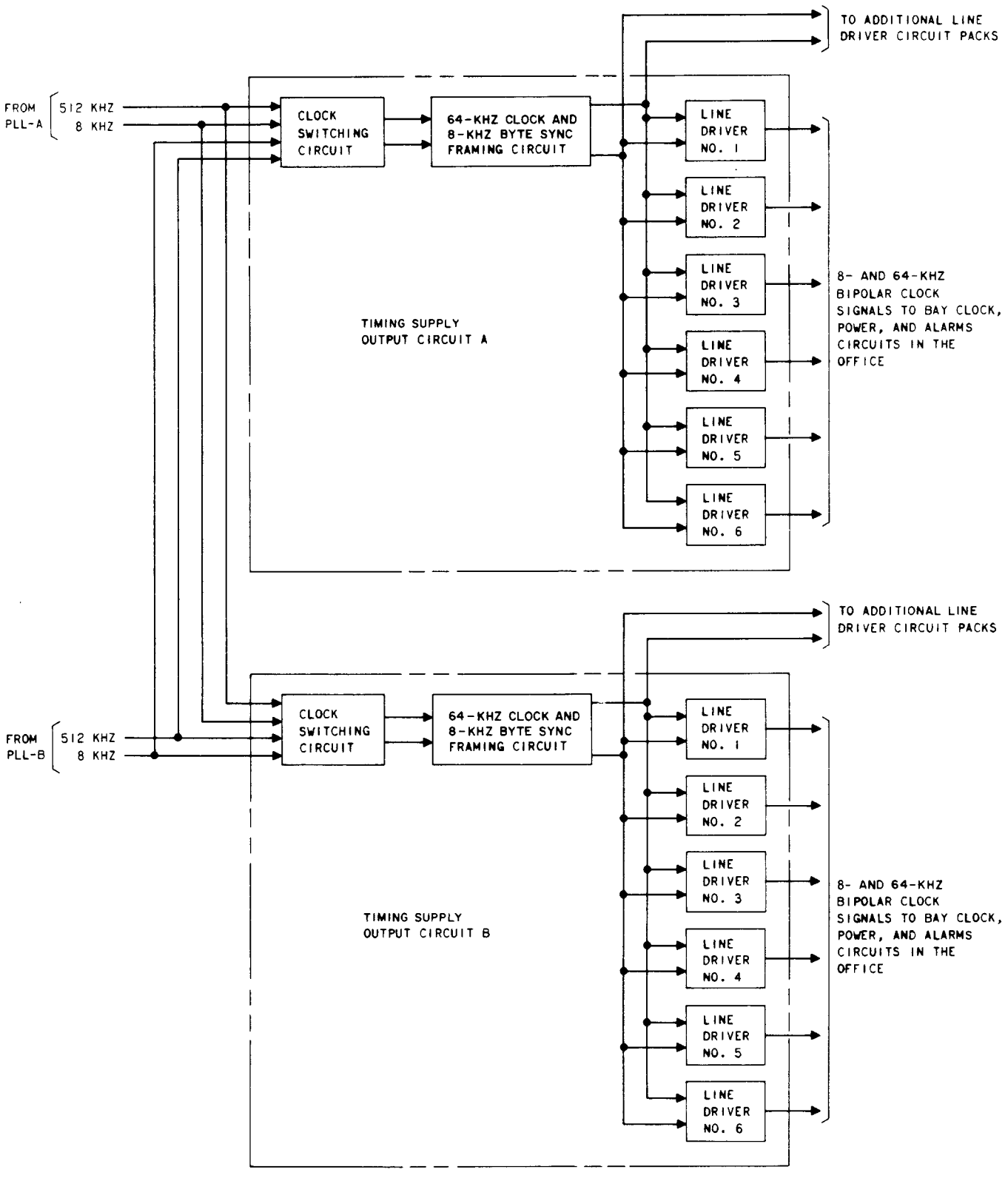

Fig. 6—Timing Supply Output Circuits—Block Diagram

bit clock and 8-kHz byte clock formats (Fig. 7A and 7B). These signals are then sent to the line driver circuits.

2.22 The 8- and 64-kHz signals are transmitted to each line via a single line driver arranged to transmit bipolar signals. Only one line driver and its associated pair of line leads are used to transmit both the 64-kHz bit clock and 8-kHz byte clock signals. This is accomplished by transmitting only the 64-kHz clock signals and causing a one-pulse violation in the bipolar signal to denote the location of the byte signal (Fig. 7C). The second of the two successive 64-kHz pulses that occur with the same polarity defines the beginning of a byte. Therefore, the first 64-kHz pulse of a byte has the same polarity as the eighth 64-kHz pulse of the previous byte. The byte signal may be easily recognized and extracted from the composite signal by the BCPA circuits in the office. The violations alternate in polarity, and therefore, the signal has no dc component.

2.23 Each TSOC contains six line drivers for distribution of the timing signal. When more timing supply line drivers (TSLDs) are needed, additional HL58 circuit packs, each containing 16 line drivers, may be installed in the STS. The timing signals from both TSOCs must be sent to the same BCPA circuit to have redundancy of operation if one TSOC fails. Therefore, when extra TSLDs are installed with one TSOC, they must also be installed with the other TSOC. Up to five pairs of HL58 circuit packs may be installed for a maximum capability of 86 pairs of timing signal lines.

Alarm Control

2.24 The timing supply alarm logic (TSAL), CP HL55, receives alarm signals from the TSIUs, PLLMs, TSOCs, and power units; and causes the appropriate major (MJ) or minor (MN) alarm to operate. In addition, it controls the lights on the display and control unit and causes office audible

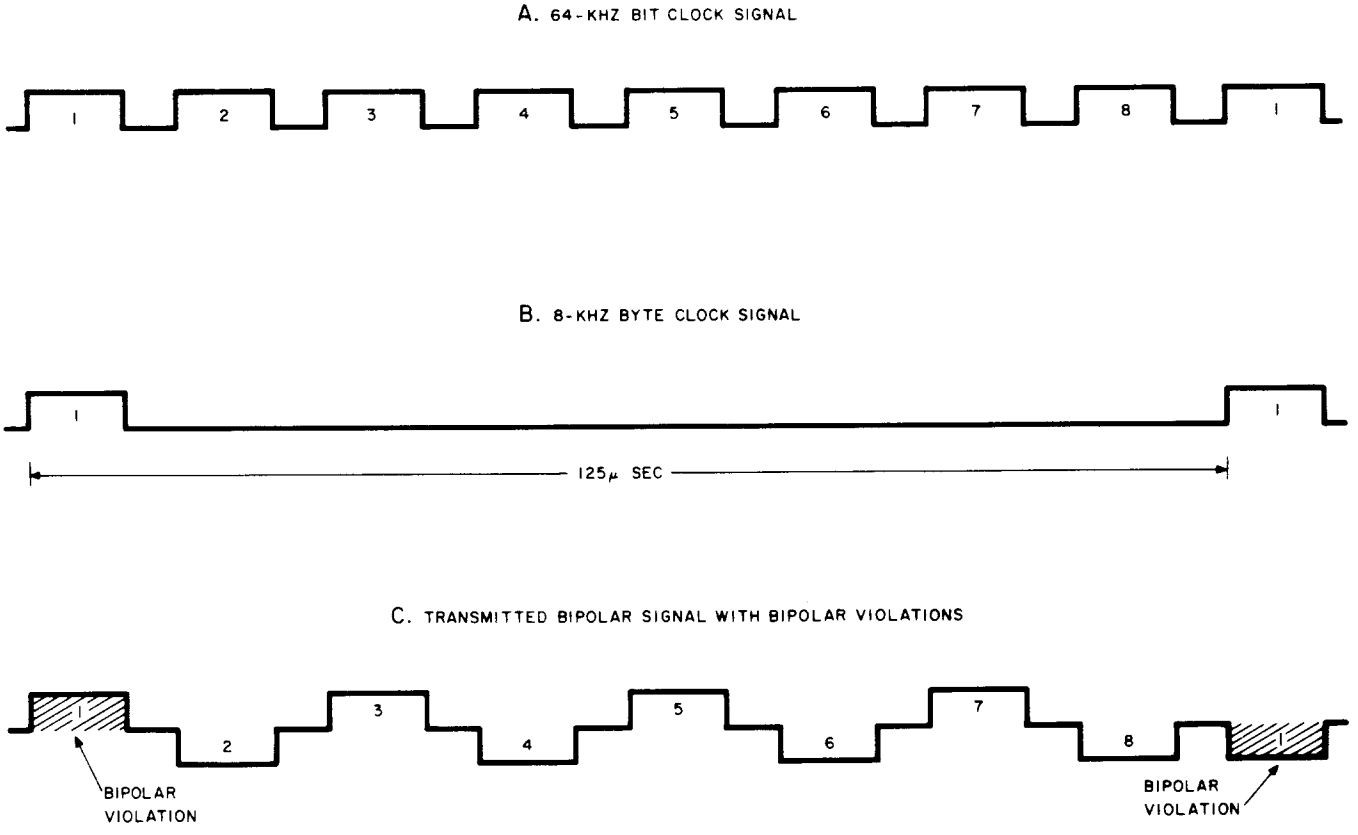

Fig. 7—Clock Waveforms of Output Circuits

and visual alarms and signals for the T Carrier Administration System to be generated.

2.25 A major alarm is given if:

(a) Each PLLM has detected slips in its associated PLL, both PLLMs have detected malfunctions, or a slip has been detected by one PLLM and a malfunction has been detected by the other PLLM.

(b) The output of each PLL is faulty.

(c) Both TSOCs are faulty.

(d) Both TSIUs cannot find framing.

A minor alarm is generated if:

(a) One TSIU cannot find framing.

(b) One PLLM or both PLLMs give an EOR indication.

(c) A slip or malfunction, or both, is detected in one PLL.

(d) The output of one PLL is faulty.

(e) One TSOC is faulty.

Display and Control Unit

2.26 The display and control unit (Fig. 8) accepts signals from various circuits in the STS and gives a visual indication of the status of the circuits. The unit contains the MJ and MN alarm lamps and the control keys for the STS, and a numeric display for use with the phase metering circuit (PMC).

2.27 The display panel markings show the three functional sections of the STS and their interconnecting signal paths. Each functional section and the signal paths contain lights that indicate the status of each section. Table A gives the designation and color of each light in the STS. A flowchart arrangement showing how to interpret the light indications is provided in Section 314-913-315.

2.28 The control keys force certain conditions to occur in the STS. The IS switch, as described in 2.07, selects the TSIU that supplies the F-bit to the PLLs. An additional set of key switches is used to control the STS when maintenance is being performed. Table B gives each key designation and function.

2.29 As discussed in 2.24, the MJ and MN alarm lamps are actuated by certain conditions of the STS.

Phase Metering Circuit

2.30 The PMC, CP HL57, measures the phase difference between any two selected 8-kHz digital signals. The measured phase is given as a number between 00 (0 degrees of phase difference) and 64 (360 degrees of phase difference). The phase difference is displayed as a decimal number on two 7-segment display units mounted on the display and control unit (Fig. 8). Measurements are taken at a rate of one a second.

2.31 The phase difference can be measured between either the positive or negative transition of one input and either the positive or negative transition of the other input. The transitions to be used are selected by switches associated with each input. The inputs to the PMC, CP HL57, are made via test points 1 (IN1) and 7 (IN2) on the faceplate of the circuit pack.

2.32 When the PMC is not in use, the numerical display on the display panel is in a blank condition. Also, when one of the inputs does not have a repetition rate of 8 kHz or is absent, a single light located next to the numerical display indicates an invalid (INV) input and the numerical display is blanked.

Power Distribution

2.33 The STS contains two power units for converting office battery to the proper regulated voltages (Fig. 9). All circuits in TSIU-A, PLL-A, PLLM-A, and TSOC-A receive +5 and −12 volts from logic power unit A. All circuits in TSIU-B, PLL-B, PLLM-B, TSOC-B, and the PMC receive +5 and −12 volts from logic power unit B.

2.34 The alarm control and most of the display and control unit lights normally obtain +5 volt power from logic power unit A; when logic power unit A fails, however, logic power unit B automatically supplies power to these circuits via a relay.

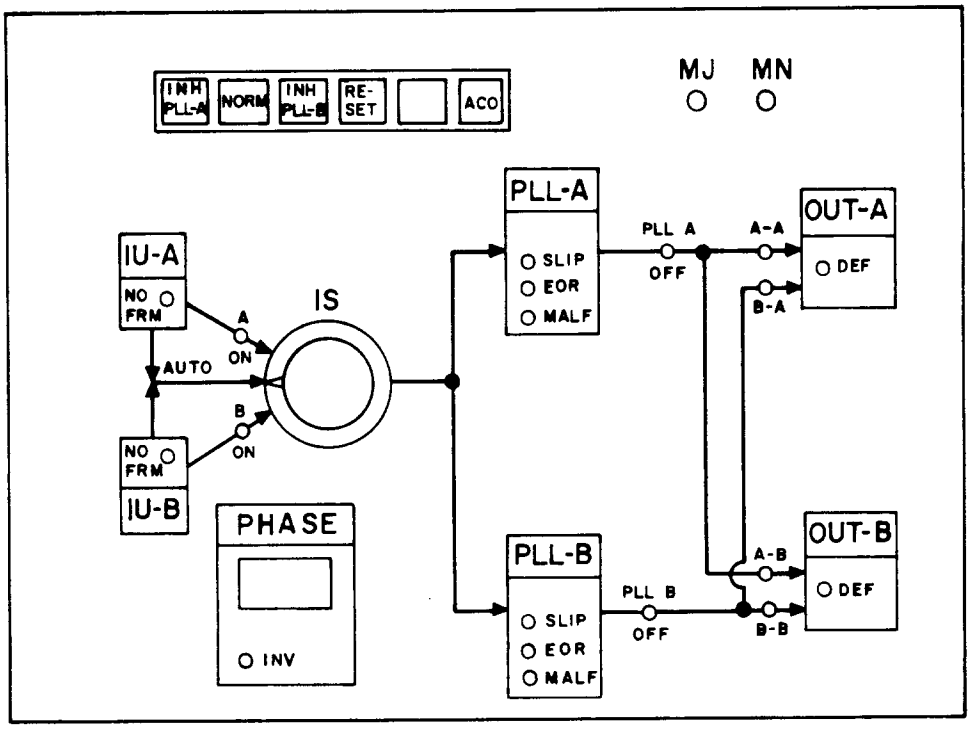

Fig. 8—Secondary Timing Supply Display and Control Unit

2.35 The office battery supplied to the power units may be −48 or −24 volts. Two 74A-type power units are required when −48 volts is used. When −24 volts is used, two 78A-type power units are required. For either office battery, two office battery lines are brought into the power units, each supplying one power unit. The two lines are coupled to the alarm relays via diodes so that the alarm circuitry remains operative if either office battery line fails.

3. EQUIPMENT DESIGN

Bay Arrangement and Markings

3.01 As stated in 1.10, the STS can be converted into an NTS. Therefore, the STS uses the same bay arrangement and wiring as the NTS.

3.02 The STS can be contained in either an 11-foot 6-inch bay or a 7-foot bay. It is arranged in a 5-shelf unit, shown in Fig. 10. The first and second shelves are used when the STS is converted to an NTS. The third shelf contains all the circuit packs for section B of the STS and for logic power unit B. Section A of the STS, the common circuit packs, and logic power unit A are contained in the fourth shelf. The fifth shelf contains the display and control unit.

3.03 Each circuit pack is labeled on the faceplate with an HL number and a functional abbreviation. Each HL number also has a certain shelf position number in the bay in which it must be installed. Table C gives the HL number, function, and shelf position number of each circuit pack in the STS.

4. REFERENCES

4.01 The following sections provide additional information. These sections may not have been issued yet; check the applicable index to determine whether they are available.

314-900-100	Digital Data System—Private Line Service—Overall Description
314-912-100	Digital Data System—T1 Data Multiplexer—Description

TABLE A

LIGHT DESIGNATION	MEANING
NO FRM	The red NO FRAMING light will light if the respective interface unit cannot lock to the incoming DS-1 signal.
A ON	This green light indicates that TSIU-A is supplying the F-bit to both PLLs.
B ON	This green light indicates that TSIU-B is supplying the F-bit to both PLLs.
EOR	The red END OF RANGE light will light when the respective VCO has drifted such that the phase error is greater than 1/4 cycle.
SLIP	This red light will light when a slip has occurred in the respective PLL.
MALF	The red MALFUNCTION light will light when a miscellaneous trouble is present in the TSIU, PLL, or PLLM.
PLL A OFF	This red light will light when the output of PLL-A has been inhibited or is defective.
PLL B OFF	This red light will light when the output of PLL-B has been inhibited or is defective.
A-A	This green light will light when PLL-A is providing timing signals to TSOC-A.
B-A	This green light will light when PLL-B is providing timing signals to TSOC-A.
A-B	This green light will light when PLL-A is providing timing signals to TSOC-B.
B-B	This green light will light when PLL-B is providing timing signals to TSOC-B.
DEF	The red DEFECTIVE light indicates that the respective TSOC is faulty.
INV	The red INVALID light indicates that one of the two inputs to the PMC is not at an 8-kHz rate or is absent.

TABLE B

KEY DESIGNATION	FUNCTION
NORM	The NORMAL key is used to release the other interlocking keys, thereby placing the STS in normal operation.
INH PLL A	The INHIBIT PLL A interlocking key forces the input to the TSOCs from PLL-A to be turned off.
INH PLL B	The INHIBIT PLL B interlocking key forces the input to the TSOCs from PLL-B to be turned off.
RESET	This key resets the slip detector on the PLLMs to a normal state.
ACO	The ALARM CUT OFF key is used to turn off the office audible alarms.

314-913-215	Digital Data System—Secondary Timing Supply—Conversion to a Nodal Timing Supply	314-913-515	Digital Data System—Secondary Timing Supply—Tests
314-913-315	Digital Data System—Secondary Timing Supply—Maintenance and Troubleshooting	314-916-100	Digital Data System—Bay Clock, Power, and Alarms Circuit—Description

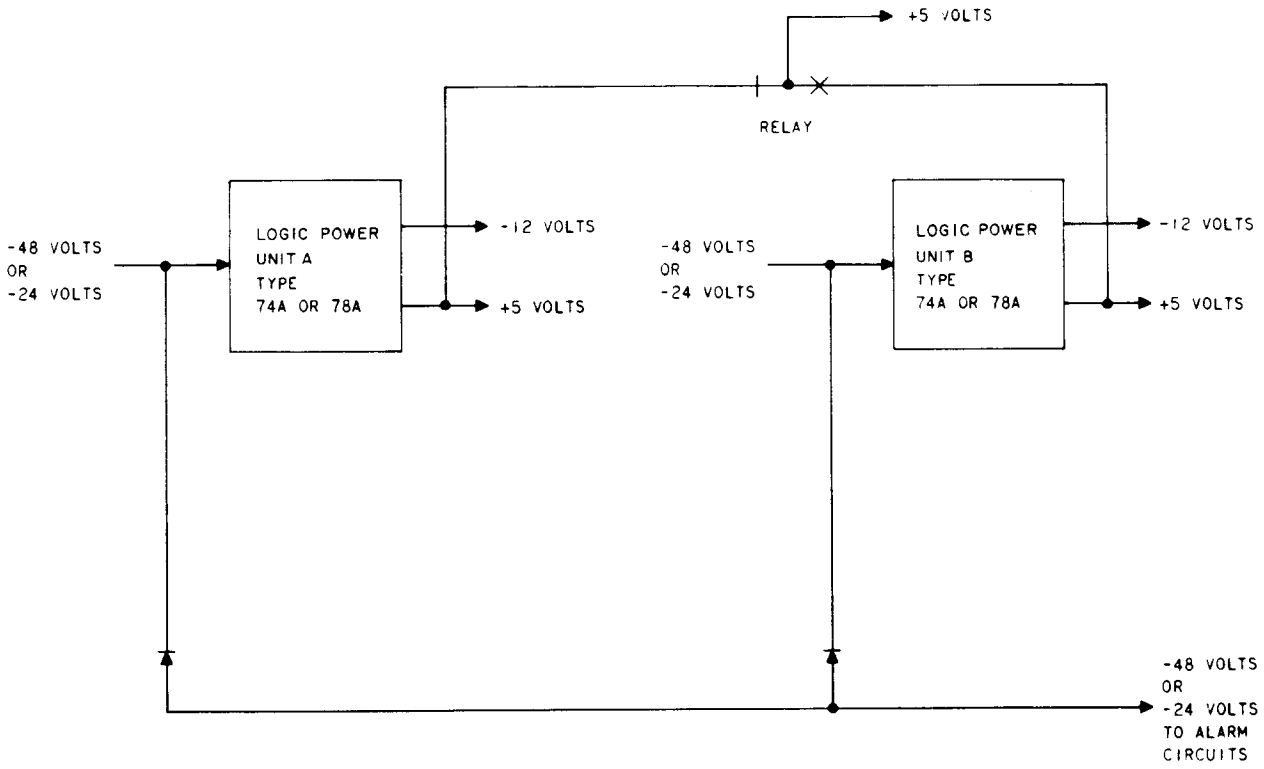

Fig. 9—Secondary Timing Supply Power Distribution

365-010-100 Fundamentals of Digital Transmission

365-200-110 DSX-1 Patch and Cross-Connect—Description

880-601-110 Digital Data Systems—Synchronization Network

4.02 Detailed schematics and circuit information are contained in the following SDs and CDs.

CD- & SD-73082-01 Digital Data System—Central Office Bay Clock, Power, and Alarms Circuit

CD- & SD-73083-01 Digital Data System—Central Office Nodal Timing Supply

SD-73087-01 Digital Data System—Station and Central Office System Interconnection and Application Schematic

CD- & SD-99503-01 DSX-1 Patch and Cross-Connect

SD-99596-01 System Block Diagram—Digital Data Service

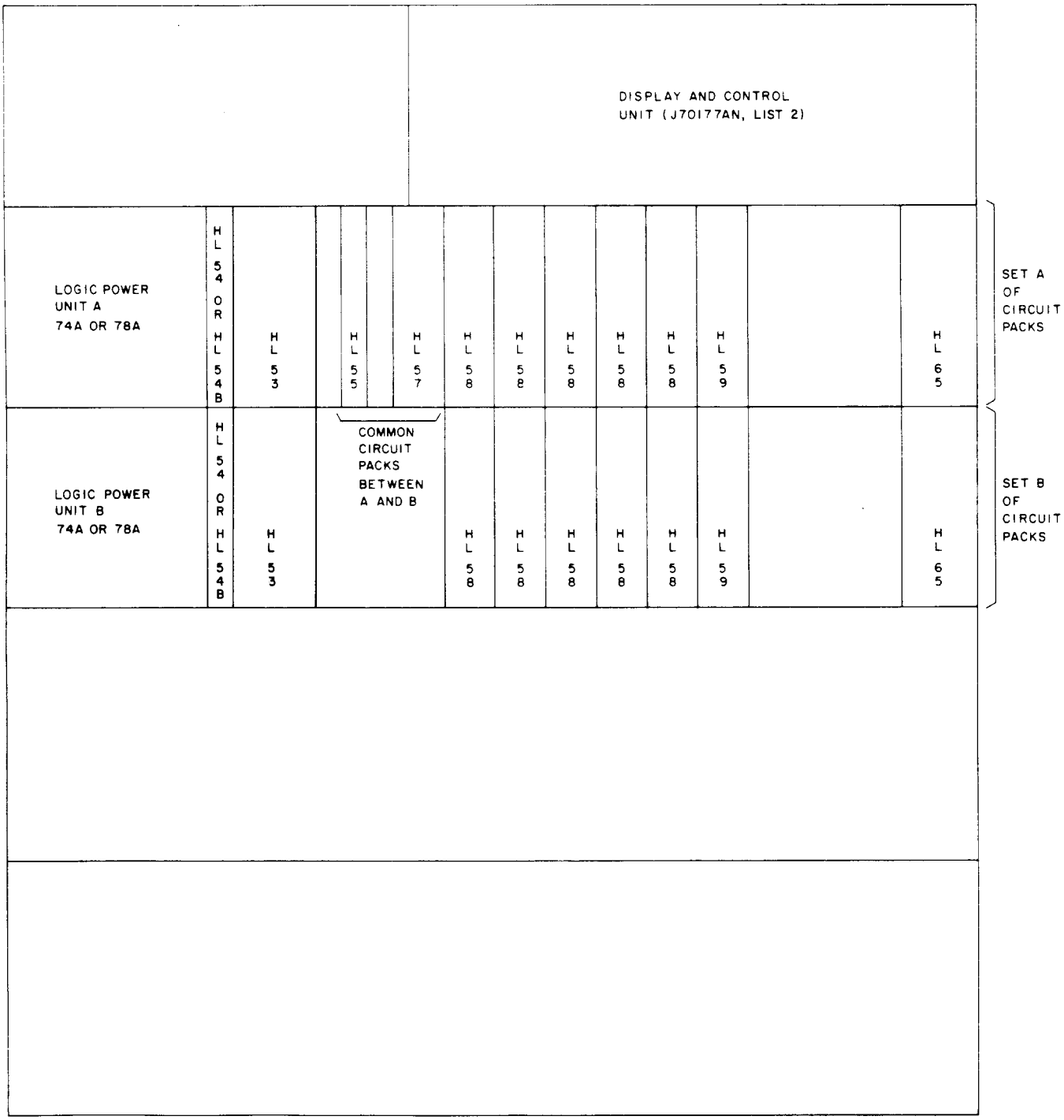

Fig. 10—Shelf Arrangement for the Secondary Timing Supply

TABLE C

HL NUMBER	FUNCTION	SHELF POSITION NUMBER	
		SET A	SET B
53	Phase-Lock Loop (PLL)	24	24
54 (MFR DISC) or 54B	Phase-Lock Loop Monitor (PLLM)	19	19
55	Timing Supply Alarm Logic (TSAL)	32	
57	Phase Metering Circuit (PMC)	36	
58	Timing Supply Line Drivers (TSLD)	39	39
58	Timing Supply Line Drivers (TSLD)	42	42
58	Timing Supply Line Drivers (TSLD)	45	45
58	Timing Supply Line Drivers (TSLD)	48	48
58	Timing Supply Line Drivers (TSLD)	51	51
59	Timing Supply Output Circuit (TSOC)	53	53
65	Timing Supply Interface Unit (TSIU)	68	68