DIGITAL DATA SYSTEM
LOCAL TIMING SUPPLY
DESCRIPTION

1. GENERAL

1.001 This addendum supplements Section 314-913-120, Issue 1. Place this pink sheet ahead of Page 1 of the section.

1.002 This addendum is issued for the following reasons:

(a) To rate the local timing supply (LTS), J70177AG, manufacture discontinued

(b) To change the legend on the bottom of Page 1

(c) To add information covering cabling distances between the DSX-1 cross-connect, LTS, and T1 data multiplexer (T1DM)

(d) To revise information covering the 64-kHz clock and 8-kHz byte sync framing circuit

(e) To change a section title and number included in the references.

2. CHANGES TO SECTION

2.001 On Page 1, add the following paragraph:

1.07.1. The LTS, J70177AG, has been rated manufacture discontinued. Future end offices will obtain timing signals from the secondary timing supply or the integrated timing supply associated with the T1WB5 data-voice multiplexer. The secondary timing supply, J70177E or J70177M, will be used in large end offices and in some hub offices. The integrated timing supply associated with the T1WB5, J70177W on J70177Y, will be used in small end and chain offices.

2.002 On the bottom of Page 1, delete the copyright notice and add the following:

NOTICE

Not for use or disclosure outside the Bell System except under written agreement.

2.003 On Page 3, revise paragraph 2.08 as follows:

2.08 The TSIU, circuit pack HL65, receives its timing signals via the DS-1 signal. The DS-1 line is routed to the TSIU by the DSX-1 cross-connect (Section 365-301-101) or equivalent. The DS-1 line is then routed from the TSIU to the T1DM. The total connection between the DSX-1 and input A of the LTS should be no longer than 655 feet of ABAM cable or 473 feet of 750-type cable. The total connection between the DSX-1 and the inputs to the T1DM to which input B of the LTS is connected should be no longer than 655 feet of ABAM cable, or 473 feet of 750-type cable. The connection between input B of the LTS and the T1DM must be less than 50 feet of ABAM or 750-type cable. The signal amplitude at the DSX-1 must have a pulse height of 3.0 ±0.3 volts and must meet the standard DS-1 pulse shape specifications. For maximum protection against failure, separate incoming DS-1 lines should drive two TSIUs when possible. If only one DS-1 line is available for synchronization, then both TSIUs should be driven by it.

2.004 On Page 7, revise paragraphs 2.23 and 2.24 as follows:

2.23 The signals from both PLLs enter the TSOCs, CP HL59, and are sent to the clock switching circuits which make up a common flip-flop switch (Fig. 6). Although signals from both PLLs enter the TSOCs, the clock switching circuits select the signals from only one PLL by monitoring the

incoming 8-kHz signal of each PLL. The selected 8- and 512-kHz signals are sent to both the 64-kHz clock and 8-kHz byte sync framing circuits. If the 8-kHz signal from the selected PLL circuit is interrupted for any reason, the clock switching circuits automatically switch to the signals from the other PLL circuit, which then remains in that condition until the 8-kHz signal is interrupted.

2.24 The 64-kHz clock and 8-kHz byte sync framing circuit accepts the 8- and 512-kHz signals and converts them into the required 64-kHz bit clock and 8-kHz byte clock formats (Fig. 7A and 7B). These signals are then sent to the line driver circuits.

2.005 On Page 10, Fig. 6, change the blocks labeled 8-KHZ AND 64-KHZ BYTE SYNC FRAMING CIRCUIT to 64-kHz CLOCK AND 8-KHZ BYTE SYNC FRAMING CIRCUIT.

2.006 On Page 20, paragraph 4.01, change 365-200-110 to 365-301-101 DSX-1, DSX-1C, and DSX-2 Patch and Cross-Connect—General Description.