SYNCHRONIZATION DISTRIBUTION EXPANDER INSTALLATION AND MAINTENANCE PROCEDURES

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1. GENERAL

1.01 This practice describes the test requirements associated with the installation, provisioning, and maintenance of the J98726W-1, J98726W-2, and J98726Y-1 SDE (Synchronization Distribution Expander). Broad schematic coverage is given in application schematic SD-7C389-01 and in SD-7C389-02. The plug-in equipment is coded AHG1, AHG2, AHG2B, AHG3, AHG4, AHG5, AHG10, AHG15, AHG25, and AHG26.

1.02 This practice is being reissued to reflect design and operational improvements. The major changes are as follows:

- The AHG5 TD has been added.
- The AHG15 TI has been added.
- The J98726Y-1 panel has been added.
- The AHG25 TD has been added.
- The AHG26 TD has been added.

Since this is a general revision, revision arrows are not used.

1.03 The SDE provides timing signals to network elements requiring a CC (composite clock) timing signal, (e.g., DDS [digital data system], D3, D4, D5, and/or SLC®-96 carrier. The SDE may also supply all-ones DS-1 signals with either D4 or ESF framing formats to network elements.

1.04 The SDE is also capable of providing analog timing signals including 512 kHz or 64 kHz for synchronizing the PFS (Primary Frequency Supply) (PFS-2B J68857AC or PFS-2 J68857M). The SDE may also supply a 2.048 MHz sine wave input for network elements requiring BSRF (basic system reference frequency) type inputs.

1.05 The SDE operates from diverse timing inputs including DS-1, DS-1C, or composite clock. The SDE capable of directly bridging onto working DS-1 or DS-1C facilities.

1.06 The SDE may distribute up to 40 CC or DS-1 (framed, all-ones) output signals. Additional single SDE outputs include 2.048 MHz, 512 KHz, or 64 KHz sine waves.

1.07 The output capacity of an SDE installation may be increased by using either distributed or concentrated timing arrangements. Distributed timing arrangements require a master SDE to recover timing from a high stability input source and serve as the office timing master. Other SDE shelves, slaved from the office timing master, are then distributed throughout the office and located where the timing is needed. The benefits of distributed timing are low cabling costs (only two input pairs per distributed panel), reduction of office interference (output cables may be much shorter), flexible growth, and low additional system costs (the low cost AHG10 TI was designed to be used in distributed panels).

1.08 Concentrated timing arrangements allow the direct expansion of a single SDE shelf. The concentrated configuration provides a large number of outputs from a common, physical location. Backplane signals from the existing or "main" shelf are carried via cables to physically close additional or "auxiliary shelve(s)". Though the auxiliary shelves act as an extension of the main shelf, they are separately powered and alarmed.

1.09 The SDE is assembled in a D4 channel bank-type shelf which will mount on a standard 23-inch, duct-type bay and requires a minimum of 10 inches of vertical space.

1.10 Additional information pertaining to the SDE and the available circuit packs may be found in AT&T Practice 314-913-220.

1.11 When the SDE is operating properly, the following indications are provided:

- All lamps on the fuse and alarm panel (F & A Panel) are extinguished.
- Pressing the MEM button extinguishes all LEDs on the AHG1 TA.
- Only a single IN SCE LED shall be lighted on either TI.

- Each TD will have a single lighted TI ( ) OUTPUT IN USE LED.

2. APPARATUS

2.01 Equipment required to perform the installation and maintenance tests includes the following:

- Digital multimeter
- Dual-trace oscilloscope with differential input capability
- A 133 and 100 ohm resistor termination - 133 and 100 ohm termination mini-clip EA end or slip-on
- R-4987 antistatic wrist strap (or equivalent)
- A KS-21838 extractor tool for white option plugs or a long-nose pliers
- A frequency counter able to measure to 4.096 MHz with input impedance of 1 Meg-ohm
- Cords as required.

3. INSTALLATION OF SDE PANEL

A. Description

3.01 The SDE is attached to the equipment bay using brackets on either side of the shelf. These brackets are reversible and allow both front and rear mounting without any additional hardware. This arrangement is shown in Fig. 1.

3.02 The -48 volt battery is cabled to TS 1 located at the rear of the Fuse & Alarm panel. Provision is made for three separate -48 volt battery feeds (-48 A, -48 B, and -48 ABS). Since the SDE is capable of operating with a single blown fuse or damaged power feed, these feeds should be kept separate and individually fused to ensure true power redundancy.

3.03 Input signals are cabled to TS 2 located at the rear of the SDE beside the Fuse & Alarm panel. There is provision for two input signals, one per TI circuit pack. The DS-1, DS-1C, CC, inputs must be cabled with 22BF or equivalent cable. All unshielded wire at TS 2 should be kept as short as possible. Pig-tail shield wires should also be kept short.

3.04 Alarm output connections are cabled to backplane "E" terminals located at the rear of the SDE, beside the Fuse & Alarm panel. These alarm output connections are from dry relay contacts which present a shunt during alarmed conditions. Multiple alarm options are available for combining the alarms of a main-auxiliary SDE configuration. Multiple alarm information is presented in T-7C389-33 Issue 6 or higher.

3.05 The TD backplane connector pins are wired to the two center terminal blocks above the SDE panel. The connectors for TDs 1 and 2 go to the SDE A terminal strip; those for TDs 3 and 4 go to SDE B. Terminal access is thereby provided for the 40 separate clock outputs. Terminal blocks BK A and BK B provide terminals for terminating a maximum of 80 shielded pairs for delivering timing signals to D-type channel banks. Cross-connections between the SDE and BK terminal blocks provide the means of assigning CC output ports to bays as required. A direct-connection option is also available that allows output tap cabling directly to the SDE A and SDE B terminal blocks.

3.06 The SDE shelf assembly is installed and wired by the AT&T Technologies installation forces or the local central office installation group. The plug-in units are installed after the wiring and cabling is completed. The plug-in units should be installed as shown in Fig. 2, 3, and 4.

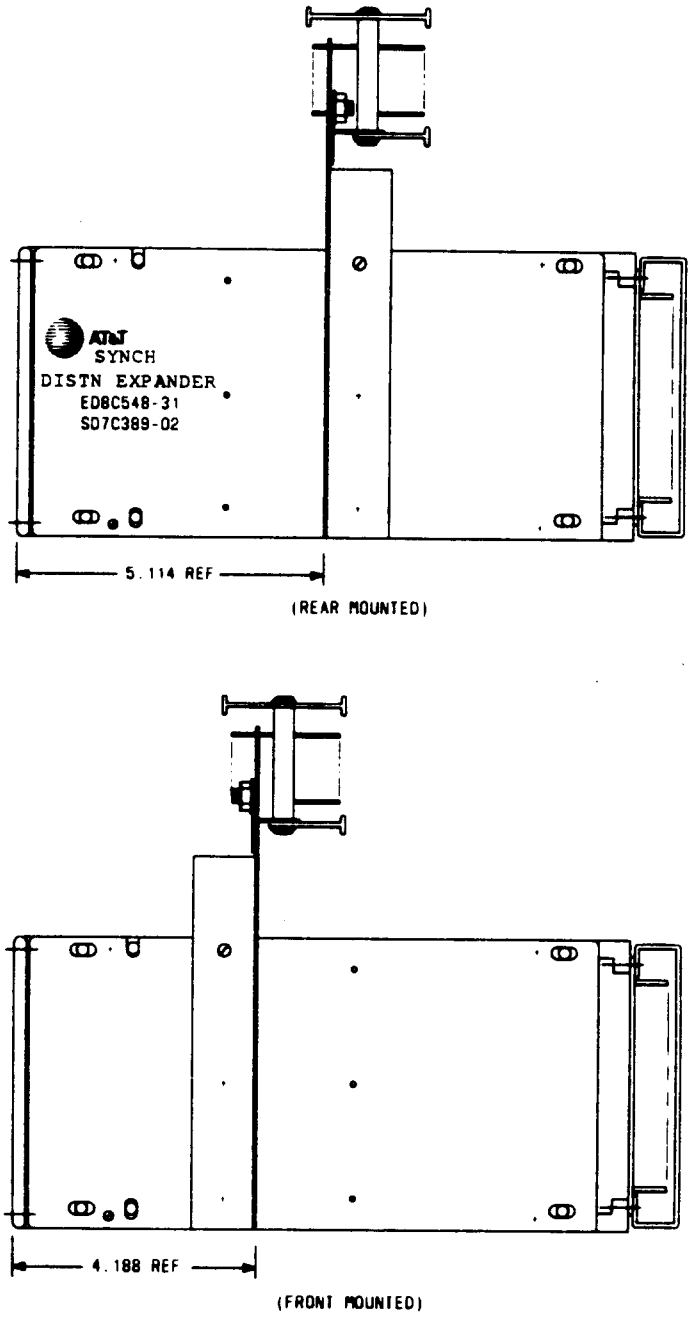


Fig. 1 - Bracket Location for Front and Rear Mounting of SDE

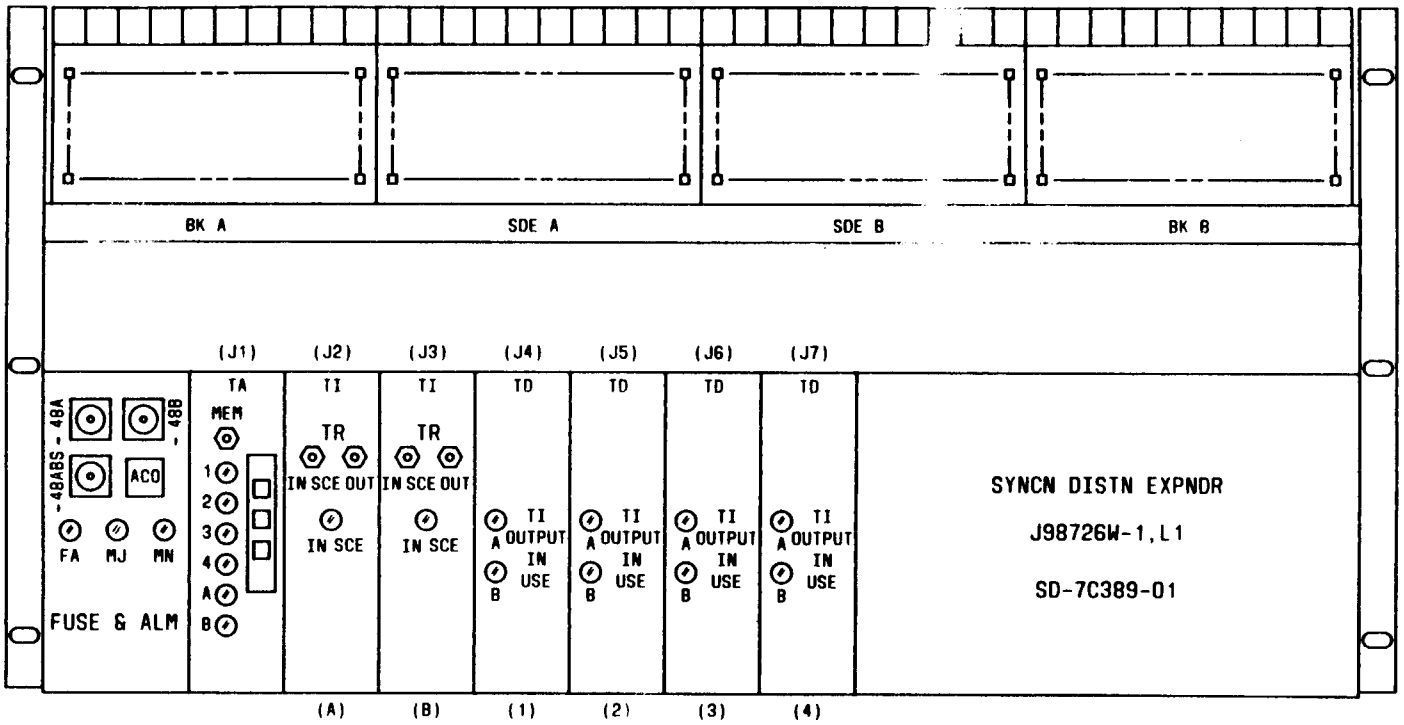


Fig. 2 - Front View of Synchronization Distribution Expander (J98726W-1)

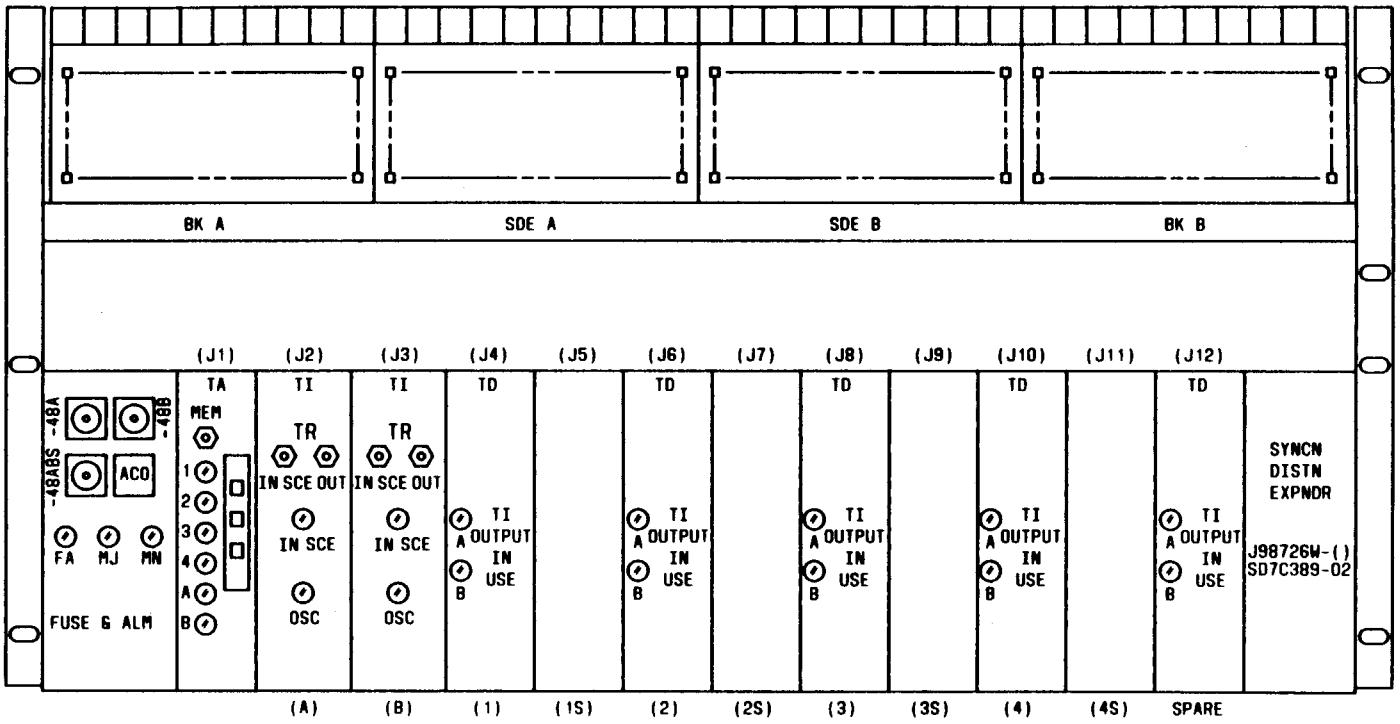


Fig. 3 - Front View of Synchronization Distribution Expander (J98726W-2)

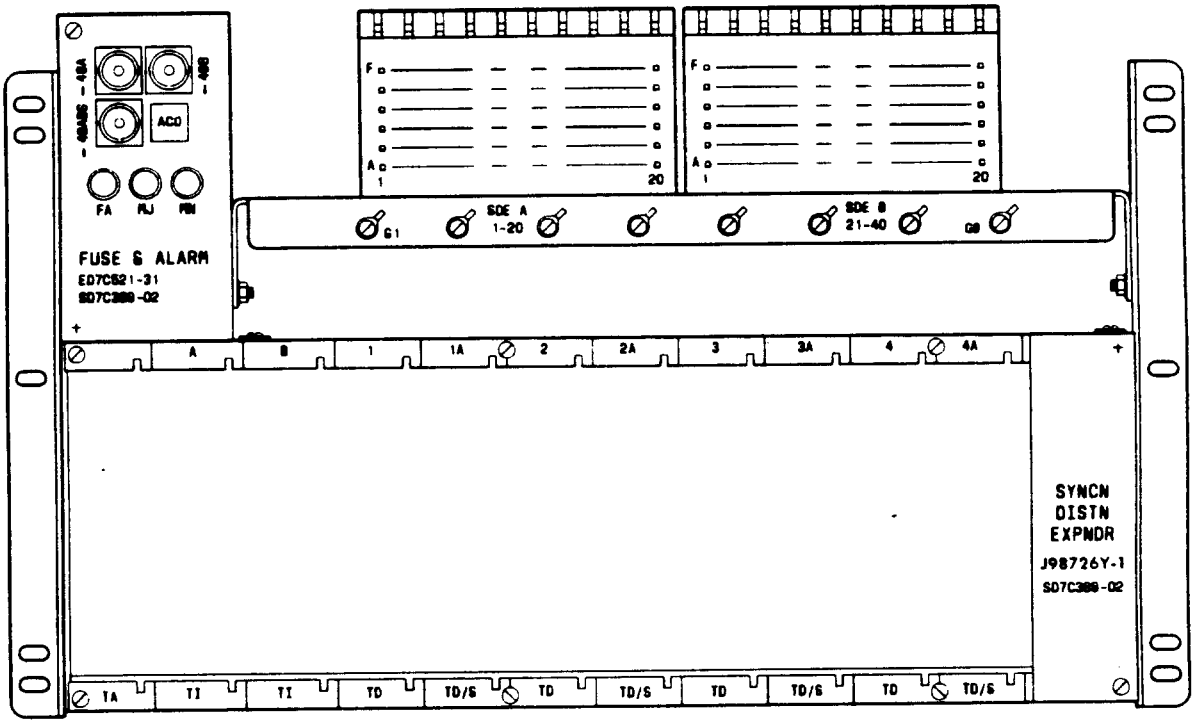


Fig. 4 - Front View of Synchronization Distribution Expander (J98726Y-1)

4. PROVISIONING AND OPERATION PROCEDURES

4.01 The provisioning and operation procedures include the following:

- Verifying fusing, powering, and alarming
- Verifying continuity
- Verifying input and output signals
- Replacing circuit packs
- Expanding output capability using AHG2B TI auxiliary panel
- Increasing output capability using AHG10/15 TI auxiliary panel expansion.

Verifying Fusing, Powering, and Alarming

4.02 Chart 1 gives the procedures for verifying fusing and powering. This procedure assumes that either an ED-7C521-30, G1,A, B, C or an ED-7C521-31, G2 is equipped.

Verifying Continuity

4.03 Chart 2 gives the procedures for verifying continuity of input source connections. When fed from bridging repeaters, each DS-1 or DS-1C input should come from two separate repeater shelves. One powered from the -48V A battery and the other from the -48V B battery. Another power feed option is to use a single shelf with split power capability to achieve the same configuration. Dual-power feeding will serve to preserve the SDE's input redundancy protection.

Verifying Input and Output Signals

4.04 Chart 3 gives the procedures for verifying input and output signals. The input signal waveforms that will be observed may either be two CC timing signals, two framed DS-1 timing signals, two framed DS-1C timing signals, or a framed DS-1 and framed DS-1C timing signal. As the SDE is intended for use as a high quality distribution of timing signals, it is suggested that input signals meet a minimum of Stratum III (4.6 PPM) accuracy.

4.05 The SDE's input and output signals will vary from those shown in the waveform figures due to cable length and parasitic capacitance.

Replacing Circuit Packs

4.06 Chart 4 contains information for the in-service replacement of all SDE circuit packs. The circuit packs covered in this information include: AHG1, AHG2, AHG2B, AHG3, AHG4, AHG5, AHG10, AHG15, AHG25, and AHG26. Instructions for the PCS (Parallel Change-Over System) are also presented in Chart 4.

Auxiliary Panel Expansion Using the AHG2B TI

4.07 Chart 5 contains information for the increase of output capacity using the AHG2B TI auxiliary panel expansion option.

Auxiliary Panel Expansion Using the AHG10 or AHG15 TI

4.08 Chart 6 contains information for auxiliary panel expansion using the AHG10 or AHG15 TI.

SDE Maintenance and Troubleshooting

4.09 Chart 7 contains information for checking the operation of an in service SDE. Input, output, and backplane signals are evaluated to determine the source of any operation problems.

5. PROCEDURES

5.01 The following charts provide installation and maintenance information.

A. CHART 1 — VERIFYING FUSING, POWERING, and ALARMING

STEP	PROCEDURE
	CAUTION: Do not install any circuit packs until directed to do so.
	Note: This test assumes that an ED-7C521-30, G1, A, B, C is equipped. If an ED-7C521-31, G2 is equipped, proceed to Step 18.
1	Verify that the TS 1 terminals 2, 4, and 6 on the SDE panel are free from ground before installing the 1-1/3 ampere office feeder fuses associated with the SDE.
2	Remove the -48 (F2), -48B (F3), and the -48ABS (F1) fuses from their fuse holders at the front of the panel.
3	Install the 1-1/3 ampere office feeder fuses. ***Requirement:*** Audible alarms sound.
4	If the ACO lamp is not lighted, depress the ACO switch. ***Requirement:*** Audible alarm is cut off. The ACO switch lights.
5	Using the VOM (volt-ohm-milliammeter), verify that -48 volts exists at TS 1 between terminals 1 and 2, 3 and 4, and 5 and 6. (Terminals 1, 3, and 5 are GRD.)
6	Reinstall the -48A (F2) and -48ABS (F1) fuses. ***Requirement:*** The MN and MJ lamps will light and remain on.
7	Insert a blown fuse into the -48B (F3) fuse holder. ***Requirement:*** The FA (K1) relay will operate and the FA lamp will light.
8	Remove the blown fuse from the -48B (F3) fuse holder and reinstall the -48B (F3) fuse. ***Requirement:*** The FA (K1) relay will release and the FA lamp will extinguish.
9	Remove the -48A (F2) fuse and install the blown fuse into the -48A (F2) fuse holder. ***Requirement:*** The FA (K1) relay will operate and the FA lamp will light.
10	Remove the blown fuse from the -48A (F2) fuse holder and reinstall the -48A (F2) fuse. ***Requirement:*** The FA (K1) relay releases and the FA lamp extinguishes.

STEP	PROCEDURE
11	Remove the -48ABS (F1) fuse and install the blown fuse into the -48ABS fuse holder. ***Requirement:*** The FA relay (K1) operates, the FA lamp lights, the MN and MJ lamps extinguish.
12	Remove the blown fuse from the -48ABS (F1) fuse holder and reinstall the -48ABS (F1) fuse. ***Requirement:*** The FA (K1) relay operates, the FA lamp extinguishes, and the MN and MJ lamps light.
13	Depress the ACO switch. ***Requirement:*** Audible alarms are enabled and the ACO lamp extinguishes.
14	With the VOM on the RX1 scale, verify that a short exists between the following terminals on TS 3: • TS 3 3 and 4 • TS 3 5 and 6 • TS 3 7 and 8 • TS 3 9 and 10 • TS 3 11 and 12 • TS 3 13 and 14
15	Depress the ACO switch. ***Requirement:*** An open exists at TS 3, between terminals 3 and 4 and terminals 9 and 10. The ACO lamp will light.
16	Depress the ACO button. ***Requirement:*** The ACO lamp extinguishes.
17	Apply a short between terminals 1 and 2 of TS 3. ***Requirement:*** Open exists between terminals 3 and 4, and 9 and 10 of TS 3. ***Note:*** This is the end of verifying fusing and power for the ED-7C521-30, G1, A, B, C. The verification for ED-7C521-31, G2 begins at Step 18.
18	Verify that the TS 1 terminals 2, 4, and 6 on the SDE panel are free from ground before installing the 1-1/3 ampere office feeder fuses associated with the SDE.
19	Remove the -48A (F2), -48B (F3), and the -48 ABS (F1) fuses from their fuse holders at the front

STEP	PROCEDURE
	of the panel.
20	Install the 1 1/3 ampere office feeder fuses.
	Requirement: Audible alarms sound and the FA lamp is lighted.
21	If the ACO lamp is not lighted, depress the ACO switch.
	Requirement: Audible alarm is cut off.
22	Using the VOM (volt-ohm-milliammeter), verify that -48 volts exists at TS 1 between terminals 1 and 2, 3 and 4, and 5 and 6. (Terminals 1, 3, and 5 are GRD.)
23	Reinstall the -48A (F2), -48B (F3) and -48ABS (F1) fuses.
	Requirement: The MN and MJ lamps will light and remain on. The FA lamp will extinguish.
24	Remove the -48A (F2) fuse.
	Requirement: The MN, MJ, and FA lamps will light and remain on.
25	Replace the -48A (F2) fuse.
	Requirement: Only the MN and MJ lamps will be lighted.
26	Remove the -48B (F3) fuse.
	Requirement: The MN, MJ, and FA lamps will light and remain on.
27	Replace the -48B (F3) fuse.
	Requirement: Only the MN and MJ lamps will be lighted.
28	Remove the -48ABS (F1) fuse.
	Requirement: Only the FA lamp will be lighted.
29	Replace the -48ABS (F3) fuse.
	Requirement: The MN and MJ lamps will light and remain on.
30	Depress the ACO switch to extinguish the ACO lamp.
	Requirement: The audible alarm is enabled.

STEP	PROCEDURE
31	With the VOM on the RX1 scale, verify that a short exists between the following pairs of backplane E terminals. • E3 and E4 • E5 and E6 • E7 and E8 • E9 and E10 • E11 and E12 • E13 and E14.
32	Depress the ACO switch to light the ACO lamp. ***Requirement:*** An open exists between backplane E terminals: E3-E4 and E9-E10. A short exists between backplane terminals E5-E6, E7-E8, E11-E12, and E13-E14.
33	Depress the ACO switch. ***Requirement:*** The ACO lamp will extinguish.
34	Apply a short between the backplane E terminals E1 and E2. ***Requirement:*** An open exists between the backplane E terminals E3-E4 and E9-E10.

B. CHART 2 — VERIFYING CONTINUITY

STEP	PROCEDURE
1	Check all leads that are run by the installer for continuity.
	CC Timing Input Source
2	Verify that the clock A and B timing sources are connected to TS 2 as follows: • Clock A [L( )X] TS 2 1 • Clock A [L( )Y] TS 2 2 • Shield A TS 2 3 • Clock B [L( )X] TS 2 6 * • Clock B [L( )Y] TS 2 7 * • Shield B TS 2 8 * — The AHG2B TI requires a reversal of the tip and ring on only one of the CC inputs to ensure hitless output switching.
	Synchronized DS-1 or DS-1C Timing Source
3	Verify that the DS-1 or DS-1C, A and B timing sources are connected to TS 2 as follows: • DS ( ) T TS 2 4 • DS ( ) R TS 2 5 • Shield TS 2 3 • DS ( ) T TS 2 9 • DS ( ) R TS 2 10 • Shield TS 2 8

C. CHART 3 — VERIFYING INPUT AND OUTPUT SIGNALS

STEP	PROCEDURE

Note 1: The following steps assume that at least one TD will be equipped in the SDE unit under test. If one TD is used it shall be located in TD-1 position.

Note 2: DS-1 output measurements must be taken across a 100 ohm terminating resistor. Input measurements also require a 100 ohm resistor unless the corresponding TI is present.

Note 3: DS-1C input measurements must be taken across a 100 ohm terminating resistor unless the corresponding TI is present.

Note 4: CC output measurements must be taken across a 133 ohm terminating resistor. Input measurements also require a 100 ohm resistor unless the corresponding TI is present.

Note 5: The 64 kHz or 512 kHz output measurements must be taken across a 133 ohm terminating resistor.

Input Signal Measurements

Note: The following steps will verify the input signals to the following TI circuit packs. AHG2, AHG2B, AHG10, and AHG15.

1 Set up a dual-trace oscilloscope for differential measurements with Channel 2 added and inverted using an internal trigger.

- Set Channels 1 and 2 to 2V/DIV (DS-1/1C norm) or 5V/DIV (CC) or
- Channel 2 invert
- Set the time base to .5 μs/DIV (DS-1) or .5 μs/DIV (DS-1C) or 20 μs/DIV (CC).

2 Connect the probes of the dual-channel oscilloscope across the input points of TS 2, ensuring that the measurement is being taken across the appropriate terminating resistor (see Chart 3 notes). Connect ground leads of the probes to frame ground.

Requirement: If the input waveform is a CC signal, the waveform will match one of the waveforms shown in Figs. 5A, 5B, 5C, or 5D. If the input waveform is a DS-1 signal, the waveform will match either Fig. 6A or 6B. If the input waveform is a DS-1C signal, the waveform will match either Fig. 7A or 7B.

3 Remove termination.

Optional Backplane Wiring

Note: Depending on the intended TD circuit packs and SDE shelf type, additional backplane wiring may be necessary. This backplane wiring carries either control information to the TD (as in

STEP	PROCEDURE

the cut off option) or provides connection to output signals (as in the 512/64 kHz and 2.048 MHz sine wave outputs). Those TD circuit packs which may require additional backplane wiring are: AHG4, AHG5/25, and the AHG26.

4 If an AHG4 TD is to be installed it will be assigned to TD-4 slot. Control wiring to this slot is presented in Table A.

Note: This wiring will be installed only for the J98726W-1 and J98726W-2 shelf assemblies.

5 Install one of the two AHG4 TD output wiring options. These options select either the attenuated output level (-23 dBm or -54 dBm) or the nonattenuated level (+10 dBm). Output wiring is presented in Table B.

Note: This wiring will be installed only for the J98726W-1, J98726W-2, and the J98726Y-1.

6 If an AHG5/25 TD is to be installed it may be assigned to any TD slot. Control wiring to this slot is presented in Table C.

Note: This wiring will be installed only for the J98726W-1 and J98726W-2 shelf assemblies.

7 If an AHG26 TD is to be installed it may be assigned to either TD-1 or TD-4 slot. Control wiring to these slots is presented in Table D

Note: This wiring will be installed only for the J98726W-1 and J98726W-2 shelf assemblies.

8 Install the AHG26 TD output wiring. Output wiring is presented in Table E

Note: This wiring will be installed only for the J98726W-1, J98726W-2, and the J98726Y-1.

Circuit Pack Installation

9 Set the AHG1 TA faceplate option plugs according to planned TD usage. Refer to Fig. 8 and Table F.

Requirement: The option plugs should be in the labeled "IN" positions for the corresponding TD positions that are planned for use. The options plugs should be in the unlabeled "out" positions for the corresponding TD positions that are not planned to be used.

10 Install the AHG1 TA circuit pack into the TA card slot.

Requirement: All LEDs (light emitting diodes) on the faceplate will be lighted.

11 Set the options (if provided) on the TI circuit packs. If the AHG2B TIs are used, set the input options on the sub-board according to Fig. 9 and Table G. If the AHG15 TIs are used, set the input options on the sub-board according to Fig. 10 and Table H.

STEP	PROCEDURE

12 Install TI circuit packs of the same type into the TI-A and TI-B card slots. The TIs may be either the AHG2, AHG2B, AHG10, or AHG15.

13 Wait approximately 15 to 30 seconds after inserting the last TI and press the MEM button on the TA.

Requirement: All yellow or red LEDs on the TIs and the yellow LEDs on the TA will be extinguished. Only the red TD LEDs on the TA and major alarm lamps on the fuse and alarm panel will be lighted. Only one IN SCE LED on one of the TI circuit packs will be lighted.

14 Set the appropriate options (if provided) on the TD circuit packs. If the AHG4 TD is used refer to Fig. 11, Table I. If the AHG5/25 TD is used refer to Fig. 12, Table J. If the AHG26 TD is used refer to Fig. 17, Table K.

15 Install the TD circuit pack(s) into the TD card slots. Leave the TD/s card slots empty in the J98726W-2 and J98726Y-1 panels. Use TD-1 slot first and then any other TD slot may be used.

Requirement: Only one TI ( ) OUTPUT IN USE LED will be lighted on each TD.

Note: The outputs of the two TIs connect to all four TD positions. When an SDE is first powered up, each TD may latch onto the output from TI-A or TI-B, if both are functioning properly. Only one of the two inputs is used by a TD at a given time. If desired, a nonlocking switch, TR IN SCE is operated on one of the TIs to provide the input signal source selection. Another nonlocking switch, TR OUT, is operated on one of the TIs to cause all TDs to select signals from one particular TI. The TR OUT switch is located only on the AHG2 and AHG2B TI circuit packs.

16 In each TD position (except position 1) where a TD is used, the corresponding white option plug on the AHG1 TA should be placed in the "IN" position. The "out" position is designated as the unlabeled position below the "IN" label for each numbered TD. Since there is no option setting for the TD-1 position, a TD must always be used in this slot. Press the MEM button on the AHG1 TA after these options are set.

Requirement: All LEDs on the AHG1 TA will be extinguished. All lamps on the fuse and alarm panel will be extinguished.

High Level Output Signal Measurements

Note: The following section will verify the output signals from the following TD circuit packs. AHG3, AHG5, and AHG25. If the AHG4 and AHG26 TD circuit packs are being used refer to the Low Level Output Signal Measurements section.

17 Set up a dual-trace oscilloscope for differential measurements with Channel 2 added and inverted using an internal trigger.

STEP	PROCEDURE

- Set Channels 1 and 2 to 2V/DIV.
- Channel 2 invert
- Set the time base to .5 μs/DIV (DS-1) or 20 μs/DIV (CC).

18 Measure the first ten clock outputs associated with the TD-1 circuit pack (Table L). Use the appropriate terminating across each X and Y lead (for outputs other than CC the X and Y leads become Tip and Ring). Connect the dual-trace oscilloscope probes across the resistor and connect both probe's shield leads to the most convenient terminal on the A row of the SDE terminal blocks.

Requirement: The waveforms observed must match the appropriate waveform shown in Fig. 13 or Fig. 14.

Note: All output measurements will be made at SDE A and SDE B terminal blocks. Refer to Tables L and M for the output test points corresponding to the TD circuit pack positions TD-1, TD-2, TD-3, and TD-4.

19 Repeat the previous Step for the remaining clock outputs for each TD located in the panel. If there are unused TD slots in the panel, then one of the working TD circuit packs may be rolled to the unused positions. To prevent audible alarms from being reported during this check, the ACO switch on the Fuse & Alarm panel may be activated (lighted switch).

20 When finished testing the clock outputs replace the TDs into their assigned slots. Depress the MEM button on the TA circuit pack and press the ACO button if lighted.

Requirement: All LEDs will be extinguished on the TA and all lamps on the fuse and alarm panel will be extinguished.

Note: Only the unused outputs of the AHG5/25 TDs must be terminated across tip and ring with a 100 ohm resistor (nine are provided with each AHG5/25 TD circuit pack). If the output is to be used, they must be deleted.

21 A check of the validity of the CC outputs may be made by one of the following two methods. If CC inputs are used, they may be directly compared with the outputs. This comparison may be made by using a dual-trace oscilloscope with the following adjustments:

- Channels 1 and 2 set to 5V/DIV, DC coupling, ALT
- Time base set to 20 μs/DIV
- Trigger set to Channel 1, AC coupling, AUTO

22 Connect Channel 1 to TS2 at terminal 2 and the probe's ground to terminal 1. Connect Channel 2 to the C1 terminal on SDE A terminal block and the probe's ground to B1. Adjust the trigger level for a stable trace.

STEP	PROCEDURE

Requirement: The waveforms will be stationary with respect to each other.

23 Repeat the previous Step but connect Channel 1 to TS2 terminal 7 and ground to terminal 6.

CAUTION: The following Step may be service affecting and should be done during off-peak hours.

24 If DS-1 or DS-1C inputs are used, the frequency of each TI's CC generating circuitry may be compared or measured. If the AHG2 or AHG2B TIs are used, this operation may be done by using a dual-trace oscilloscope with the following adjustments:

- Channels 1 and 2 set to 5V/DIV, DC coupling, ALT
- Time base set to 5μs/DIV (AHG2 and AHG2B TI)
- Trigger set to Channel 1, AC coupling, AUTO

Note: If using the AHG15 TI, go to Step 28.

25 Connect Channel 1 to TI-A test points as follows:

- AHG2 - Terminal 41 of J2
- AHG2B - Terminal 5 of J2

Connect the probe's shield to frame ground.

26 Connect Channel 2 to TI-B test points as follows:

- AHG2 - Terminal 41 of J3
- AHG2B - Terminal 5 of J3

Connect the probe's shield to frame ground.

27 Examine the two traces on the oscilloscope.

Requirement: Two 256 kHz square waves should be visible. There should be no rolling or cycle slipping between the two square waves.

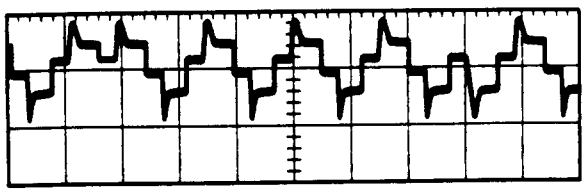
28 If the AHG15 TIs are used, this clock frequency may be directly measured at the TST faceplate pin jack with a frequency counter. The frequency will be a 4.096 MHz square wave. The frequency counter's probe should be connected via a pin plug to the TST jack of TI-A and the probe's shield connected to the faceplate latch.

Requirement: The resulting frequency shall be 4.096 MHz +/- 1 Hz.

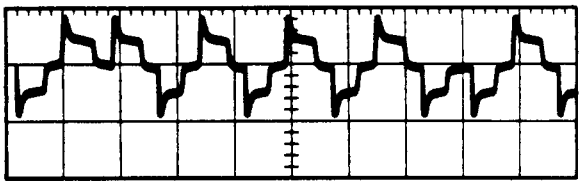
29 Repeat the above Step for the AHG15 TI IN TI-B slot.

STEP	PROCEDURE
30	Remove the DS-1 or 1C inputs to the TIs and then restore them. Wait approximately 45 seconds and then repeat the previous frequency evaluation Steps for the AHG2 or AHG2B TI (Step 27) or AHG15 TI (Steps 28 and 29). *Note:* This is the end of verifying the output signals for the AHG3, AHG5, and AHG25 TDs. If the AHG4 or AHG26 TD are used, Steps 31 to 42 should be followed. **Low Level Output Signal Measurements** *Note:* The following Steps will verify the output signals from the AHG4 and AHG26 TD circuit packs.
31	Set a dual-trace oscilloscope for differential measurements as follows: • Set Channels 1 and 2 to .5 volts/Div • Time Base set to 20μs/DIV (for 64 kHz output from the AHG4 TD) • Time Base set to 2μs/DIV (for 512 kHz output from the AHG4 TD) • Time Base set to 200 ns/DIV (for 2.048 MHz output from the AHG26 TD) • Trigger set to Channel 1, AC coupling, Auto
32	If using an AHG4 TD, remove the circuit pack and re-option as follows: • Set the dip switch positions 1 and 2 to +10 dB. *Note:* The AHG4 TD is capable of transmitting output signals at very low levels that are difficult to view with an oscilloscope. However, the nonattenuated output (+10 dBm) provides a signal that may be checked easily.
33	Replace the AHG4 TD in TD-4 slot and observe the red CUT OFF LED extinguish after two seconds.
34	If using the AHG4 TD connect the dual-trace oscilloscope to the backplane pins of the TD-4 (48 [tip] and 21 [ring]). Measure across a 133 ohm resistor for proper termination. Connect both probe's shield leads to frame ground. ***Requirement:*** One of the waveforms in Fig. 15a or 15b should be observed.
35	Remove the oscilloscope leads and terminating resistor.
36	If using the AHG26 TD connect the dual-trace oscilloscope to the 2.048 MHz +10 dBm faceplate jack. Use a bantam plug to obtain access to the tip (Channel 1) and ring (Channel 2) connections. Measure across a 75 ohm resistor for proper termination. Connect both probe's shield leads to frame ground.

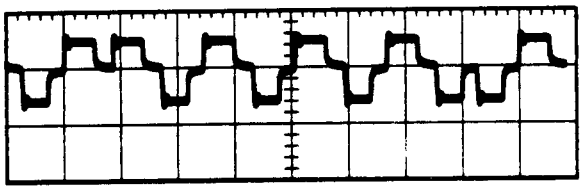
STEP	PROCEDURE
	Requirement: The waveform in Fig. 16 should be observed.
37	Remove the oscilloscope leads, terminating resistor, and bantam plug.
38	If using the AHG26 TD connect a frequency counter to the 2.048 MHz +10 dBm faceplate jack. Use a bantam plug to obtain access to the tip (Probe) and ring (Shield) connections. Measure across a 75 ohm resistor for proper termination.
	Requirement: A frequency of 2.048 MHz +/- 1 Hz shall be measured.
39	Remove the frequency counter leads, terminating resistor, and bantam plug.
40	If using an AHG4 TD remove the TD and select the proper options for the desired output. The option settings are given in Table I.
	Note 1: The output frequency of the AHG4 TD is dependent on the PFS used (either 64 kHz or 512 kHz). The output attenuation is dependent on the frequency (-54 dBm for 64 kHz and -23 dBm for 512 kHz).
	Note 2: Detailed wiring information showing input connections to the PFS-2B may be found in SD-50802-1.
41	Install the AHG4 TD and wait two seconds.
	Requirement: With wiring installed from the SDE to the PFS, the LOSS OF SYNC alarms on the PFS will clear and the Sensitrol will indicate a stable reading of approximately zero.
42	This is the end of verifying output signals for the AHG4 and AHG26 TD.



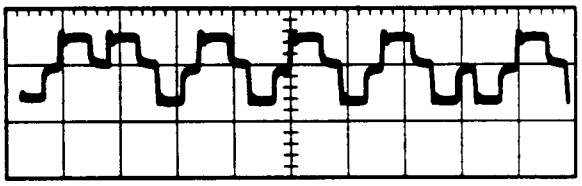
A. CABLE LENGTH - 50 FT. OR LESS



B. CABLE LENGTH - 500 FT.



C. CABLE LENGTH - 1000 FT.



D. CABLE LENGTH - 1500 FT.

Fig. 5 - Composite Clock Input Waveforms

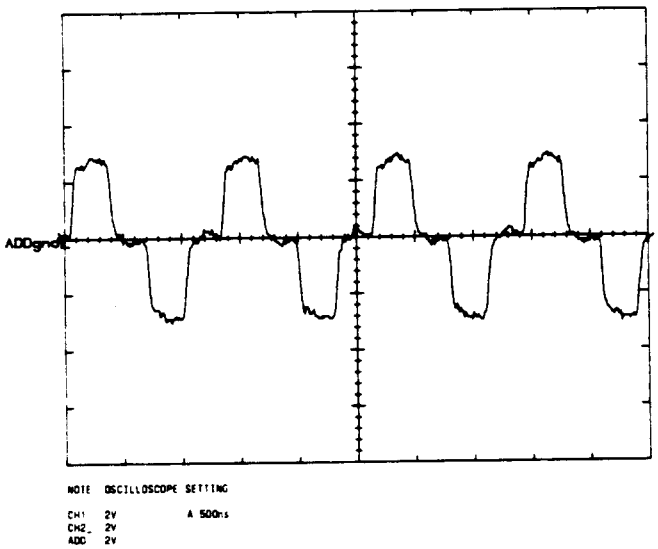


Fig. 6A - DS-1 Input Waveforms

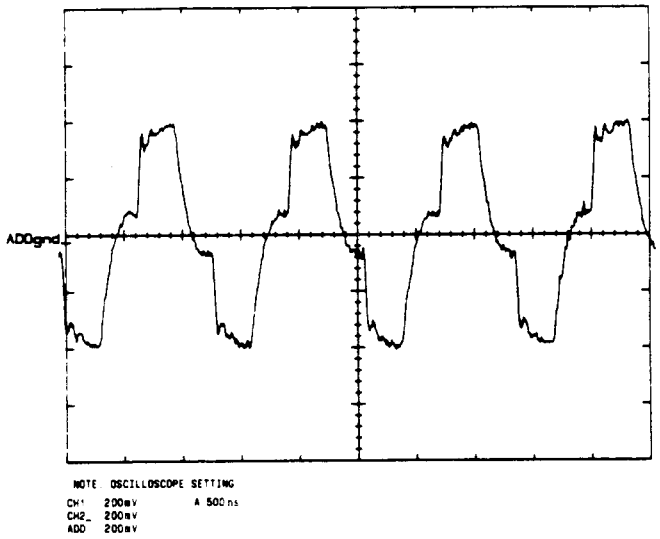


Fig. 6B - DS-1 Bridged Input Waveform

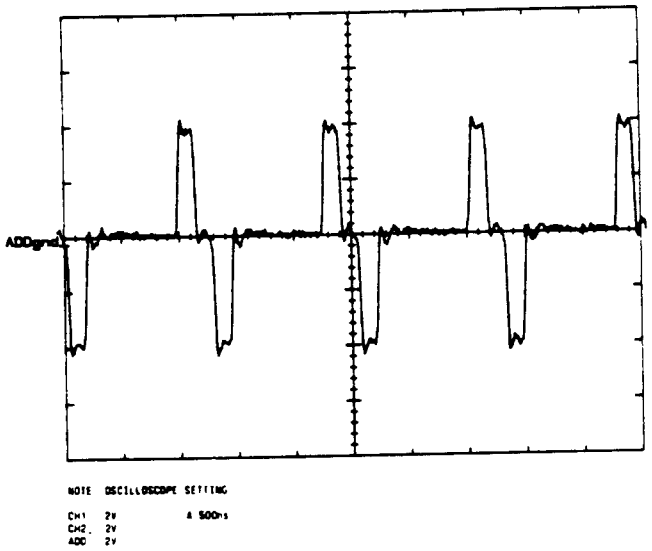


Fig. 7A - DS-1C Input Waveforms

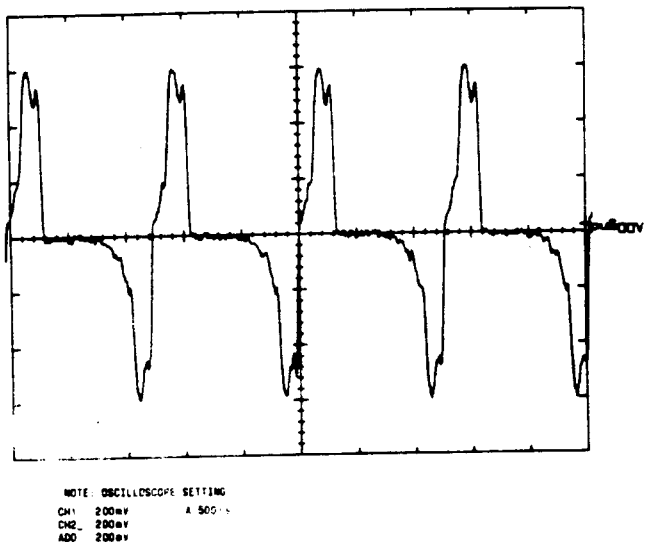


Fig. 7B - DS-1C Bridged Input Waveform

TABLE A (NOTE)

AHG4 TIMING DISTRIBUTOR CONTROL WIRING

J98726W-1 PANEL CONNECTIONS

FROM		TO	
CONNECTOR	TERMINALS	CONNECTOR	TERMINALS
J2 (TI-A)	16	J10 (TD-4)	42
J3 (TI-B)	16	J10 (TD-4)	43

J98726W-2 PANEL CONNECTIONS

FROM		TO	
CONNECTOR	TERMINALS	CONNECTOR	TERMINALS
J2 (TI-A)	16	J2 (TI-A)	45
J3 (TI-A)	16	J2 (TI-A)	45
J9 (TD-3)	44	J10 (TD-4)	42
J9 (TD-3)	45	J10 (TD -4)	43

Note: All control wire connections shall be made with 26-gauge wire.

TABLE B (NOTES 1, AND 2)

AHG4 TIMING DISTRIBUTOR OUTPUT WIRING

ATTENUATED-OUTPUT CONNECTIONS

FROM		TO		
CONNECTOR	TERMINALS	CONNECTOR	TERMINALS	TYPE
J10 (TD-4)	22	SDE B	D20	GRD
J10 (TD-4)	20	SDE B	E20	TIP
J10 (TD-4)	47	SDE B	F20	RING

NONATTENUATED-OUTPUT CONNECTIONS

FROM		TO		
CONNECTOR	TERMINALS	CONNECTOR	TERMINALS	TYPE
J10 (TD-4)	22	SDE B	D20	GRD
J10 (TD-4)	21	SDE B	E20	TIP
J10 (TD-4)	48	SDE B	F20	RING

*Note 1:*All tip, ring, and ground wires are 26-gauge twisted triples with three twists per inch and within one half at each end.

*Note 2:*All cabling from the SDE ( ) terminal blocks to the PFS (J68857AC) will be 22BF-type cable and should not exceed a length of 1000 feet.

TABLE C (NOTE)

AHG5/25 TIMING DISTRIBUTOR CONTROL WIRING PER TD SLOT

J98726W-2 PANEL CONNECTIONS

TD SLOT	FROM CONNECTOR	FROM TERMINALS	TO CONNECTOR	TO TERMINALS
ALL	J2 (TI-A)	16	J2 (TI-A)	43,44,45
	J3 (TI-B)	16	J3 (TI-B)	43,44,45
TD-1	J4 (TD-1)	44	J4 (TD-1)	42
	J4 (TD-1)	45	J4 (TD-1)	43
TD-2	J6 (TD-2)	44	J6 (TD-2)	42
	J6 (TD-2)	45	J6 (TD-2)	43
TD-3	J8 (TD-3)	44	J8 (TD-3)	42
	J8 (TD-3)	45	J8 (TD-3)	43
TD-4	J9 (TD-3/S)	44	J10 (TD-4)	42
	J9 (TD-3/S)	45	J10 (TD-4)	43

Note: All control wire connections shall be made with 26-gauge wire.

TABLE D (NOTE)

AHG26 TIMING DISTRIBUTOR CONTROL WIRING PER TD SLOT

J98726W-2 PANEL CONNECTIONS

TD SLOT	FROM CONNECTOR	FROM TERMINALS	TO CONNECTOR	TO TERMINALS
ALL	J2 (TI-A)	16	J2 (TI-A)	43,45
	J3 (TI-B)	16	J3 (TI-B)	43,45
TD-1	J4 (TD-1)	44	J4 (TD-1)	42
	J4 (TD-1)	45	J4 (TD-1)	43
TD-4	J9 (TD-3/S)	44	J10 (TD-4)	42
	J9 (TD-3/S)	45	J10 (TD-4)	43

Note: All control wire connections shall be made with 26-gauge wire.

TABLE E (NOTES 1 AND 2)

AHG26 OUTPUT WIRING CONNECTIONS PER TD SLOT

TD SLOT	FROM		TO		TYPE
	CONNECTOR	TERMINALS	CONNECTOR	TERMINALS	
TD1	J4 (TD 1)	20	SDE A	E1	SHIELD
	J4 (TD 1)	47	SDE A	F1	TIP
	SDE A	A1	SDE A	E1	-
TD4	J10 (TD 2)	20	SDE B	E20	SHIELD
	J10 (TD 2)	47	SDE B	F20	TIP
	SDE B	A20	SDE B	E20	-

Note 1: All wiring between the backplane and SDE ( ) terminal blocks shall be twisted pair with three twists per inch (26 gauge or equivalent).

Note 2: All cabling from SDE ( ) terminal blocks shall be 728A or equivalent and not to exceed 1500 feet.

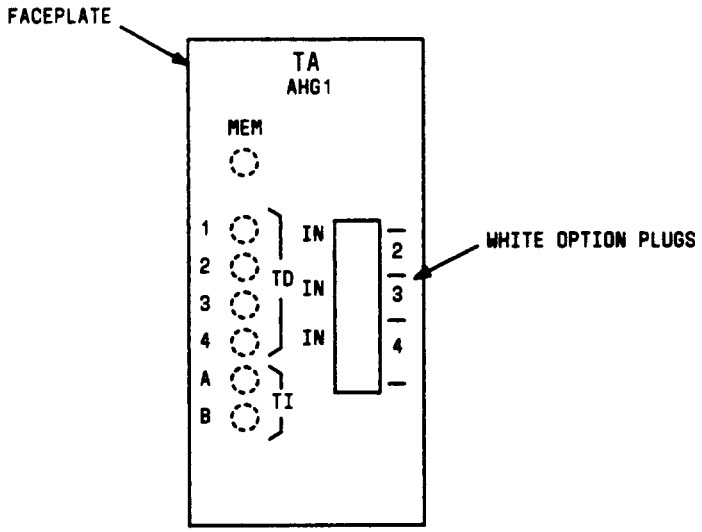


Fig. 8 - Location of Options for the AHG1 Timing Alarm Circuit Packs

TABLE F AHG1 TIMING ALARM OPTIONS						
TD POSITIONS USED				TD OPTION		
1	2	3	4	2	3	4
YES	NO	NO	NO	OUT	OUT	OUT
YES	YES	NO	NO	IN	OUT	OUT
YES	YES	YES	NO	IN	IN	OUT
YES	YES	YES	YES	IN	IN	IN

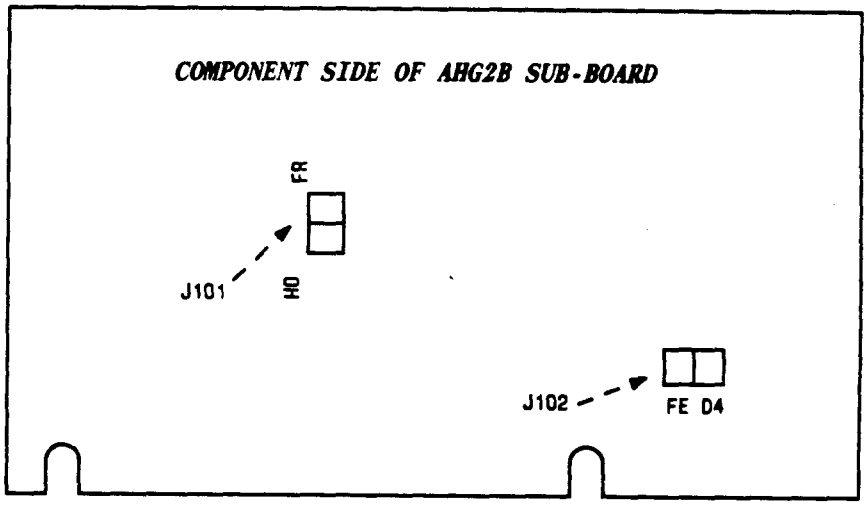


Fig. 9 - Location of Options on the AHG2B Timing Interface Circuit Pack

TABLE G AHG2B TIMING INTERFACE OPTIONS			
INPUT SIGNAL	FRAMING	J101	J102
DS-1	D4	HO	D4
DS-1	ESF	HO	FE
CC	-	FR	-
NONE	-	FR	-

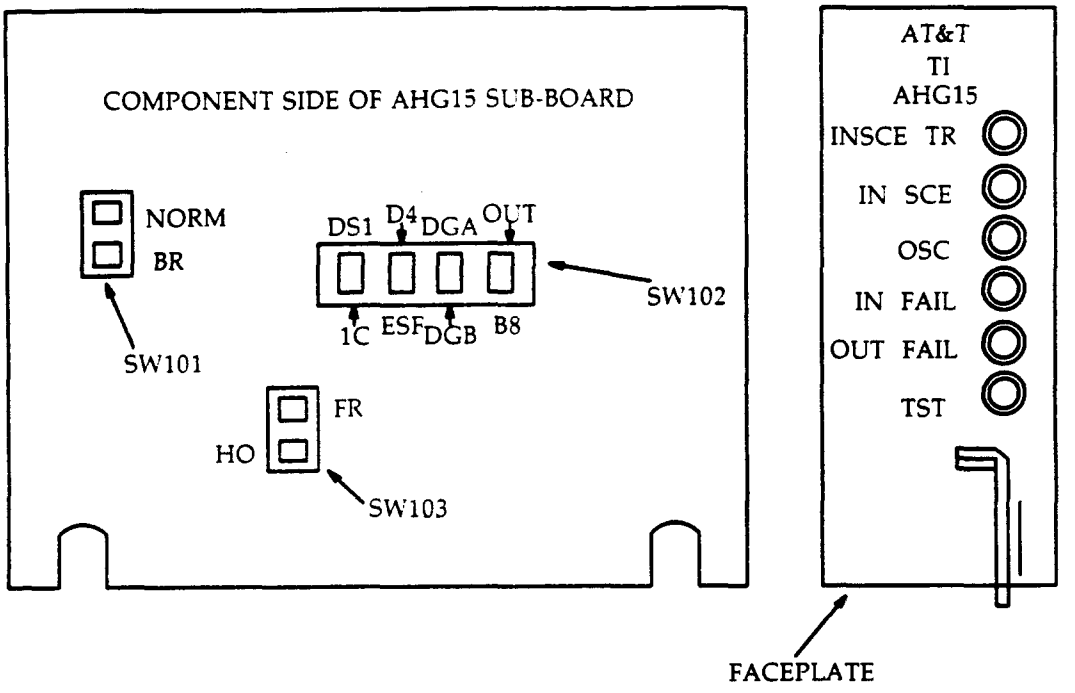


Fig. 10 - Location of Options on the AHG15 Timing Interface Circuit Pack

TABLE H AHG15 TIMING INTERFACE OPTIONS	
SW 101 POSITION	**OPTION**
NORM	DS-1/1C Normal Level Input
BR	DS-1/1C Monitor Level Input
SW 102 POSITION	**OPTION**
DS-1	DS-1 Format Input
1C	DS-1C Format Input
D4	D4 Framing
ESF	Extended Superframe Framing
DGA	Di-Group (A) Selection of DS-1C
DGB	Di-Group (B) Selection of DS-1C
OUT	B8ZS Format Off
B8	B8ZS Format On
SW 103 POSITION	**OPTION**
HO	Holdover Mode
FR	Free Run Mode

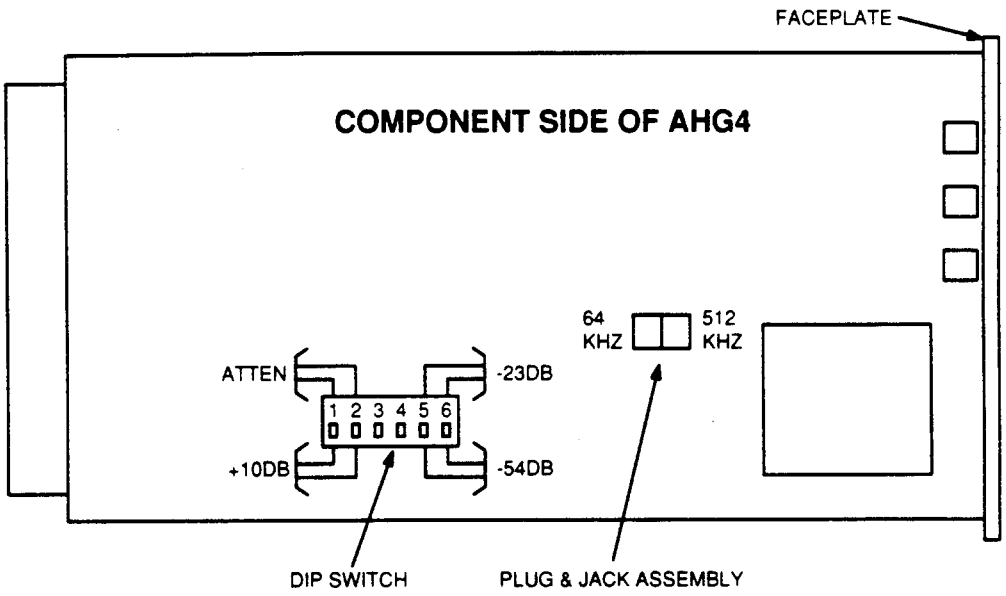


Fig. 11 - Location of Options on the AHG4 Timing Distributor Circuit Pack

TABLE I
AHG4 TIMING DISTRIBUTOR OPTIONS

DESIRED OUTPUT	DIP SWITCH						PLUG POSITION
	1	2	3	4	5	6	
512 kHz @ -23 dBm	ATTEN	ATTEN	-	-	-23DB	-23DB	512 KHZ
64 kHz @ -54 dBm	ATTEN	ATTEN	-	-	-54DB	-54DB	64 KHZ
512 kHz @ +10 dBm	+10DB	+10DB	-	-	-	-	512 KHZ
64 kHz @ +7 dBm	+10DB	+10DB	-	-	-	-	64 KHZ

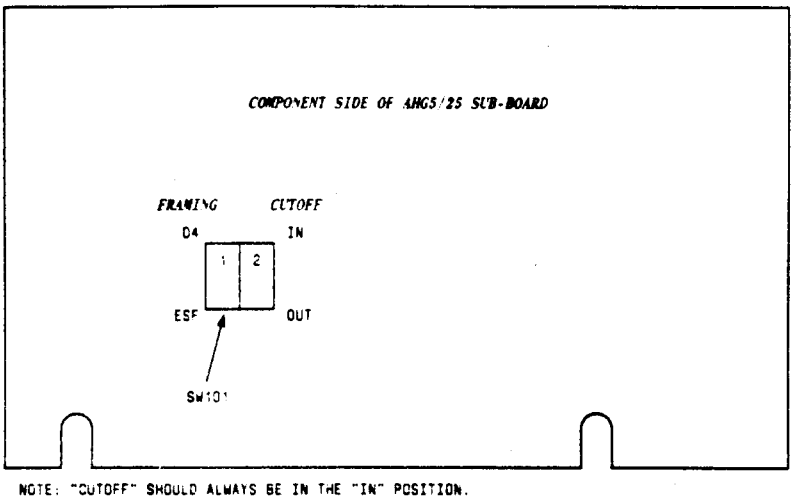
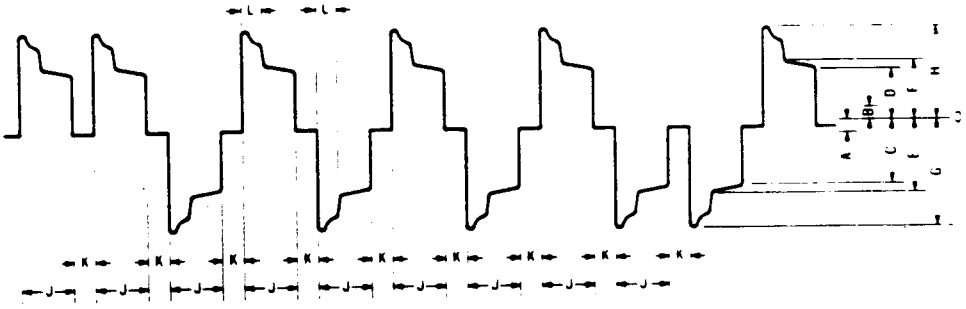


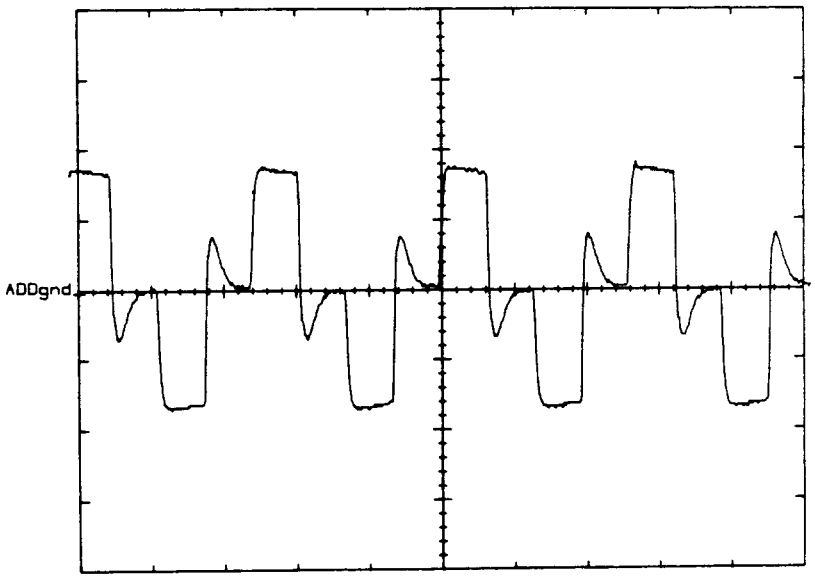
Fig. 12 - Location of Options on the AHG5/25 TD

TABLE J AHG5/25 TIMING DISTRIBUTOR OPTIONS	
SWITCH 101 POSITION	**OPTION**
D4	DS-1 Output Framing Format is D4
ESF	DS-1 Output Framing Format is ESF
IN	Cut Off Option Enabled
OUT	Cut Off Option Disabled



A = 0.2 ± 0.2 VOLTS
B = 0.2 ± 0.2 VOLTS
C = 2.9 ± 0.5 VOLTS
D = 2.9 ± 0.5 VOLTS
E = 3.2 ± 0.5 VOLTS
F = 3.2 ± 0.5 VOLTS
G = 5 ± 0.4 VOLTS
H = 5 ± 0.4 VOLTS
J = 9.8 ± 0.2 μSECS
K = 5.8 ± 0.2 μSECS
L = 2.0 ± 0.2 μSECS

Fig. 13 - Composite Clock Output Waveform at SDE Terminal Blocks



NOTE: OSCILLOSCOPE SETTING

CH1 2V A 500ns
CH2_ 2V
ADD 2V

Fig. 14 - AHG5/25 TD DS-1 Output Waveform

TABLE K AHG26 TIMING DISTRIBUTOR OPTIONS	
SWITCH 1 POSITION	OPTION
-35 dBm	2.048 MHz Sine Wave Output @ -35 dBm
-20 dBm	2.048 MHz Sine Wave Output @ -20 dBm

TABLE L (NOTE)

SDE A TERMINAL BLOCK CONNECTIONS

OUTPUT LEAD	X CONNECTION TERMINAL BLOCK	TERMINAL	LEAD	SDE BACKPLANE CONNECTION	OUTPUT LEAD	X CONNECTION TERMINAL BLOCK	TERMINAL	LEAD	SDE BACKPLANE CONNECTION
L1Y	SDE A	C1	32	TD-1	L11Y	SDE A	C11	32	TD-2
L1X	SDE A	B1	5	TD-1	L11X	SDE A	B11	5	TD-2
S	SDE A	A1		TD-1	S	SDE A	A11		TD-2
L2Y	SDE A	C2	33	TD-1	L12Y	SDE A	C12	33	TD-2
L2X	SDE A	B2	6	TD-1	L12X	SDE A	B12	6	TD-2
S	SDE A	A2		TD-1	S	SDE A	A12		TD-2
L3Y	SDE A	C3	34	TD-1	L13Y	SDE A	C13	34	TD-2
L3X	SDE A	B3	7	TD-1	L13X	SDE A	B13	7	TD-2
S	SDE A	A3		TD-1	S	SDE A	A13		TD-2
L4Y	SDE A	C4	35	TD-1	L14Y	SDE A	C14	35	TD-2
L4X	SDE A	B4	8	TD-1	L14X	SDE A	B14	8	TD-2
S	SDE A	A4		TD-1	S	SDE A	A14		TD-2
L5Y	SDE A	C5	36	TD-1	L15Y	SDE A	C15	36	TD-2
L5X	SDE A	B5	9	TD-1	L15X	SDE A	B15	9	TD-2
S	SDE A	A5		TD-1	S	SDE A	A15		TD-2
L6Y	SDE A	C6	37	TD-1	L16Y	SDE A	C16	37	TD-2
L6X	SDE A	B6	10	TD-1	L16X	SDE A	B16	10	TD-2
S	SDE A	A6		TD-1	S	SDE A	A16		TD-2
L7Y	SDE A	C7	38	TD-1	L17Y	SDE A	C17	38	TD-2
L7X	SDE A	B7	11	TD-1	L17X	SDE A	B17	11	TD-2
S	SDE A	A7		TD-1	S	SDE A	A17		TD-2
L8Y	SDE A	C8	39	TD-1	L18Y	SDE A	C18	39	TD-2
L8X	SDE A	B8	12	TD-1	L18X	SDE A	B18	12	TD-2
S	SDE A	A8		TD-1	S	SDE A	A18		TD-2
L9Y	SDE A	C9	40	TD-1	L19Y	SDE A	C19	40	TD-2
L9X	SDE A	B9	13	TD-1	L19X	SDE A	B19	13	TD-2
S	SDE A	A9		TD-1	S	SDE A	A19		TD-2
L10Y	SDE A	C10	41	TD-1	L20Y	SDE A	C20	41	TD-2
L10X	SDE A	B10	14	TD-1	L20X	SDE A	B20	14	TD-2
S	SDE A	A10		TD-1	S	SDE A	A20		TD-2

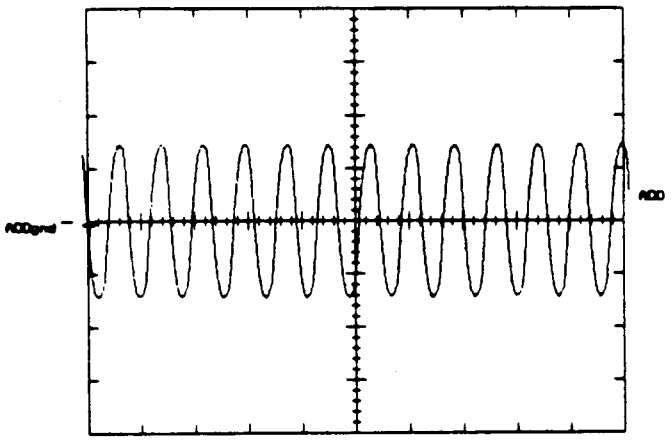
*Note:*Output taps labeled L( )X and L( )Y may be other than CC format.

TABLE M (NOTE)

SDE B TERMINAL BLOCK CONNECTIONS

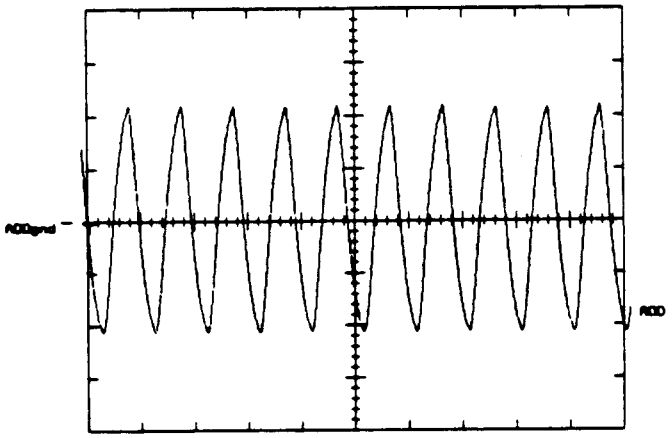
OUTPUT LEAD	X CONNECTION TERMINAL BLOCK	TERMINAL	LEAD	SDE BACKPLANE CONNECTION	OUTPUT LEAD	X CONNECTION TERMINAL BLOCK	TERMINAL	LEAD	SDE BACKPLANE CONNECTION
L21Y	SDE B	C1	32	TD-3	L31Y	SDE B	C11	32	TD-4
L21X	SDE B	B1	5	TD-3	L31X	SDE B	B11	5	TD-4
S	SDE B	A1		TD-3	S	SDE B	A11		TD-4
L22Y	SDE B	C2	33	TD-3	L32Y	SDE B	C12	33	TD-4
L22X	SDE B	B2	6	TD-3	L32X	SDE B	B12	6	TD-4
S	SDE B	A2		TD-3	S	SDE B	A12		TD-4
L23Y	SDE B	C3	34	TD-3	L33Y	SDE B	C13	34	TD-4
L23X	SDE B	B3	7	TD-3	L33X	SDE B	B13	7	TD-4
S	SDE B	A3		TD-3	S	SDE B	A13		TD-4
L24Y	SDE B	C4	35	TD-3	L34Y	SDE B	C14	35	TD-4
L24X	SDE B	B4	8	TD-3	L34X	SDE B	B14	8	TD-4
S	SDE B	A4		TD-3	S	SDE B	A14		TD-4
L25Y	SDE B	C5	36	TD-3	L35Y	SDE B	C15	36	TD-4
L25X	SDE B	B5	9	TD-3	L35X	SDE B	B15	9	TD-4
S	SDE B	A5		TD-3	S	SDE B	A15		TD-4
L26Y	SDE B	C6	37	TD-3	L36Y	SDE B	C16	37	TD-4
L26X	SDE B	B6	10	TD-3	L36X	SDE B	B16	10	TD-4
S	SDE B	A6		TD-3	S	SDE B	A16		TD-4
L27Y	SDE B	C7	38	TD-3	L37Y	SDE B	C17	38	TD-4
L27X	SDE B	B7	11	TD-3	L37X	SDE B	B17	11	TD-4
S	SDE B	A7		TD-3	S	SDE B	A17		TD-4
L28Y	SDE B	C8	39	TD-3	L38Y	SDE B	C18	39	TD-4
L28X	SDE B	B8	12	TD-3	L38X	SDE B	B18	12	TD-4
S	SDE B	A8		TD-3	S	SDE B	A18		TD-4
L29Y	SDE B	C9	40	TD-3	L39Y	SDE B	C19	40	TD-4
L29X	SDE B	B9	13	TD-3	L39X	SDE B	B19	13	TD-4
S	SDE B	A9		TD-3	S	SDE B	A19		TD-4
L30Y	SDE B	C10	41	TD-3	L40Y	SDE B	C20	41	TD-4
L30X	SDE B	B10	14	TD-3	L40X	SDE B	B20	14	TD-4
S	SDE B	A10		TD-3	S	SDE B	A20		TD-4

*Note:*Output taps labeled L( )X and L( )Y may be other than CC format.



A. 64 kHz

NOTE: OSCILLOSCOPE SETTING
CH1 500 mV A 20 us
CH2_ 500 mV
ADD 500 mV



B. 512 kHz

NOTE: OSCILLOSCOPE SETTING
CH1 500 mV A 2 us
CH2_ 500 mV
ADD 500 mV

Fig. 15 - Nonattenuated AHG4 TD Output Waveforms

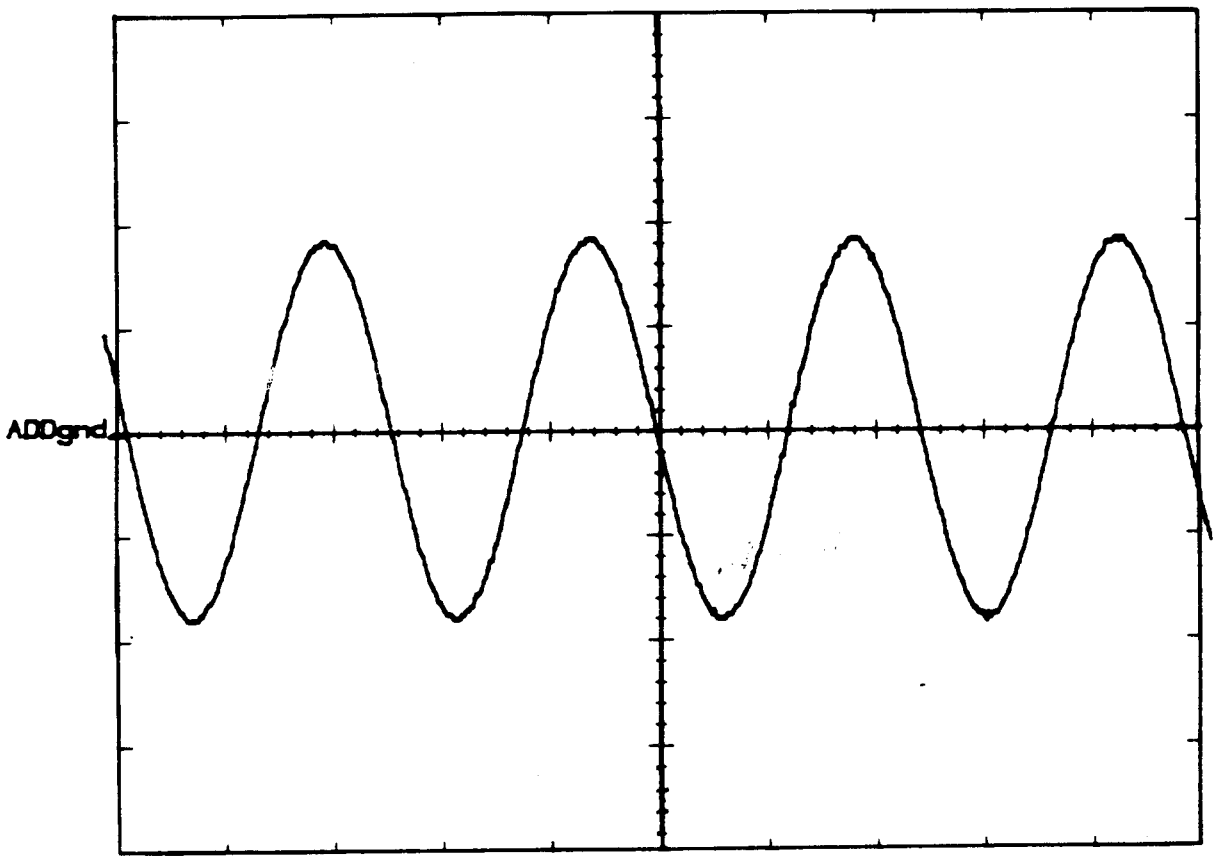


Fig. 16 - AHG26 Monitor Output (2.048 MHz) Waveform

D. CHART 4 — REPLACING CIRCUIT PACKS

STEP	PROCEDURE

Removal of the Timing Alarm Circuit Pack

Note: The AHG1 TA is the only code for the TA circuit pack. The TA circuit pack reports the alarm status from the TI and TD circuit packs. The TA does not interact directly with the timing signals of the SDE and therefore may be removed without disruption of service.

1 Press the ACO switch located on the Fuse & Alarm panel so that the switch lights.

Requirement: Audible alarms will be silenced.

2 Set the white option plugs on the replacement AHG1 TA circuit pack to those of the removed TA.

3 Remove the AHG1 TA circuit pack from the TA slot.

4 Insert the replacement TA circuit pack into the TA slot.

5 Press the MEM switch on the faceplate of the TA

Requirement: All LEDs on the TA should extinguish.

6 Press the ACO switch located on the Fuse & Alarm panel.

Requirement: The ACO lamp should extinguish.

Removal of the Timing Interface Circuit Packs

Note: There are four codes of TI circuit packs that are available for the SDE. AHG2, AHG2B, AHG10, and AHG15. Two TI circuit packs are used in a single SDE panel which provides an input signal redundancy. This redundancy makes it possible to remove a single TI circuit pack from an SDE panel without disruption of the input signal.

CAUTION: Only remove a TI when a replacement TI is optioned and ready to be inserted. The TI removal may be service affecting and should be done during off-peak hours.

7 Press the ACO switch on the Fuse & Alarm panel so that the switch lights.

Requirement: Audible alarms will be silenced.

8 Press the IN SCE TR switch on the TI circuit pack to be removed.

Requirement: The IN SCE LED on the adjacent TI lights.

9 On the AHG2 and the AHG2B TIs, press the TR OUT switch on the TI to be removed.

STEP	PROCEDURE

Requirement: The corresponding TI OUTPUT IN USE LEDs light on the TD circuit packs.

10 If the AHG2B TI is used, set the proper input options located on the sub-board. Refer to Table G and Fig. 9. If the AHG15 TI is used, set the proper input options located on the sub-board. Refer to Table H and Fig. 10.

11 If the AHG2 TI is used, check to see if a strap exists across E1 and E2 on the top left-hand side of the board. If the strap is missing either install one or return to AT&T for repair.

12 Remove the bad TI. As a precaution, only remove the TI if a replacement TI is ready to be inserted.

13 Insert the replacement TI into the empty TI slot. Make sure that the replacement TI is the same type as the TI already in the panel.

Note 1: If the AHG2B or AHG15 TI are used, the yellow OSC LED should light and extinguish after 15 seconds. If the OSC LED does not extinguish after this time, the input signal is bad or possibly the replacement TI is at fault. Verification of proper operation may be found in Chart 3, Steps 24-30.

Note 2: If the AHG2 TI is used, allow 45 seconds from the time of insertion for the TI to lock on to the input. Verification of proper operation may be found in Chart 3, Step 30.

14 Press the MEM switch on the TA circuit pack.

Requirement: All LEDs on the TA will extinguish.

15 Press the ACO switch on the Fuse & Alarm panel.

Requirement: The ACO LED will extinguish.

Removal of the Timing Distributor Circuit Packs using PCS

Note: The PCS is a means for the replacement of an in-service AHG3 TD only. The PCS is only available on the J98726W-2 and the J98726Y-1 SDE panels.

CAUTION: Only remove a TD when a replacement TD is optioned and ready to be inserted. The TD removal may be service affecting and should be done during off-peak hours.

16 Press the ACO switch on the Fuse & Alarm panel.

Requirement: The ACO LED lights.

17 Depress and hold the TR OUT switch on the TI as indicated by the dark LED on the TD to be

STEP	PROCEDURE

replaced.

18 While holding the TR OUT switch in on the AHG2 or AHG2B TI, insert the SPARE TD into the TD/S slot to the right of the TD to be replaced.

19 While holding the TR OUT switch in on the AHG2 or AHG2B TI, remove the bad TD.

20 While holding the TR OUT switch in on the AHG2 or AHG2B TI, insert the replacement TD into the slot where the bad TD was located.

21 While holding the TR OUT switch in on the AHG2 or AHG2B TI, remove the TD in the TD/S slot and then release the TR OUT switch.

22 Press the MEM switch on the TA.

Requirement: All the LEDs will extinguish on the TA.

23 Press the ACO switch on the Fuse & Alarm panel.

Requirement: The ACO LED extinguishes.

Removal of the TD Circuit Pack Not Using the PCS Procedure

Note 1: There are five codes of TD circuit packs that are available for the SDE. AHG3 ,AHG4, AHG5, AHG25, and AHG26. The AHG3, AHG5, and AHG25 TDs may be placed in any TD slot, but the AHG4 TD may only be placed in the TD-4 slot. The AHG26 TD may only be placed in TD-1 or TD-4 slots.

Note 2: Only the AHG5 and AHG25 TD circuit packs may be interchanged. All other TDs must be replaced "like-for-like".

CAUTION: Only remove a TD when a replacement TD is optioned and ready to be inserted. The TD removal will be service affecting and should be done during off-peak hours.

24 Press the ACO switch on the Fuse & Alarm panel.

Requirement: The ACO LED lights.

25 If the AHG4, AHG5, AHG25, or AHG26 TDs are used, set the output options on the replacement TD according to those given in Table I, Fig. 11 or Table J, Fig. 12 or Table K, Fig. 17 respectively.

26 Remove the AHG4 , AHG5, AHG25 or AHG26 TDs from the panel.

STEP	PROCEDURE
	Requirement: Office alarms will sound at this point. Make sure a replacement TD is available before removing the bad TD.
27	Insert a TD of the same type as the one removed into the appropriate TD slot.
	Requirement: If the AHG4, AHG5, AHG25, or AHG26 TDs are inserted, the red CUTOFF LED will light for approximately two seconds and then extinguish.
28	If using the AHG4 TD, the Sensitrol on the PFS will need to be reset when the TD's CUT OFF LED extinguishes.
	Requirement: Only one TI OUTPUT IN USE LED will be lighted on the replacement TD. Office alarms will be silenced.
29	Press the MEM switch on the TA.
	Requirement: All of the LEDs extinguish on the TA.
30	Press the ACO switch on the Fuse & Alarm panel.
	Requirement: The ACO switch extinguishes.
	Note: Verification of proper operation may be done in Chart 3 under the "High Level" or "Low Level" output signal measurements section.

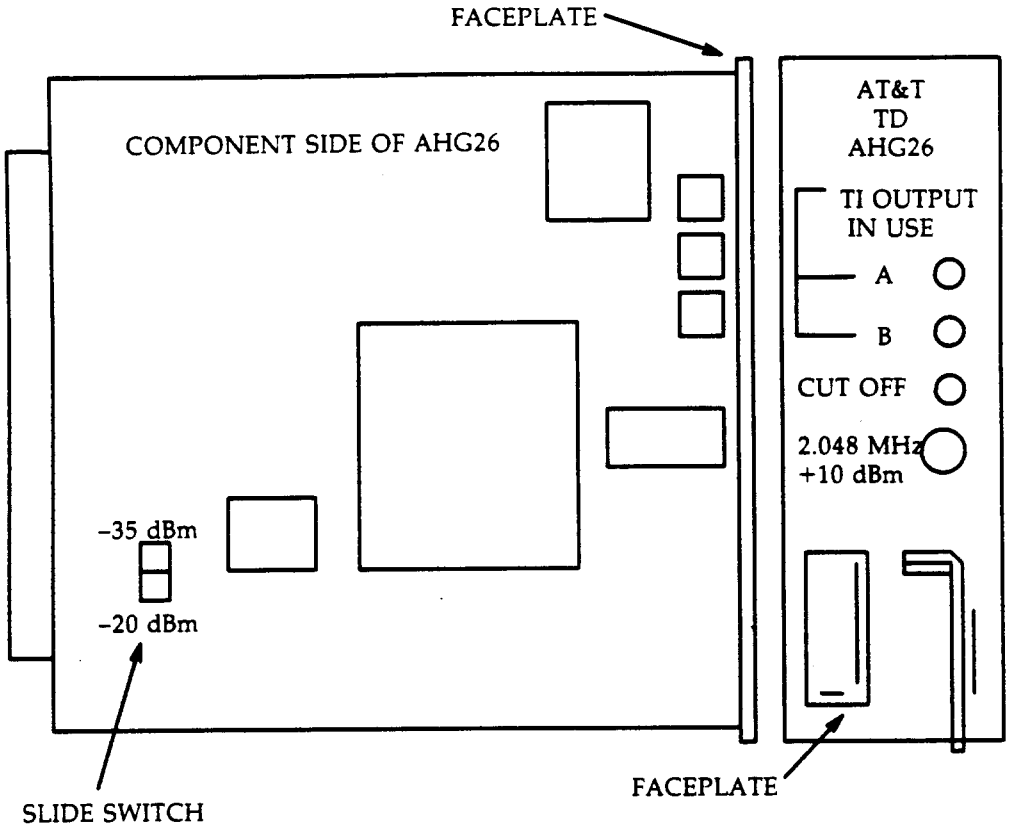


Fig. 17 - Location of Options on the AHG26 TD

TABLE N (NOTES 1, 2, 3, AND 4)
CABLING CONNECTIONS FOR AHG2B AUXILIARY PANEL

MAIN PANEL		AUXILIARY PANEL		
FROM		TO		CABLE
CONNECTOR	TERMINAL	CONNECTOR	TERMINAL	
J2 (TI-A)	2	J2 (TI-A)	2	A
J2 (TI-A)	3	J2 (TI-A)	3	A
J2 (TI-A)	29	J2 (TI-A)	29	A
J2 (TI-A)	30	J2 (TI-A)	30	A
J3 (TI-B)	2	J3 (TI-B)	2	B
J3 (TI-B)	3	J3 (TI-B)	3	B
J3 (TI-B)	29	J3 (TI-B)	29	B
J3 (TI-B)	30	J3 (TI-B)	30	B

AUXILIARY PANEL JUMPERS (NOTE 4)

CONNECTOR	FROM TERMINAL	TO TERMINAL
J2 (TI-A)	16	22
J3 (TI-B)	16	22

Note 1: Each twisted shielded pair consists of two 26-gauge wires, P1 and P2. The P1 connections are given in this table. All of the P2 connections are tied to the frame ground on each panel. Any unused wires should also be tied to the frame ground at both ends.

Note 2: The shield connection is tied to the frame ground on the main panel, but not connected on the auxiliary panel.

Note 3: The maximum overall cable length may not exceed 4 feet.

Note 4: All jumper wires should be 26-gauge wire.

E. CHART 5 — AHG2B AUXILIARY PANEL EXPANSION

STEP	PROCEDURE

Note 1: The auxiliary panel must be placed within a four-foot cabling distance from the main panel. The auxiliary panel will consist of either the J98726W-1, J98726W-2, or J98726Y-1 panel, one AHG1 TA, and at least one AHG3 TD. As an ESD precaution, it is recommended that blank board ED-8C715 (or equivalent) be placed in the vacant TI slots of the auxiliary panel. The only requirement for the main panel is that it contain two AHG2B TI circuit packs, one AHG1 TA circuit pack and at least one TD.

Note 2: If the AHG4, AHG5, AHG25, or AHG26 TDs are to be used, they may only be placed in the main panel.

1 Connect the auxiliary panel to -48 volt battery. (Chart 2 provides verification information of the -48 volt battery.)

CAUTION: The installation of cabling between the backplanes of the main and auxiliary panels must be done with care and may cause service affecting hits if the main panel is in service. Therefore, it is recommended that the installation be done during off-peak hours.

2 Connect the auxiliary panel to the office alarm. (Chart 1 provides verification information of the auxiliary panel alarms).

Note: The cabling between the main and auxiliary panels is identical for the J98726W-1, J98726W-2, and J98726Y-1 panels. The actual wiring is connected between the back planes of each panel with two separate multi-wire cables as shown in Fig. 18. Each cable consists of four 26-gauge twisted pairs in a common shield. One of the cables connects the output signals from TI-A of the main panel to TI-A of the auxiliary panel. The other cable connects the output signals from TI-B of the main panel to TI-B of the auxiliary panel. An individual ground return is carried by the second wire in each pair. The shield for each cable will be connected to frame ground of the main panel, but left open at the auxiliary panel.

3 Dress the cables as in Fig. 19. Connect the ground wires of each pair on the common ends of each cable with a crimp eyelet. Connect only the shield at the main panel end of each cable with a soldered pig-tail (not to exceed 1.5 inches) and also to the crimp eyelet. Any unused wires should also be connected to ground.

4 At the main panel, connect the eyelet on the main panel end of the cable to the second top screw from the right edge of the backplane as shown in Fig. 20.

5 At the auxiliary panel, connect the eyelet on the other end of the cable to the second top screw from the right edge of the backplane as shown in Fig. 20.

6 At the auxiliary panel, connect terminal 16 on J2 and J3 to ground as in Table N.

STEP	PROCEDURE
7	At the auxiliary panel, connect cables A and B to J2 and J3 as in Table N.
8	Press the IN SCE TR switch on TI-A. *Requirement:* The IN SCE LED on TI-B shall light.
9	Connect the A cable to J2 on the main panel as in Table N.
10	Press the IN TR switch on TI-B. *Requirement:* Observe the IN SCE LED light on TI-A.
11	Connect the B cable to J3 on the main panel as in Table N.
12	Connect the auxiliary panel to the office alarm. Refer to Chart 2 for verification information of the auxiliary panel alarms. *Note:* At this point, the auxiliary panel is fully connected and ready for operation. The auxiliary panel may accept up to four AHG3 TD circuit packs and TD-1 slot must be occupied.
13	Option the AHG1 TA according to Table F and Fig. 8. In each TD position (except for position 1) where a TD is to be used, place the corresponding white option plug on the AHG1 TA in the "IN" position. *Note:* The white option plugs allow the AHG1 TA to report alarm information about the corresponding TD slot when in the "IN" position and inhibit alarm information when in the "out" position. The "out" position is designated as the unlabeled position below the "IN" label for each numbered TD. Since there is no option setting for the TD-1 position, a TD must always be used in this slot.
14	Insert an AHG1 TA circuit pack into the TA slot on the auxiliary panel. All white option plugs on the faceplate will be in the "out" position (Fig. 8). *Requirement:* All of the red LEDs on the AHG1 TA will be lighted.
15	Install the TD circuit packs into the TD card slots (leave the TD/S card slots empty if applicable). Refer to the "Circuit Pack Installation" section of Chart 3. *Requirement:* Only one TI OUTPUT IN USE LED will be lighted on each TD. *Note 2:* The outputs of the two TIs on the main panel connect to all four TD positions on the auxiliary panel. When the circuit packs are first powered up, each TD may latch onto the output from TI-A or TI-B if both are functioning properly. Only one of the two inputs is used by a TD at a given time. When desired, a nonlocking switch, TR IN SCE, on one of the TIs is operated to provide the input signal source selection. Another nonlocking switch, TR OUT, is operated on one

STEP	PROCEDURE
	of the TIs to cause all TDs to select signals from one particular TI.
16	After installing all of the AHG3 TDs, press the MEM button on the AHG1 TA. ***Requirement:*** All LEDs on the AHG1 TA will be extinguished. All lamps on the Fuse & Alarm panel will be extinguished.
	Auxiliary Panel Check-Out
17	Compare the CC outputs of the main panel with the CC outputs of the auxiliary panel using a dual-trace oscilloscope with the following adjustments: • Channels 1 and 2 set to 5V/DIV, DC coupling, ALT • Time base set to 20 μs/DIV • Trigger set to Channel 1, AC coupling, AUTO
18	Press the IN SCE TR switch on TI-B. ***Requirement:*** The IN SCE LED lights on TI-A on the main panel.
19	Connect Channel 1 to any unused CC output tap on the SDE terminal block of the main panel. Connect the probe to the C row and the probe's shield to the B row. ***Requirement:*** This measurement shall be made across a 133 ohm resistor
20	Connect Channel 2 to the C1 terminal on SDE A terminal block of the auxiliary panel and the probe's ground to B1. ***Requirement:*** This measurement shall be made across a 133 ohm resistor
21	Adjust the trigger level for a stable trace. ***Requirement:*** The waveforms will be stationary with respect to each other as shown in Fig. 21.
22	Repeat the previous step except press the IN SCE TR switch on TI-A ***Requirement:*** The IN SCE LED lights on TI-B.
23	Set up the dual-trace oscilloscope differentially: • Channels 1 and 2 set to 5 V/DIV, DC coupling, ALT • Channel 2 set to INV • Time base set to 20 s/DIV

STEP	PROCEDURE
	• Trigger set to Channel 1, AC coupling, AUTO
24	Measure the first ten CC outputs associated with the TD-1 circuit pack (Use a 133-ohm resistor across each X and Y lead.) Bridge the dual-trace oscilloscope probes across the resistor and connect both of the ground leads on the probe to the most convenient terminal on the "A" row of the SDE terminal blocks. *Requirement:* The waveforms observed must agree with the waveform shown in Fig. 13. *Note:* All output measurements will be made at SDE A and SDE B terminal blocks of the auxiliary panel. Refer to Tables L and M for the output test points corresponding to the TD circuit pack positions TD-1, TD-2, TD-3, and TD-4.
25	Repeat the previous Step for the remaining CC outputs for each AHG3 TA located in the panel.
26	If there are unused TD slots in the panel, one of the working AHG3 TD circuit packs may be rolled to the unused positions. To prevent audible alarms from being reported during this check, the ACO switch on the Fuse & Alarm panel may be activated (lighted switch). *Requirement:* Results should agree with the previous Step.
27	When testing of the CC outputs is completed, replace the AHG3 TDs into their assigned slots.
28	Depress the MEM button on the TA circuit pack and press the ACO button on the Fuse & Alarm panel, if lighted. *Requirement:* All LEDs will be extinguished on the TA and all lamps on the Fuse & Alarm panel will be extinguished.

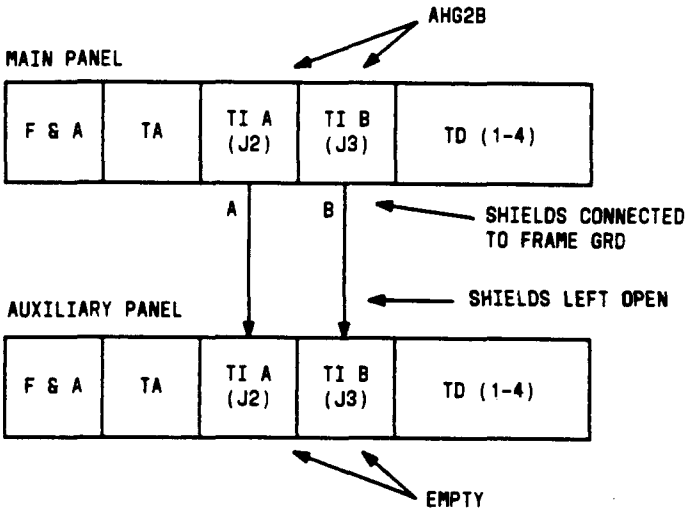


Fig. 18 - Cabling Diagram Showing AHG2B Auxiliary Panel Expansion

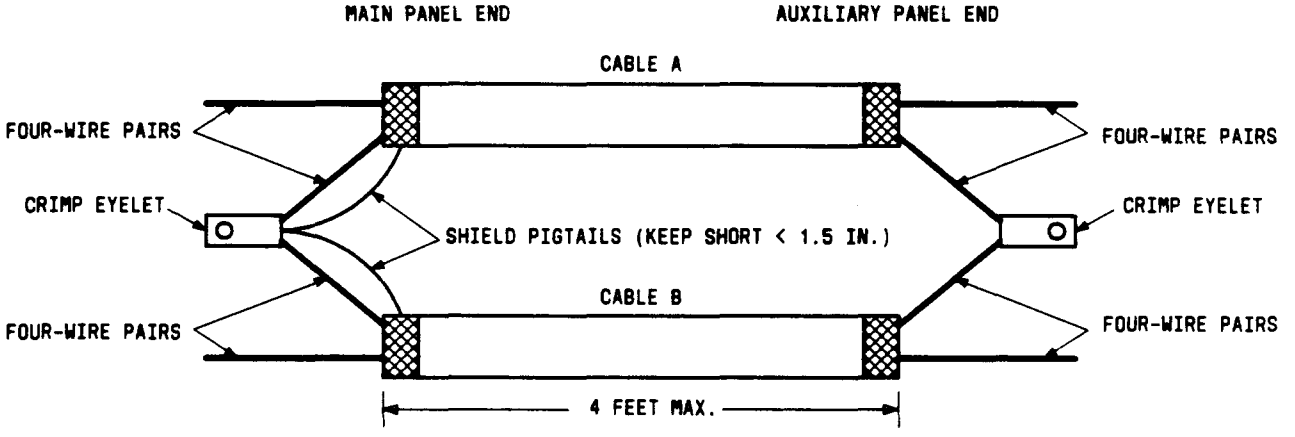


Fig. 19 - Cable Dressing for AHG2B Auxiliary Panel

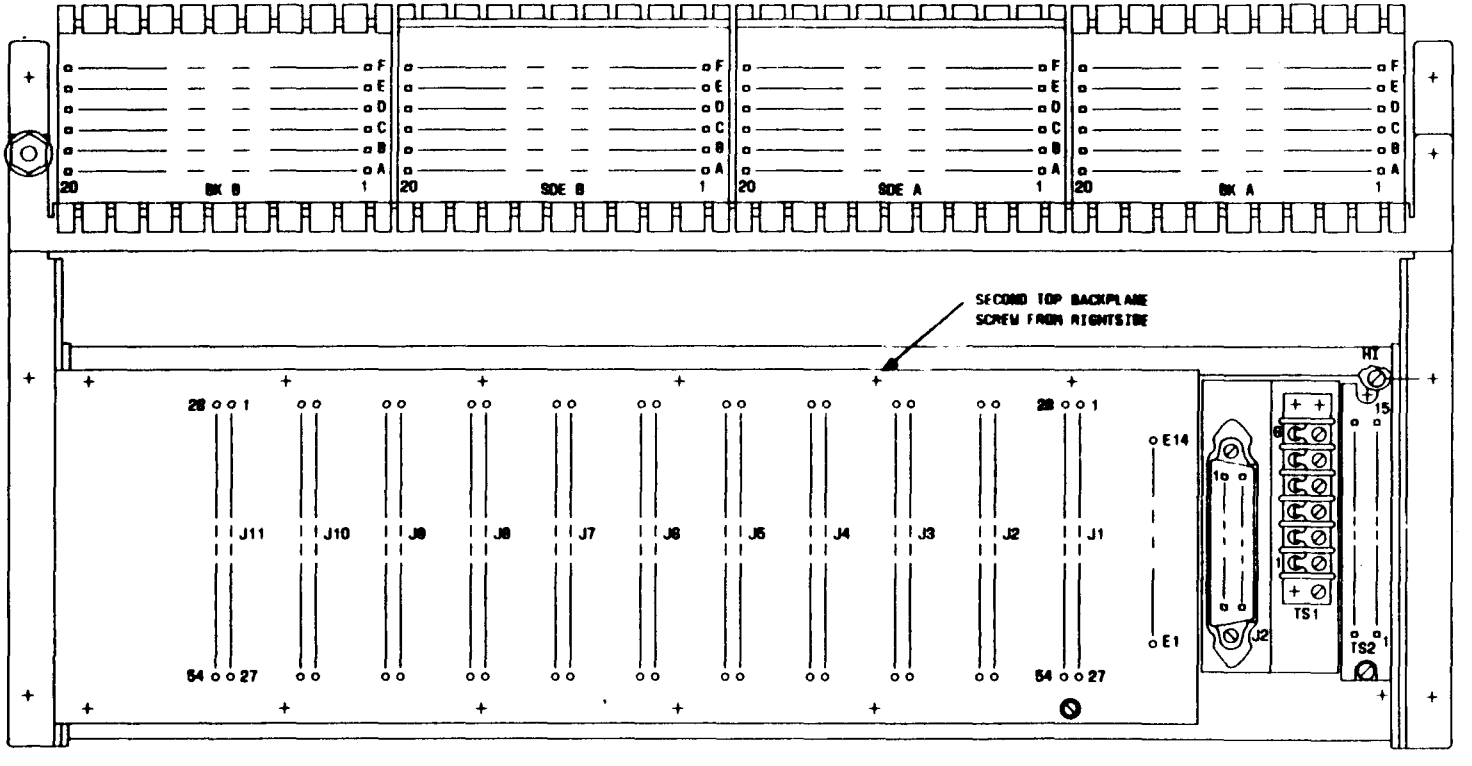
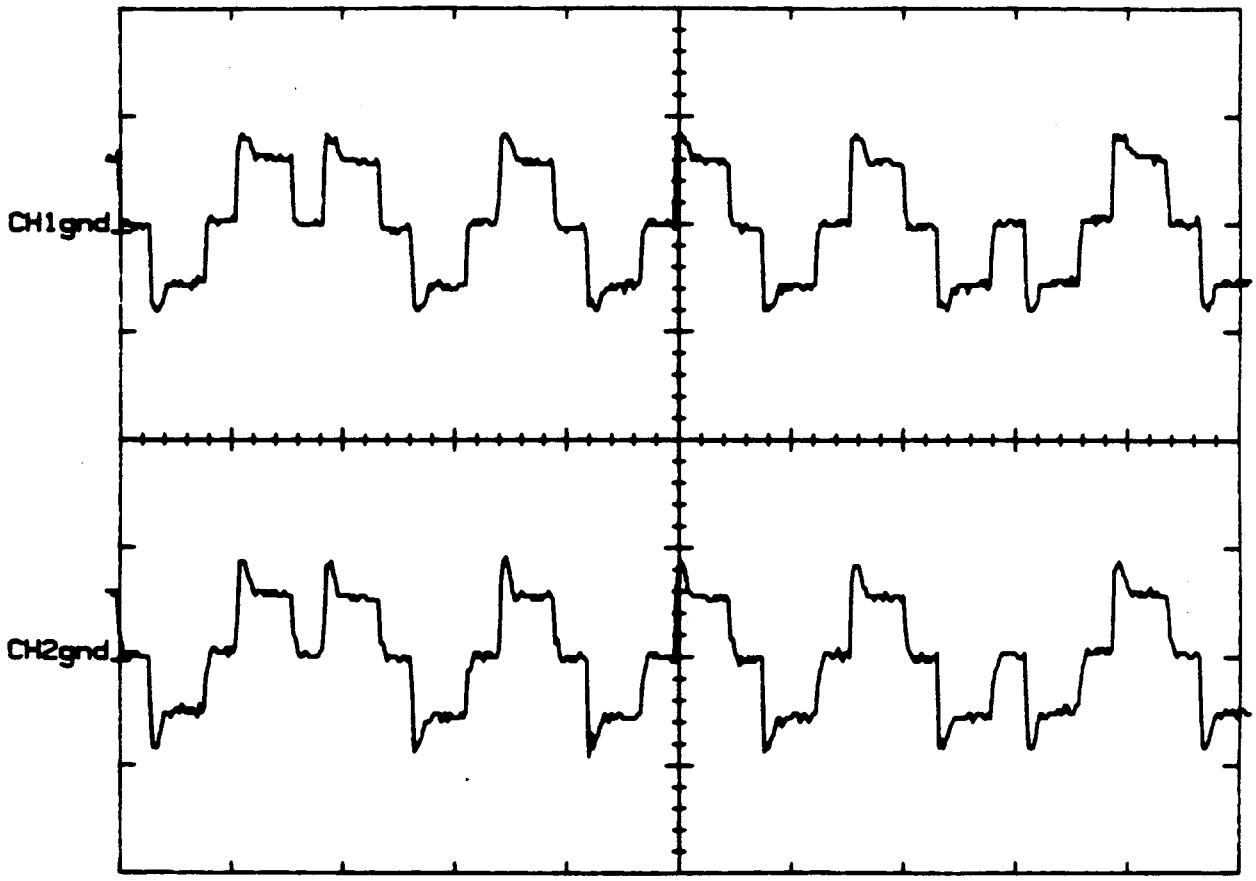


Fig. 20 - Rear View of Synchronization Distribution Expander (J98726W-2) Panel



NOTE: OSCILLOSCOPE SETTING
CH1 5V A 20us
CH2 5V

Fig. 21 - AHG2B TI Main/Auxiliary CC Comparison

F. CHART 6 — AHG10, AHG15 AUXILIARY PANEL EXPANSION

STEP	PROCEDURE

Note: The auxiliary panels must be placed within a six-foot cabling distance from the main panel. The auxiliary panel will consist of either the J98726W-1, J98726W-2, or J98726Y-1 panel, one AHG1 TA, and at least one TD. As an ESD precaution it is recommended that blank board ED-8C715 (or equivalent) be placed in the vacant TI slots of the auxiliary panel. The only requirement for the main panel is that it contain two AHG10 or two AHG15 TI circuit packs and one AHG1 TA circuit pack.

1 Connect the auxiliary panel to the -48 volt battery. Refer to Chart 1 for verification information of the -48 volt battery.

CAUTION: The installation of cabling between the backplanes of the main and auxiliary panels must be done with care and may cause service affecting hits if the main panel is in service. Therefore, it is recommended that the installation be done during off-peak hours.

2 Connect the auxiliary panel to the office alarm. Refer to Chart 2 for verification information of the auxiliary panel alarms.

Note: The cabling between the main and auxiliary panels is identical for the J98726W-1, J98726W-2, and J98726Y-1 panels. The actual wiring is connected between the backplanes of each panel with two separate multi-wire cables Fig. 22. Each cable consists of three 26-gauge twisted pairs in a common shield. One of the cables connects to dedicated output signals from TI-A of the main panel and to TI-A of the auxiliary panel. The other cable connects to dedicated output signals from TI-B of the main panel to TI-B of the auxiliary panel. An individual ground return is carried by the second wire in each pair. The shield for each cable will be connected to frame ground of the main panel but left open at the auxiliary panel.

3 Dress the cables as shown in Fig. 23. Keep all pigtails short (not to exceed 1.5 inches).

Requirement: On the main panel end of the cable pairs, the common ends of each pair along with each cables shield shall be connected together with a crimp eyelet. On the auxiliary panel end of the cable pairs, only the common ends of each pair shall be connected together with a crimp eyelet.

Note: The auxiliary panel connections are given in Table O. The first auxiliary panel is connected by cables A1 and A2 and the second auxiliary panel is connected by cables B1 and B2. The order of installation of the auxiliary panels is as required.

CAUTION: To prevent a signal outage, press the IN TR switch on TI-A and observe the IN SCE LED light on TI-B.

4 Begin the installation of the A (B) cables to the main panel by first connecting the cable eyelet on

STEP	PROCEDURE

the main panel end. The eyelet is connected to the second top backplane screw from the right edge of the backplane as shown in Fig. 20.

5 Repeat the previous Step except connect the cable eyelet on the auxiliary panel end to the auxiliary panel.

6 Connect the A1 (B1) cable to J2 of the main panel. Follow the connections given in Table O.

7 Connect the A1 (B1) cable to J2 of the auxiliary panel. Follow the connections given in Table O.

8 Press the IN TR switch on TI-B.

Requirement: Observe the IN SCE LED light on TI-A.

9 Connect the A2 (B2) cable to J3 of the main panel. Follow the connections given in Table O.

10 Press the IN TR switch on TI-B.

Requirement: Observe the IN SCE LED light on TI-A.

11 Connect the A2 (B2) cable to J3 of the auxiliary panel. Follow the connections given in Table O.

Note 1: At this point, the auxiliary panel is fully connected and ready for operation. The auxiliary panel may accept up to four TD circuit packs and the TD-1 slot must be occupied.

Note 2: The white option plugs allow the AHG1 TA to report alarm information about the corresponding TD slot when in the "IN" position and inhibit alarm information when in the "out" position. The "out" position is designated as the unlabeled position below the "IN" label for each numbered TD. Since there is no option setting for the TD-1 position, a TD must always be used in this slot.

12 Set the options on the AHG1 TA according to the planned TD usage. Refer to Fig. 8.

Requirement: The white option plugs shall be in the "IN" position for each corresponding TD position that is filled. The white option plugs shall be in the unlabeled "out" position for each corresponding TD position that is empty.

13 Insert the AHG1 TA circuit pack into the TA slot on the auxiliary panel.

Requirement: All of the red LEDs on the AHG1 TA will be lighted.

14 Install the TD circuit packs into the TD card slots (leave the TD/S card slots empty if applicable). Refer to the "Circuit Pack Installation" section of Chart 3.

Note 1: If AHG3 TD circuit packs are to be used, use TD-1 slot and then the other TD slots may

STEP	PROCEDURE
	be used. If the AHG4 TD is to be used, it shall be placed in TD-4 slot and additional backplane wiring detailed in Tables A and B must be followed. Also, when the AHG4 TD is used, at least one AHG3 TD must be used starting in TD-1 slot. If an AHG26 TD is to be used, it may be placed in either the TD-1 or TD-4 slots. *Note 2:* The outputs of the two TIs on the main panel connect to all four TD positions on each auxiliary panel. When the circuit packs are first powered up, each TD may latch onto the output from TI-A or TI-B, if both are functioning properly. Only one of the two inputs is used by a TD at a given time. When desired, a nonlocking switch, TR IN SCE, on one of the TIs is operated to provide the input signal source selection.
15	Press the MEM button on the AHG1 TA after all of the TDs have been inserted. *Requirement:* All LEDs on the AHG1 TA will be extinguished. All lamps on the Fuse & Alarm panel will be extinguished.
16	Refer to Chart 3 to verify the output signals of the auxiliary panel.

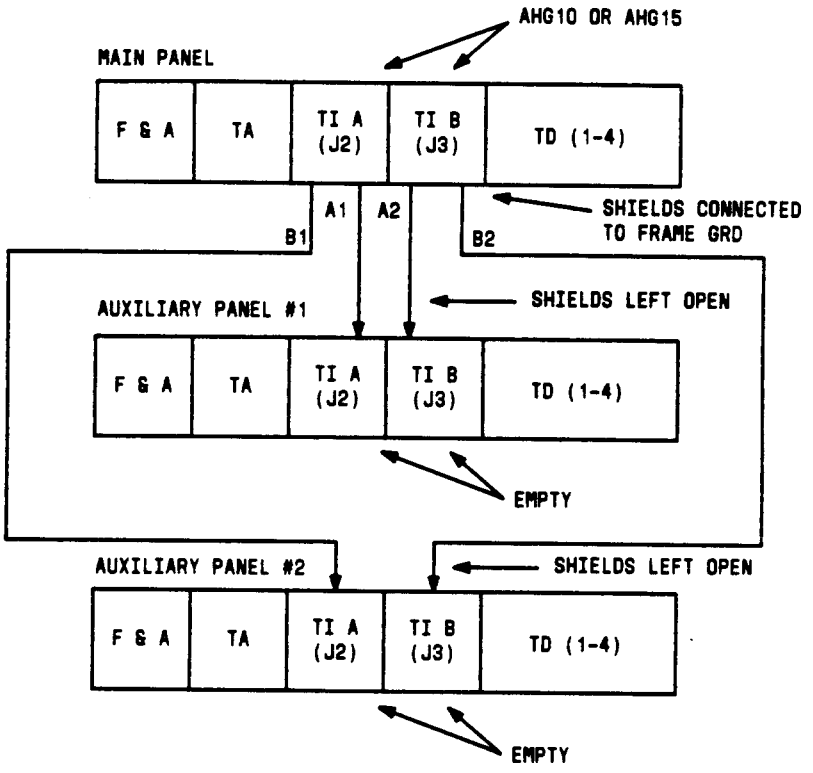


Fig. 22 - Cabling Diagram Showing AHG10 and AHG15 TI-Auxiliary Panel Expansion

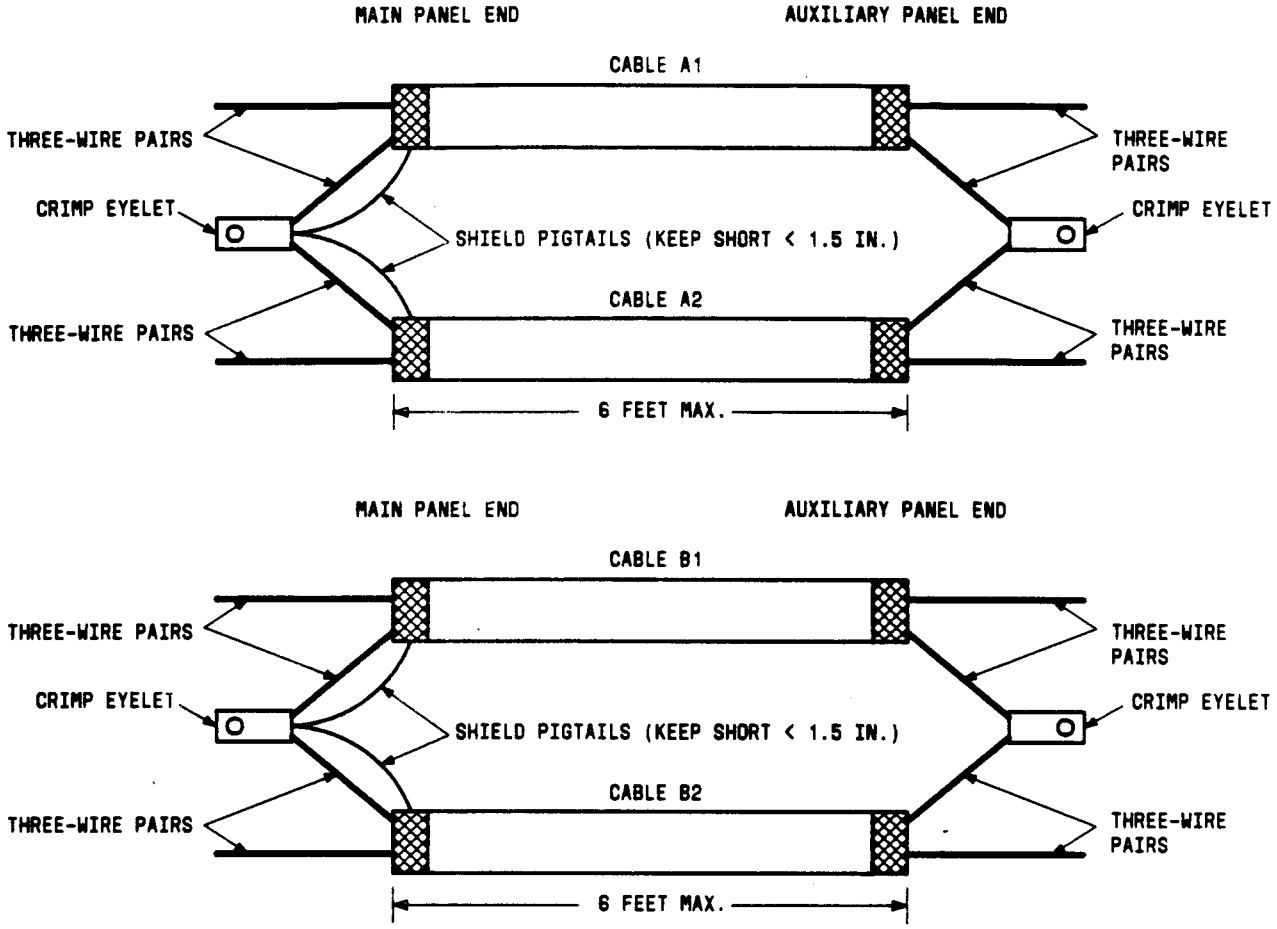


Fig. 23 - Cable Dressing for AHG10 and AHG15 TI-Auxiliary Panels

TABLE O (NOTES 1 , 2, AND 3)

CABLING CONNECTIONS FOR AHG10/15 AUXILIARY PANEL EXPANSION

FROM MAIN PANEL		TO AUXILIARY PANEL #1 (NOTE 3)		
CONNECTOR	TERMINALS	CONNECTOR	TERMINALS	CABLE
J2 (TI-A)	15	J1 (TA)	2	A1
J2 (TI-A)	7	J2 (TI-A)	2,3	A1
J2 (TI-A)	34	J2 (TI-A)	29,30	A1
J3 (TI-B)	15	J1 (TA)	3	A2
J3 (TI-B)	7	J3 (TI-B)	2,3	A2
J3 (TI-B)	34	J3 (TI-B)	29,30	A2
FROM MAIN PANEL		**TO AUXILIARY PANEL #2 (NOTE 3)**		
CONNECTOR	TERMINALS	CONNECTOR	TERMINALS	CABLE
J2 (TI-A)	42	J1 (TA)	2	B1
J2 (TI-A)	8	J2 (TI-A)	2,3	B1
J2 (TI-A)	35	J2 (TI-A)	30	B1
J3 (TI-B)	42	J1 (TA)	3	B2
J3 (TI-B)	8	J3 (TI-B)	2,3	B2
J3 (TI-B)	35	J3 (TI-B)	29,30	B2

*Note 1:*Each auxiliary panel is fed by two shielded cables (A1 and A2 for auxiliary panel #1; and B1 and B2 for auxiliary panel #2). Each cable contains three twisted pairs of 26-gauge wire.

*Note 2:*The shield connection is tied to frame ground on the main panel, but not connected on the auxiliary panel.

*Note 3:*The maximum overall cable length for each auxiliary panel should not exceed 6 feet.

G. CHART 7 — SDE MAINTENANCE AND TROUBLESHOOTING

STEP	PROCEDURE

Note 1: The following is a brief procedure for checking the operation of an in service Synchronization Distribution Expander (SDE). This procedure takes advantage of signals located at test points on the backplane. This test procedure is written for either the J98726W-1, J98726W-2, or J98726Y-1 panels with the following circuit packs: AHG1 (TA); AHG2, AHG2B, or AHG15 (TI); AHG3, AHG4, AHG5, AHG25, or AHG26 (TD).

Note 2: The following test equipment will be needed:

- A dual trace oscilloscope
- A VOM (volt-ohm-milliammeter)
- A frequency counter able to measure to 4.096 MHz with an input impedance of 1 Meg-ohm

Visual Checks

1 Examine the alarm and ACO lamps on the fuse and alarm panel.

Requirement: All lamps shall be dark.

Note: The lamps indicate the real-time status of the SDE. If any lamp is lighted it indicates a potentially service affecting problem. The FA lamp indicates that either one of the fuses is blown or that one of the -48 volt power feeds is dead (J98726W-2 and J98726Z-1 only). The MN lamp indicates that at least one TI has experienced either an input or output signal failure. The MJ lamp indicated that at least one TD has experienced an input signal failure.

2 Press the ACO switch (if not already lighted) located on the fuse and alarm panel.

Requirement: The ACO switch shall light.

3 Press the ACO switch located on the fuse and alarm panel.

Requirement: The ACO switch shall extinguish.

Note: If the ACO switch does not light, replace the bulb in the switch.

4 Examine the LEDs on the TA.

Requirement: These LEDs are intended to record past problems with either the TI or TD circuit packs. Make note of the lighted LEDs as this may indicate a potential problem.

Note: The LED indications on the TA represent either past or present alarms. If the SDE has a past history of alarms, then the appropriate LEDs will be lighted on the TA. To clear these alarm status LEDs, the MEM button on the TA may be pressed. If all TA LEDs do not extinguish after

STEP	PROCEDURE

pressing the MEM button then either a problem with the indicated circuit pack exists, or the appropriate TD option plug for TDs 2-4, are not correctly placed (the TD plugs are placed in the "IN" position when the corresponding position is used and in the "out" (unlabeled) position when the corresponding position is not used.

5 Press the MEM switch on the TA.

Requirement: Any lighted LEDs on the TA shall extinguish. If they do not then either the TA is optioned incorrectly, defective or the SDE is in alarm. Refer to the appropriate Charts for corrective action.

6 Examine the LED indications on the TI circuit packs.

Requirement: Only one IN SCE LED for both TIs (TI-A or TI-B) shall be lighted.

7 Examine the LED indications on each TD circuit pack.

Requirement: Only one LED on each TD shall be lighted.

Power Checks

8 Using the VOM, verify that -48 volts exists at TS 1 between terminals 1 and 2, 3 and 4, 5 and 6. (Terminals 1, 3, and 5 are GRD.)

Requirement: The measured voltage shall be between -41 and -60 volts.

Note: Three separate, independently fused power feeds are recommended for use with the SDE. This ensures power redundancy during a power feed failure. The same practice should extend to any equipment feeding the SDE (ie. bridging repeaters).

System Checks

Note 1: Two input signal sources must be used with an externally synchronized SDE. Diverse inputs are recommended since this ensures against dual input failures. The inputs must be either a pair of:

- DS-1 with either D4 or ESF framing
- DS-1C Mode 2 with either D4 or ESF framing
- Composite Clock (CC)

Note 2: Th. AHG15 TI provides the capability of being directly bridged onto a working DS-1 or DS-1C line. If this option is chosen, two 432 ohm bridging resistors must be placed at the DS-X to provide the monitor level signal to the SDE.

STEP	PROCEDURE

9 Visually verify that two appropriate sources are cabled to TS 2.

Requirement: If a pair of CC signals are used they are cabled to terminals: 1 (T), 2 (R), 3 (GRD) and 6 (T), 7 (R), 8 (GRD). The AHG2B TI requires a phase reversal to provide hitless input switching (ie. 6 (R), 7 (T), 8 (GRD). If a pair of DS-1 or DS-1C inputs are used they are cabled to terminals: 4 (T), 5 (R), 3 (GRD) and 9 (T), 10 (R), 8 (GRD).

Note: The output signals from the SDE originate at the SDE A and SDE B terminal blocks. Each terminal block has 6 rows (labeled A through F) and twenty columns. The A row is frame ground. The B and C rows are tip and ring outputs. The first ten columns of SDE A are connected to the TD-1 position and the second ten to TD-1 position. Likewise, the first ten columns of SDE B are connected to the TD-3 position and the second ten to the TD-4 position. With the exception of the AHG4 and AHG26 TDs, all other TDs use the B and C rows to provide output signals. Only the AHG3 TD are able to take advantage of the cross-connect option where The BK A and BK B terminal blocks are used to provide up to 80 different output arrangements.

10 A check of the validity of the CC outputs may be made by one of the following two methods. If CC inputs are used, they may be directly compared with the outputs. This comparison may be made by using a dual-trace oscilloscope with the following adjustments:

- Channels 1 and 2 set to 5V/DIV, DC coupling, ALT
- Time base set to 20 μs/DIV
- Trigger set to Channel 1, AC coupling, AUTO

11 Connect Channel 1 to TS2 at terminal 2 and the probe's ground to terminal 1. Connect Channel 2 to the C1 terminal on SDE A terminal block and the probe's ground to B1. Adjust the trigger level for a stable trace.

Requirement: The waveforms will be stationary with respect to each other.

12 Repeat the previous Step but connect Channel 1 to TS2 terminal 7 and ground to terminal 6.

CAUTION: The following Step will be service affecting and should only be done during off-peak hours.

13 If DS-1 or DS-1C inputs are used, the frequency of each TI's the CC generating circuitry may be compared or measured. If the AHG2 or AHG2B TIs are used, this operation may be done by using a dual-trace oscilloscope with the following adjustments:

- Channels 1 and 2 set to 5V/DIV, DC coupling, ALT
- Time base set to 5μs/DIV (AHG2 and AHG2B TI)
- Trigger set to Channel 1, AC coupling, AUTO

STEP	PROCEDURE
14	Connect Channel 1 to TI-A test points as follows: • AHG2 - Terminal 41 of J2 • AHG2B - Terminal 5 of J2 Connect the probe's shield to frame ground.
15	Connect Channel 2 to TI-B test points as follows: • AHG2 - Terminal 41 of J3 • AHG2B - Terminal 5 of J3 Connect the probe's shield to frame ground.
16	Examine the two traces on the oscilloscope. ***Requirement:*** Two 256 kHz square waves should be visible. There should be no rolling or cycle slipping between the two square waves.
17	If the AHG15 TIs are used, this clock frequency may be directly measured at the TST faceplate pin jack with a frequency counter. The frequency will be a 4.096 MHz square wave. The frequency counter's probe should be connected via a pin plug to the TST jack of TI-A and the probe's shield connected to the faceplate latch. ***Requirement:*** The resulting frequency shall be 4.096 MHz +/- 1 Hz.
18	Repeat the above Step for the AHG15 TI IN TI-B slot.
19	Remove the DS-1 or 1C inputs to the TIs and then restore them. Wait approximately 45 seconds and then repeat the previous frequency evaluation Steps for the AHG2 or AHG2B TI (Step 16) or AHG15 TI (Steps 17 and 18).
20	If using the AHG26 TD connect a frequency counter to the 2.048 MHz +10 dBm faceplate jack. Use a bantam plug to obtain access to the tip (Probe) and ring (Shield) connections. Measure across a 75 ohm resistor for proper termination. ***Requirement:*** A frequency of 2.048 MHz +/- 1 Hz shall be measured.
21	Remove the frequency counter leads, terminating resistor, and bantam plug. **Troubleshooting the Signal Path** *Note 1:* SDE signal failures may occur in three possible places: • At the input of each TI circuit pack • Between the TI and TD circuit packs

STEP	PROCEDURE

- At the output(s) of the TD circuit packs

Note 2: Measurements made with an oscilloscope may be used to determine where the problem is and how to correct it. Since the SDE uses circuit pack modularity, circuit pack replacement rather than repair is recommended.

Note 3: The following steps will verify the input signals to the following TI circuit packs. AHG2, AHG2B, AHG10, and AHG15.

CAUTION: The following procedure deals with the measurement of critical backplane signals. As disruption of these signals may cause a temporary loss of service, it is recommended that this procedure be done during off peak hours.

22 Set up a dual-trace oscilloscope for differential measurements with Channel 2 added and inverted using an internal trigger.

- Set Channels 1 and 2 to 2V/DIV (DS-1/1C norm) or 5V/DIV (CC) or
- Channel 2 invert
- Set the time base to 1 μs/DIV (DS-1) or .5 μs/DIV (DS-1C) or 20 μs/DIV (CC).

23 Connect the probes of the dual-channel oscilloscope across the input tip and ring points of TS 2. As long as TI circuit packs are in the panel, no terminating resistor is necessary. Connect ground leads of the probes to frame ground.

Requirement: If the input waveform is a CC signal, the waveform will match one of the waveforms shown in Figs. 5A, 5B, 5C, or 5D. If the input waveform is a DS-1 signal, the waveform will match either Fig. 6A or 6B. If the input waveform is a DS-1C signal, the waveform will match either Fig. 7A or 7B.

Timing Signal Evaluation

Note: The next series of tests will evaluate the timing signals between the TI and TD circuit packs. These signals are dual-rail unipolar composite clock in format. The AHG10 and AHG15 TIs have output sensing circuits that determine if these signals are good. The AHG10 and AHG15 also have this capability for the separate auxiliary panel outputs.

24 Set up a dual-trace oscilloscope for differential measurements with Channel 2 added and inverted using an internal trigger.

- Set Channels 1 and 2 to 2V/DIV
- Channel 2 invert
- Set the time base to 20 μs/DIV

STEP	PROCEDURE
25	Connect the Channels 1 and 2 to the NR1 and PR1 terminals (2 and 29 respectively) of J2 (TI-A). The shield leads shall connect to frame ground. ***Requirement:*** The waveform should match Fig. 24.
26	Connect the Channels 1 and 2 to the NR1 and PR1 terminals (2 and 29 respectively) of J3 (TI-B). The shield leads shall connect to frame ground. ***Requirement:*** The waveform should match Fig. 24.
27	Connect the Channels 1 and 2 to the NR2 and PR2 terminals (3 and 30 respectively) of J2 (TI-A). The shield leads shall connect to frame ground. ***Requirement:*** The waveform should match Fig. 24.
28	Connect the Channels 1 and 2 to the NR2 and PR2 terminals (3 and 30 respectively) of J3 (TI-B). The shield leads shall connect to frame ground. ***Requirement:*** The waveform should match Fig. 24. *Note:* If the AHG10 or AHG15 TIs are used, the next four Steps should be followed to verify the dedicated outputs to the auxiliary panel.
29	Connect the Channels 1 and 2 to the NR3 and PR3 terminals (7 and 34 respectively) of J2 (TI-A). The shield leads shall connect to frame ground. ***Requirement:*** The waveform should match Fig. 24.
30	Connect the Channels 1 and 2 to the NR3 and PR3 terminals (7 and 34 respectively) of J3 (TI-B). The shield leads shall connect to frame ground. ***Requirement:*** The waveform should match Fig. 24.
31	Connect the Channels 1 and 2 to the NR4 and PR4 terminals (8 and 35 respectively) of J2 (TI-A). The shield leads shall connect to frame ground. ***Requirement:*** The waveform should match Fig. 24.
32	Connect the Channels 1 and 2 to the NR4 and PR4 terminals (8 and 35 respectively) of J3 (TI-B). The shield leads shall connect to frame ground. ***Requirement:*** The waveform should match Fig. 24.

STEP	PROCEDURE

Timing Signal Output Evaluation

Note 1: The next series of tests will evaluate the timing signals output by the TD circuit packs.

Note 2: Proper evaluation of the SDE's working outputs may not be accurately done at the SDE ( ) terminal block access. Transmission line characteristics allow only an accurate evaluation of output signal to be made at the destination. The following tests assume that measurements will be made at the network element (NE) terminating the signal.

CAUTION: Caution must be observed while taking these measurements as working systems are involved.

33 If the AHG3 output(s) are to be examined, set-up an oscilloscope to view the waveform at the NE. The dual-trace oscilloscope will be set for differential measurements with Channel 2 added and inverted using an internal trigger.

- Set Channels 1 and 2 to 5V/DIV.
- Channel 2 invert
- Set the time base to 20 μs/DIV

Requirement: Depending on the cabling distance, the waveform shall match Fig. 5 (A,B,C,orD).

34 If the AHG5/25 TD output(s) are to be examined, set-up an oscilloscope to view the waveform at the terminating NE. The dual-trace oscilloscope will be set for differential measurements with Channel 2 added and inverted using an internal trigger.

- Set Channels 1 and 2 to 2V/DIV
- Channel 2 invert
- Set the time base to 1 μs/DIV.

35 Connect Channel 1 to Tip and Channel 2 to Ring. The probe's shields shall be tied to frame ground.

Requirement: Depending on the cabling distance, the waveform shall match either Fig. 14.

36 If problems persist with the AHG5/25 TD output(s), a DS-1 analyzer will need to be used. Set the analyzer to monitor framing and data pattern.

Requirement: The framing should be either D4 or ESF (depending on the AHG5/25 option) and the data pattern shall be all ones.

37 If the AHG4 or AHG26 TD output(s) are to be directly examined a frequency selectable voltmeter will need to be used. Because of the extremely low level signals, care must be exercised in taking the measurement.

STEP	PROCEDURE
38	Set the frequency selective voltmeter for the center frequency required by the terminating NE (2.048 MHz or 512 kHz or 64 kHz). ***Requirement:*** The resulting level shall be within the specifications for the terminating NE. Acceptable ranges for the NE's inputs are as follows: • 2.048 MHz -20 to -30 dBm (OMFS) • 2.048 MHz -35 to -45 dBm (Distribution Hybrid Tree) • 512 kHz -23 to -33 dBm • 64 kHz -54 to -64 dBm *Note 1:* 728A type cable is recommended for use with the AHG26 TD. This cable has an attenuation of .34 dB per 100 feet @ 2.048 MHz. A maximum cabling distance of 1500 feet is recommended. *Note 2:* 22BF type cable is recommended for use with the AHG4 TD. This cable has an attenuation of .35 dB per 100 feet @ 512 kHz. A maximum cabling distance of 1000 feet is recommended. *Note 3:* If troubles are incurred that cannot be cleared, notify the AT&T Technologies installation force or your supervisor.

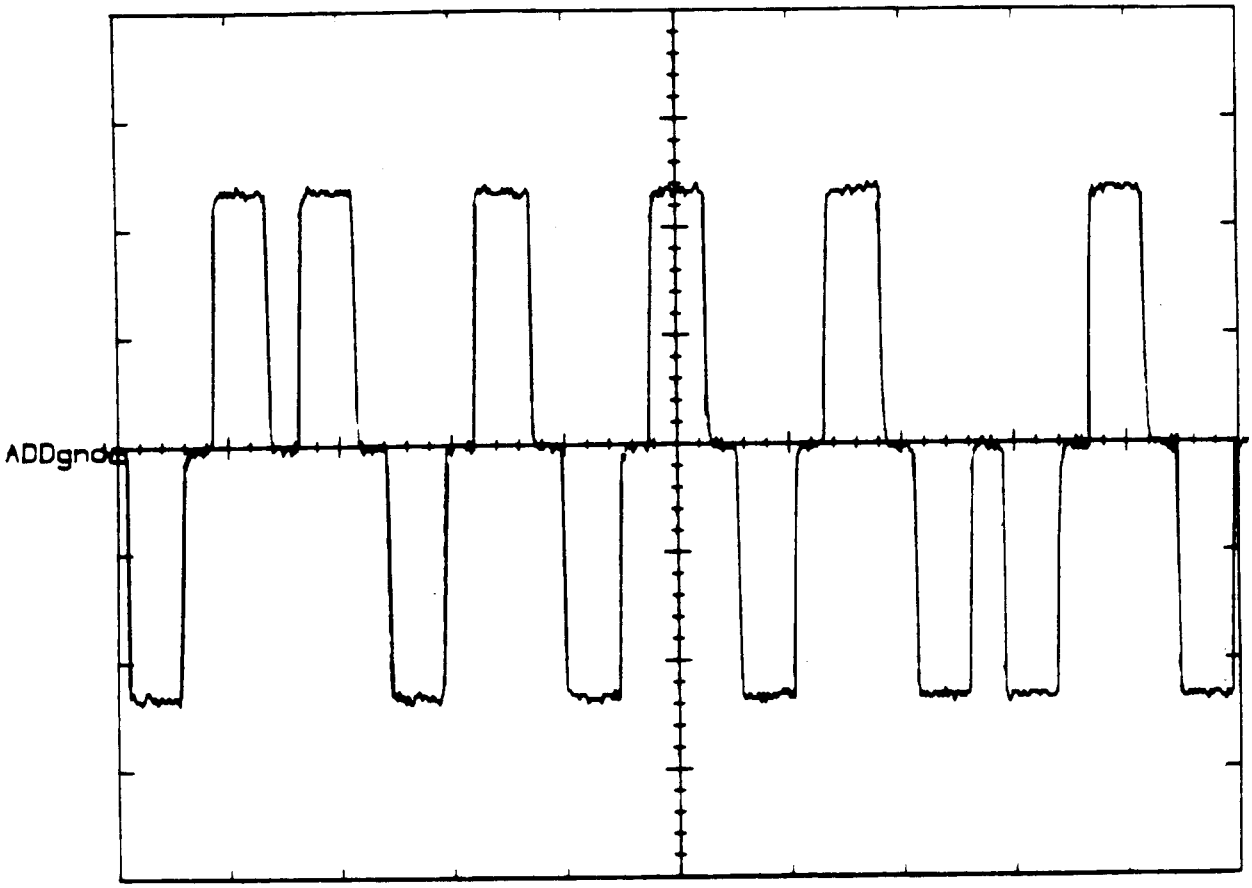


Fig. 24 - Dual-Rail Unipolar Backplane Signal

2. CLEI CODES FOR SDE CIRCUIT PACKS AND PANELS

PACK	*CLEI*
AHG1	D4PQ100AXX
AHG2	D4PQ101AXX
AHG2B	D4PQ103AXX
AHG3	D4PQ102AXX
AHG4	D4PQ107AXX
AHG10	D4PQ108AXX
AHG5	D4PQ110AXX
AHG15	D4PQ111AXX
AHG25	D4PQ115AXX
AHG26	D4PQ118AXX

PANEL	*CLEI*
J98726W-2	D4ME1A0B
J98726Y-1	D4ME1D0B

3. GLOSSARY

TERM	*DEFINITION*
ACO	Alarm Cut Off
BK	Block
BR	Bridging Option
CC	Composite Clock
CDU	Clock Distribution Unit (J98726Z-1)
CTS	Composite Timing Signal
DDS	Digital Data System
ESD	Electro-Static Discharge
ESF	Extended Super Frame
F&A Panel	Fuse and Alarm Panel
FR	Free Run
HO	Holdover
IN FAIL	Input Failure
IN SCE TR	Input Source Transfer
LED	Light Emitting Diode
MEM	Memory Reset Switch (AHG1 TA)
NE	Network Element
OMFS	Office Master Frequency Supply
PFS	Primary Frequency Supply
PLL	Phase-Locked Loop
R	Ring
SDE	Synchronization Distribution Expander
T	Tip
TA	Timing Alarm Circuit Pack
TD	Timing Distributor Circuit Pack
TI	Timing Interface Circuit Pack
TS	Terminal Strip
TST	Test Access Jack
4ESS	Number 4 Electronic Switching System

4. REFERENCES

4.01 The following publications provide more information on the SDE.

- SD-7C389-02 Issue 3 (or higher)
- T-7C3890-33 Issue 4 (or higher)
- 314-913-220 – Description and Operation
- 314-913-222 – Data Sheet – AHG1 Timing Alarm
- 314-913-226 – Data Sheet – AHG3 Timing Distributor
- 314-913-223 – Data Sheet – AHG4 Timing Distributor
- 314-913-227 – Data Sheet – AHG5 Timing Distributor
- 314-913-224 – Data Sheet – AHG10 Timing Interface
- 314-913-229 – Data Sheet – AHG15 Timing Interface
- 314-913-228 – Data Sheet – AHG25 Timing Distributor
- 314-813-103 – Data Sheet – AHG26 Timing Distributor

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