DIGITAL DATA SYSTEM

SECONDARY TIMING SUPPLY

TESTS

CONTENTS PAGE

1. GENERAL

1.01 This section provides installation and maintenance test procedures for the Digital Data System (DDS) secondary timing supply (STS).

1.02 This section is reissued to add information defining the purpose of the signal tracing tests that require the use of the oscilloscope. Revision arrows are used to emphasize the more significant changes.

2. APPARATUS

2.01 The following test equipment is required to perform the test procedures in this section:

1—General purpose oscilloscope

Note: ▶This oscilloscope is used only to perform signal tracing tests (see 6.01).◀

2—Special test cords with P-11H966 terminal assemblies on each end

2—P-11H966 terminal assemblies.

3. INITIAL TEST

3.01 The following test is used to confirm that the newly installed STS is working properly. This test is performed only after the initialization procedure for initial startup, located in Section 314-913-315, has been completed.

STEP	PROCEDURE
	Note: Verify that input selector (IS) switch on display and control unit is in AUTO position.
1	Depress NORM control key.
2	Momentarily depress RESET control key.
	Requirement: The MJ and MN lamps are off. All red LEDs are off. Either A ON or B ON LED, but not both, is lighted. One and only one of the following pairs of LEDs is lighted: A-A and A-B; B-A and B-B. The other pair of LEDs is off.

4. PHASE METERING CIRCUIT CHECKOUT

4.01 ♦The following procedure is used to check out the phase metering circuit (PMC), circuit pack (CP) HL57, to ensure that it is operating properly before it is used in any of the succeeding procedures.♦

STEP	PROCEDURE
	Note: To ensure proper connection between the P-11H966 terminal assembly and CP, terminal assembly ***must*** be inserted into test point (TP) with metal strip facing to the right.
1	Insert a special test cord equipped with a P-11H966 terminal assembly on each end from TP 1 (IN1) on CP HL57 to TP 11 on CP HL54B of phase-locked loop monitor A (PLLM-A) and set switch S1 on CP HL57 to negative (-) position.
	Requirement: The invalid (INV) LED is lighted.
2	Insert a second special test cord from TP 7 (IN2) on CP HL57 to TP 2 on CP HL54B of PLLM-A and set switch S2 on CP HL57 to positive (+) position.
	Requirement: The INV LED is off; and number 00, 01, or 02 appears on numerical display.
	Note: If phase-locked loop A (PLL-A) is suspected of being faulty or if PLL-A OFF LED is lighted, repeat Steps 1 and 2 with the test cords inserted in TPS of CP HL54B of PLLM-B. If checkout fails, problem may be in PMC.

5. PHASE BUILD-OUT PROCEDURE

5.01 The following procedure uses the PMC, CP HL57, to measure the phase between timing supply interface unit A (TSIU-A) and TSIU-B. The phase difference is measured in 1/64 of a cycle between the two 8-kHz signals connected to the meter. The phase difference is displayed as a decimal number between 00 and 64 on the phase metering numerical display on the display panel. The readings are circular; ie, the next higher number after 64 is 00 again. A reading of 64 is considered equivalent to a reading of 00.

5.02 The phase difference can be measured between either the positive or negative transition of one input and either the positive or negative transition of the other input. The transitions to be used are selected by switches S1 and S2. Inputs to the PMC are made via TP 1 (IN1) and TP 7 (IN2) on the faceplate of the circuit pack.

STEP	PROCEDURE
	Note: To ensure proper connection between the P-11H966 terminal assembly and CP, terminal standby ***must*** be inserted into TP with metal strip facing to the right.
1	Perform checkout procedure, located in Part 4, on PMC, CP HL57.
2	Turn IS switch to select TSIU-B.

STEP	PROCEDURE

Requirement: The B ON LED is lighted.

3 Adjust phase build-out switch of TSIU-A, CP HL65, to position 6.

Note 1: If position 6 is not labeled, turn phase build-out switch to position 1 and then turn it five positions counterclockwise. This is position 6.

Note 2: During normal operation, position of phase build-out switch on each TSIU is never changed. It is to be changed only when this procedure is used. Also, phase build-out switch is difficult to turn; this is normal.

4 Turn IS switch to select TSIU-A.

Requirement: The A ON LED is lighted.

5 Move both transition switches (S1 and S2) on CP HL57 to positive (+) position.

6 Insert a special test cord from TP 1 (IN1) on CP HL57 to TP 6 on CP HL65 of TSIU-A.

Requirement: The INV LED is lighted.

7 Insert another special test cord from TP 7 (IN2) on CP HL57 to TP 6 on CP HL65 of TSIU-B.

Requirement: A number from 00 to 64 appears on numerical display. The INV LED is off.

Note: If INV LED remains lighted and numerical display is blanked, one of input signals is not an 8-kHz signal. Recheck to be sure that correct TPs and CPs have been selected.

8 While observing numerical display, rotate phase build-out switch on CP HL65 of TSIU-B until a reading of 00 or 64 is obtained.

Note: If a reading of 00 or 64 cannot be obtained, reading closest to 00 or 64 should be used. For example, if a reading of 04 is obtained and one more turn of phase build-out switch gives a reading of 62, then 62 should be used since it is closer to 64 than 04 is to 00.

9 Remove special test cords from circuit pack TPs.

Requirement: The numerical display is blanked and INV LED is off.

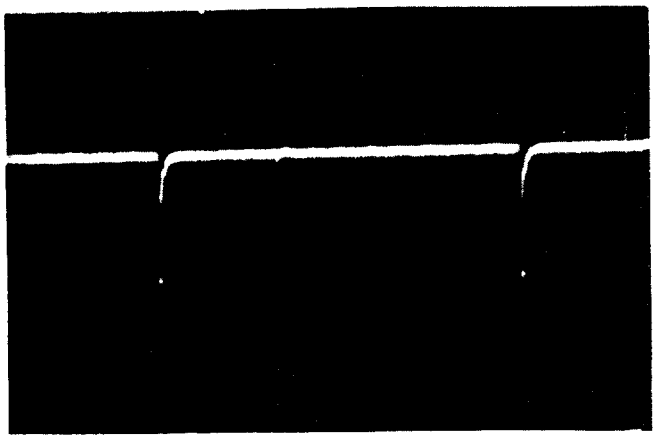
10 Turn IS switch to AUTO position.

Requirement: The A ON LED remains lighted.

6. WAVEFORMS

6.01 ▮The following oscilloscope waveforms can aid in locating a trouble condition in an STS that cannot be located by using the troubleshooting flowcharts in Section 314-913-315. The trouble can normally be isolated to a connection or wire between CPs. This signal tracing approach requires the use of the oscilloscope. P-11H966 terminal assemblies are used to gain access to the circuit pack test points.▮

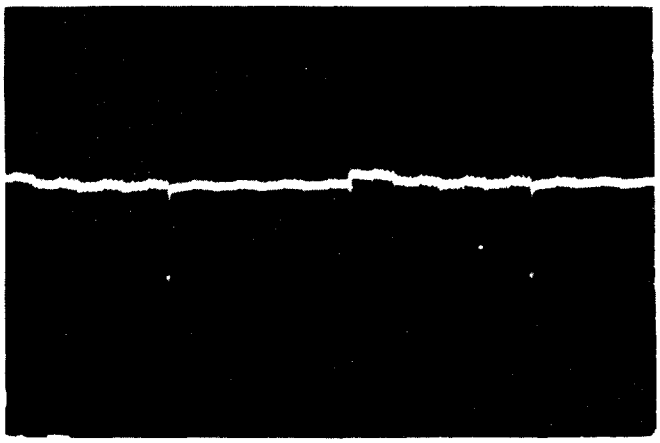
6.02 Waveform A is the 8-kHz F-bit signal derived by each TSIU. The pulse occurs once every 125 μs and has a pulse width of 0.5 μs. This waveform can be observed at TP 6 on CP HL65 of each TSIU. TP 12 on CP HL65 is ground.



HORIZONTAL SCALE: 20 μS/DIV
VERTICAL SCALE: 2 V/DIV

Fig. 1—Waveform A

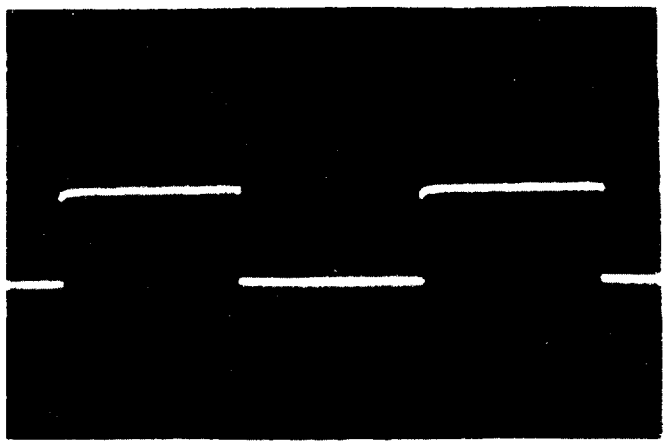
6.03 Waveform B is the 8-kHz F-bit signal received by each PLL. This waveform can be observed at TP 6 on CP HL53 of each PLL. TP 12 on CP HL53 is ground.



HORIZONTAL SCALE: 20 μS/DIV
VERTICAL SCALE: 2 V/DIV

Fig. 2—Waveform B

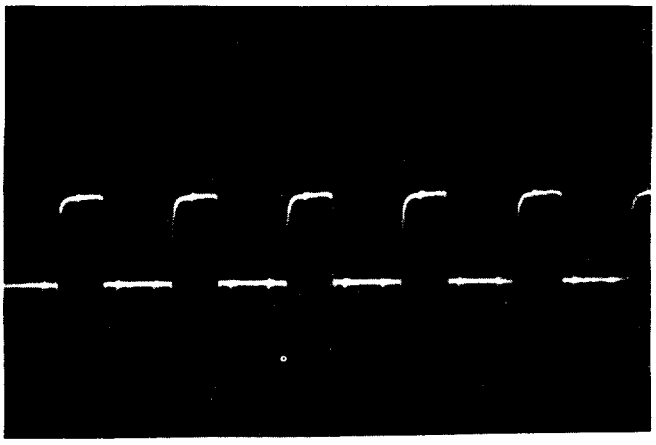
6.04 Waveform C is the 8-kHz signal supplied to the timing supply output circuits (TSOCs) by the PLL. The pulse occurs once every 125 μs. This waveform can be observed at TP 1 on CP HL53 of each PLL. TP 12 on CP HL53 is ground.



HORIZONTAL SCALE: 20 μS/DIV
VERTICAL SCALE: 2 V/DIV

Fig. 3—Waveform C

6.05 Waveform D is the 512-kHz signal supplied to the TSOCs by the PLL. The pulse occurs approximately once every 1.95 μs. Notice that the waveform stays at 0 voltage for a larger percentage of the duty cycle than it stays at the high voltage. This is a normal condition. This waveform can be observed at TP 4 on CP HL53 of each PLL. TP 12 on CP HL53 is ground.



HORIZONTAL SCALE: 1 μS/DIV
VERTICAL SCALE: 2 V/DIV

Fig. 4—Waveform D