DIGITAL DATA SYSTEM
LOCAL TIMING SUPPLY
TESTS

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1. GENERAL

1.01 This section provides installation and maintenance test procedures for the Digital Data System (DDS) local timing supply (LTS).

1.02 This section is reissued to add information defining the purpose of the signal tracing tests that require the use of the oscilloscope and rate the LTS manufacture discontinued. Revision arrows are used to emphasize the more significant changes.

2. APPARATUS

2.01 The following test equipment is required to perform the test procedures in this section:

1—General purpose oscilloscope

▶*Note:* This oscilloscope is used only to perform signal tracing tests (see 5.01).◀

2—Special test cords with P-11H966 terminal assemblies on each end

1—Phase metering circuit (circuit pack HL57), if not already provided

2—P-11H966 terminal assemblies.

3. PHASE METERING CIRCUIT CHECKOUT

3.01 ▶The following procedure is used to check out the phase metering circuit (PMC), circuit pack (CP) HL57, to ensure that it is operating properly before it is used in any of the succeeding procedures.◀

STEP	PROCEDURE
	Note: To ensure proper connection between P-11H966 terminal assembly and CP terminal assembly ***must*** be inserted into test point (TP) with metal strip facing to the right.
1	Insert a special test cord from TP 1 (IN1) of PMC, CP HL57, to TP 11 on CP HL54 or HL54B of phase-locked loop monitor A (PLLM-A) and set switch S1 of PMC to negative (-) position.
	Requirement: The invalid (INV) LED is lighted.

STEP	PROCEDURE
2	Insert a special test cord from TP 7 (IN2) on CP HL57 to TP 2 on CP HL54 or HL54B of PLLM-A and set switch S2 on CP HL57 to positive (+) position. ***Requirement:*** The INV LED is off; and number 00, 01, or 02 appears on numerical display. ***Note:*** If PLL-A is suspected of being faulty or if PLL-A OFF LED is lighted, insert test cords into PLLM-B and perform checkout. If checkout fails, problem may be in PMC.

4. PHASE BUILD-OUT PROCEDURE

4.01 The following procedure uses the PMC, CP HL57, to measure the phase between timing supply interface—unit A (TSIU-A) and TSIU-B. The phase difference is displayed as a decimal number between 00 and 64 on the phase metering numerical display on the display panel. ⧫The decimal number represents the phase difference measured in 1/64 of a cycle between the two 8- kHz signals connected to the meter. The readings are circular; ie, the next higher number after 64 is 00 again. A reading of 64 is considered equivalent to 00.⧫

4.02 The phase difference can be measured between either the positive or negative transition of one input and either the positive or negative transition of the other input. The transitions to be used are selected by switches S1 and S2. Inputs to the PMC are made via TP 1 (IN1) and TP 7 (IN2) on the faceplate of the CP.

STEP	PROCEDURE
	Note: To ensure proper connection between P-11H966 terminal assembly and CP, terminal assembly ***must*** be inserted into TP with metal strip facing to the right.
1	Perform checkout procedure, located in Part 3, on PMC, CP HL57.
2	Turn input selector (IS) switch to select TSIU-B. ***Requirement:*** The B ON LED is lighted.
3	Adjust phase build-out switch of TSIU-A, CP HL65, to position 6. ***Note 1:*** If position 6 is not labeled, turn phase build-out switch to position 1 and then turn it five positions counterclockwise. This is position 6. ***Note 2:*** During normal operation, position of phase build-out switch on each TSIU is never changed. It is to be changed only when this procedure is used. Also, phase build-out switch is difficult to turn; this is normal.
4	Turn IS switch to select TSIU-A. ***Requirement:*** The A ON LED is lighted.

STEP	PROCEDURE
5	Move both transition switches (S1 and S2) on CP HL57 of PMC to positive (+) position.
6	Insert a special test cord from TP 1 (IN1) on CP HL57 to TP 6 of TSIU-A. ***Requirement:*** The INV LED is lighted.
7	Insert another special test cord from TP 7 (IN2) on CP HL57 to TP 6 of TSIU-B, CP HL65. ***Requirement:*** A number from 00 to 64 appears on numerical display. The INV LED is off. ***Note:*** If INV LED remains lighted and numerical display is blanked, one of the input signals is not an 8-kHz signal. Recheck to be sure that correct TPs and CPs have been selected.
8	While observing the numerical display, rotate phase build-out switch on TSIU-B until a reading of 00 or 64 is obtained. ***Note:*** If a reading of 00 or 64 cannot be obtained, reading closest to 00 or 64 should be used. For example, if a reading of 04 is obtained and one more turn of phase build-out switch gives a reading of 62, then 62 should be used since it is closer to 64 than 04 is to 00.
9	Remove special test cords from CPs. ***Requirement:*** The numerical display is blanked and INV LED is off.
10	Turn IS switch to AUTO position. ***Requirement:*** The A ON LED remains lighted.

5. TESTS

5.01 ♦The following tests can aid in locating a trouble condition in a LTS that cannot be located by using the troubleshooting flowcharts in Section 314-913-320. The trouble can normally be isolated to a connector or wire between CPs. This signal tracing approach requires the use of the oscilloscope. The P-11H966 terminal assemblies are used to gain access to the appropriate test points.♦

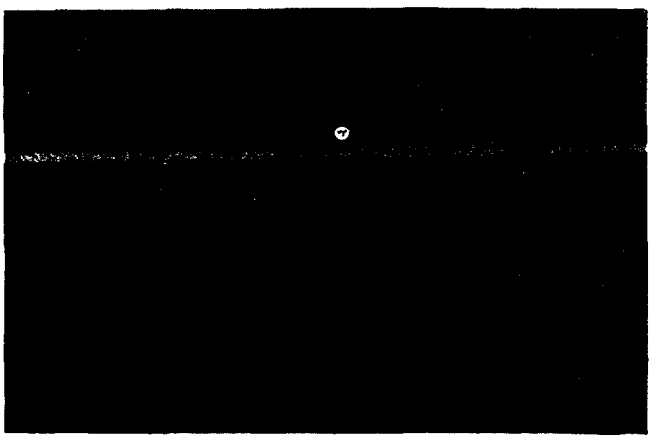
STEP	PROCEDURE
	Note: To ensure proper connection between the P-11H966 terminal assembly and CP, terminal assembly ***must*** be inserted into TP with metal strip facing to the right.
1	Set oscilloscope to a horizontal scale of 20 microseconds per division (μs/div) and a vertical scale of 2 volts per division (V/div).

STEP	PROCEDURE
2	Check TP 6 of each TSIU, CP HL65. ***Requirement:*** A waveform similar to waveform A (Fig. 1) in Part 6 of this section is seen at each TP.
3	With oscilloscope at same setting, check TP 6 of each phase-locked loop (PLL), CP HL53. ***Requirement:*** A waveform similar to waveform B (Fig. 2) in Part 6 is seen at each TP.
4	With oscilloscope at same setting, check TP 1 of each PLL. ***Requirement:*** A waveform similar to waveform C (Fig. 3) in Part 6 is seen at each TP.
5	Change oscilloscope setting to a horizontal scale of 1 μs/div and a vertical scale of 2 V/div.
6	Check TP 4 of each PLL. ***Requirement:*** A waveform similar to waveform D (Fig. 6) in Part 4 is seen at each TP.
7	Reset oscilloscope to a horizontal scale of 20 μs/div and a vertical scale of 2 V/div.
8	Check TP 3 of each timing supply output circuit (TSOC), CP HL59. ***Requirement:*** A waveform of some type is seen at each TP; ie, a steady 0 volts or a steady +4 volts is not present.
9	With oscilloscope at same setting, check TP 1 of each TSOC. ***Requirement:*** A waveform of some type is seen at each TP; ie, a steady 0 volts or a steady +4 volts is not present.
10	With oscilloscope at same setting, check TP 10 of each clock line driver (CLD), CP HL52. ***Requirement:*** A waveform similar to waveform E (Fig. 5) in Part 6 is seen at each TP.
11	Change oscilloscope setting to a horizontal scale of 4 μs/div and a vertical scale of 2 V/div.
12	Check TP 9 of each CLD. ***Requirement:*** A waveform similar to waveform F (Fig. 6) in Part 6 is seen at each TP.

6. WAVEFORMS

6.01 The following oscilloscope waveforms are used in conjunction with the tests contained in this section.

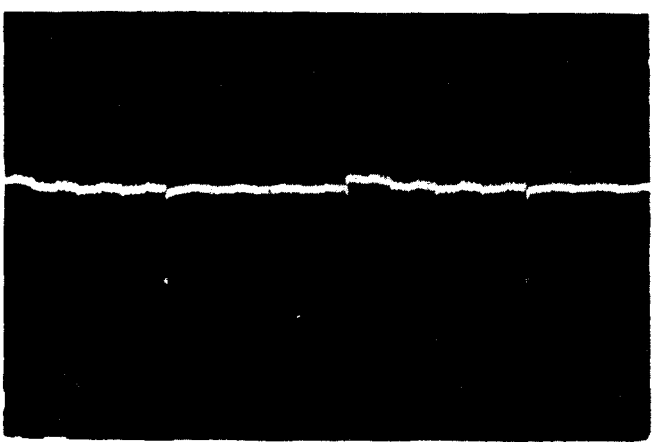
6.02 Waveform A is the 8-kHz F-bit signal derived by each TSIC. The pulse occurs once every 125 μs and has a pulse width of 0.5 μs.



HORIZONTAL SCALE: 20 μS/DIV
VERTICAL SCALE: 2 V/DIV

Fig. 1—Waveform A

6.03 Waveform B is the 8-kHz F-bit signal received by each PLL.



HORIZONTAL SCALE: 20 μS/DIV
VERTICAL SCALE: 2 V/DIV

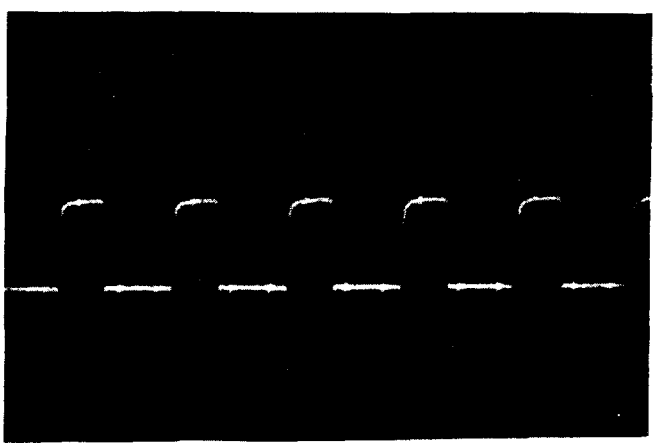
Fig. 2—Waveform B

6.04 Waveform C is the 8-kHz signal supplied to the TSOCs by the PLL. The pulse occurs once every 125 μs.

HORIZONTAL SCALE: 20 μS/DIV
VERTICAL SCALE: 2 V/DIV

Fig. 3—Waveform C

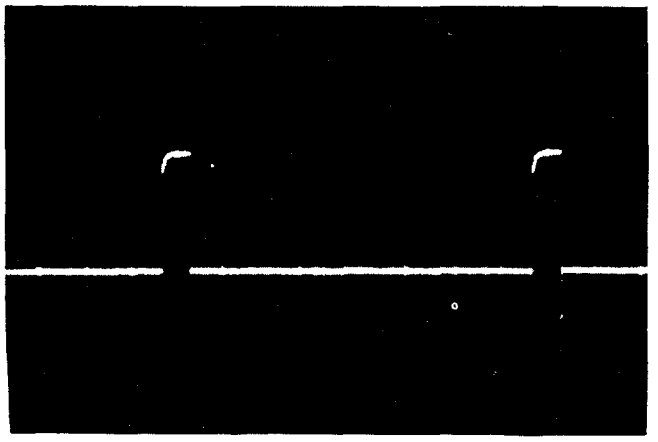
6.05 Waveform D is the 512-kHz signal supplied to the TSOCs by the PLL. The pulse occurs approximately once every 1.95μs. Notice that the waveform stays at 0 voltage for a larger percentage of the duty cycle than it stays at the high voltage. This is a normal condition.



HORIZONTAL SCALE: 1 μS/DIV
VERTICAL SCALE: 2 V/DIV

Fig. 4—Waveform D

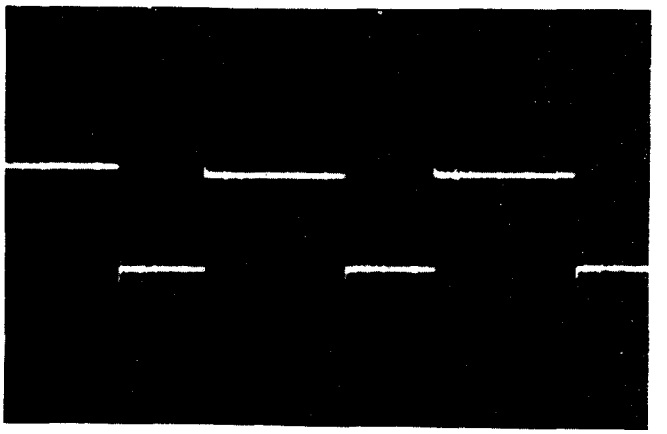
6.06 Waveform E is the reconstructed 8-kHz signal developed by the line terminator (LT). Each pulse occurs once every 125 μs.



HORIZONTAL SCALE: 20 μS/DIV
VERTICAL SCALE: 2 V/DIV

Fig. 5—Waveform E

6.07 Waveform F is the reconstructed 64-kHz signal developed by the LT. Each pulse occurs once every 15.6 μs.



HORIZONTAL SCALE: 4 μS/DIV
VERTICAL SCALE: 2 V/DIV

Fig. 6—Waveform F