MULTIPOINT JUNCTION UNITS AND AUXILIARY CIRCUITS

DESCRIPTION

DIGITAL DATA SYSTEM

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1. GENERAL

1.01 This practice contains the physical and functional descriptions of an FDX MJU (full-duplex multipoint junction unit, or referred to as an MJU), network, and associated circuits. Also provided is a description of an FDX MJU HL223 and HL224. The HL223 and HL224 CPs (circuit packs) are required for secondary channel capability.

1.02 This practice is reissued to include information on the new secondary channel HL223 and HL224 circuit packs. Revision arrows are used to emphasize the more significant changes.

1.03 A multipoint network is composed of any number of outlying stations and a common control point, connected together by means of MJUs. Figure 1 shows a typical FDX multipoint network containing three MJUs. The data rates from the customer on HL223/HL224 CPs are discussed in paragraph 2.02.

1.04 The MJU is a circuit arrangement located in a hub office and is used to combine DDS (Digital Data System) signals to form a multipoint facility. From a control station the MJU splits the channel signal into identical branch signals for transmission toward outlying stations. The MJU also combines branch-originated signals and allows the signals from an active station to be transmitted over the channel to the control station. ▶Figure 2A shows the configuration for using HL68 CPs in the 4-branch FDX MJU. Figure 2B shows the configuration for

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using HL223 and HL224 CPs in the 4-branch FDX MJU.◀

1.05 Each MJU can serve from two to four stations; if more than four stations are to be served, the MJUs must be cascaded. The MJUs are cascaded by connecting port 0 of a downstream MJU to any one of the four ports (1-4) of an upstream MJU. The MJU branches and channels can be used as intraoffice or interoffice DDS transmission facilities.

1.06 The MJU operates FDX at the 64-kb/s rate. The MJU also contains circuitry to allow automatic testing from a 950A testboard MSU (multipoint signaling unit) located in the serving test center or other remote test systems. Every MJU in a hub office is also assigned an identical HUB ID (hub identification) code for testing purposes. Each MJU is synchronized to the DDS hub office timing supply through a CLKD (clock distribution) circuit. The CLKD circuit accepts the 8-kHz and 64-kHz clock signals from a BCPA (bay clock, power, and alarms) unit and distributes the clock signals to each MJU. The CLKD circuit also provides alarms for loss of clock signals.

1.07 Power for each MJU is obtained from the 5-volt power supply shelf via fuses in the MJU shelf assembly.

2. PHYSICAL DESCRIPTION

2.01 This part contains a physical description of MJU bays, a 2-shelf MJU assembly, FDX JCT (junction) circuit packs (▶HL68 or HL223 and HL224◀), and CLKD circuit packs (HL69).

2.02 ▶The HL68 circuit packs accept data from customer stations operating at 2.4, 4.8, 9.6, or 56 kb/s without rate selection. The HL223 and HL224 circuit packs accept data from customer stations at 2.4, 4.8, or 9.6 kb/s primary rate and, in addition, provide secondary channel capability. The 56 kb/s multipoint service is not offered on secondary channel circuits. A data rate select switch is provided on the HL223 printed wiring board. No adjustments are required on the HL224 CPs.◀

2.03 The JCT CPs and CLKD CPs are organized in shelves which are part of the bay. The basic unit consists of two shelves as shown in Fig. 3. These shelves contain slots for up to 32 MJU CPs and two HL69 CPs. Each of the two shelves has space for one HL69 CP in the middle of the shelf with eight MJU CPs on each side. ▶The faceplate of an HL68 is shown in Fig. 4. The faceplate and side view of an HL223 is shown in Fig. 5. The faceplace of an HL224 is shown in Fig. 6.◀

2.04 ▶The following guidelines allow for provisioning with HL68 or HL223/HL224 CPs in a 2-shelf MJU assembly unit.

(a) An HL68 in position 0-2 provides ports 0, 1, and 2. If ports 3 and 4 are required, a second HL68 is installed.

(b) An HL223 in position 0-2 provides ports 0, 1, and 2. If ports 3 and 4 are required, an HL224 is installed.

(c) The HL68 CPs ***must not*** be mixed with HL223 or HL224 CPs within the same multipoint junction unit.

(d) A 2-shelf MJU assembly may be equipped with any combination of HL68 or HL223/HL224 CPs (Fig. 3).◀

2.05 The FDX JCT CP contains MJU circuitry that handles a channel (port 0) and two branches (ports 1 and 2). When inserted into a shelf assembly, it becomes an FDX, 3-port (2-branch) MJU (FDX MJU ports 0-2). When another JCT is inserted into an adjacent slot in the shelf assembly so that both JCTs have a common channel, the arrangement becomes an FDX, 5-port (4-branch) MJU. The second JCT becomes the FDX MJU ports 3-4 connecting to branches 3 and 4. ▶The HL223 CP consists of two printed circuit boards attached to a single faceplate. The HL224 CP consists of a single printed wiring board attached to a single faceplate. The CP faceplates contain test points and an ejector latch for removing the CP from the shelf.◀

2.06 ▶The HL223 incorporates a 2-position switch located on the left side of the printed wiring board near the upper right-hand corner. Figure 5 defines the switch positions for various customer data rates. After the appropriate selection of data rates has been made, it should be marked on the faceplate label.◀

2.07 The CLKD HL69 CP consists of a single circuit board attached to a faceplate. The faceplate contains an ejector latch, test points, and a minor and

major alarm LED (light-emitting diode), MNL and MJL, respectively.

2.08 The HL68, ▶HL223, HL224◀, and HL69 CPs require +5 volts dc for proper operation. The MJUs and CLKD circuitry will operate properly within a temperature range of +40 degrees ferenheit to +140 degrees ferenheit and a relative humidity up to 95 percent.

2.09 A 2-shelf MJU assembly (J70177AH) has external dimensions of 18-1/2 inches high, 23 inches wide, and 12 inches deep, and weighs approximately 74 pounds with all CPs installed.

2.10 The MJU assemblies can be installed in a 7-foot or an 11-1/2 foot bay. Figure 7 shows a typical installation for the 7-foot bay. The left bay (J70177T) is the start-up bay and is installed first. Timing and alarms for the second bay (J70177U) are derived from the BCPA unit in the J70177T bay. Power for List 2 of the J70177T bay is derived from the power supply shelf in List 2 of the J70177U bay. Figure 8 shows a typical installation of an 11-1/2 foot bay.

2.11 A 2-shelf MJU assembly contains:

(a) sixty-six 940A connectors (space for sixteen 5-port MJUs and two CLKD CPs)

(b) ten KS-16672-L12 connectors

(c) one 298A terminal strip

(d) eighteen alarm indicating fuses.

The HL68 and ▶HL223◀ CPs require two 940A connectors (one for each circuit board) and each HL69 ▶and HL224 ◀ CP requires only one connector. Eight of the KS-16672-L12 connectors on the rear of shelves A and B are used to connect the MJU ports to the DSX-0 cross-connection. Of the two remaining KS-16672-L12 connectors, one is used to connect the CLKD CPs to the timing supply and the other is used to pass the timing from the timing supply to a second 2-shelf MJU assembly. The 298A terminal strip is prewired with six straps, some of which are removed at the time of installation to identify the MJU shelf with the HUB ID Code. The fuse panel (Fig. 9) consists of three fuse blocks: two blocks contain one fuse holder each and the third block contains 16 fuse holders. The single fuse holders are associated with the HL69 CPs and, of the remaining 16 fuse holders, FA1A-FA8A and FA1B-FA8B are associated with MJU CPs in shelf A and shelf B, respectively. All of the fuses are 70Ds (5-amp indicating type).

3. FUNCTIONAL DESCRIPTION

3.01 This part contains a functional description of the MJU and CLKD circuitry.

HL68

3.02 A block diagram of an HL68 CP FDX MJU (HL68 ports 0-2) is shown in Fig. 10. The circuitry of an HL68 CP can be divided into three sections: splitter, combiner, and test circuit.

3.03 The HL68 CP of the MJU receives bipolar signals from the direction of the control location, and the line terminator in the SPLITTER circuit converts the signals to unipolar format. The shift register regenerates the signal and the gating circuit either allows the signal to pass through toward the outlying stations or replaces it with an all zero signal, according to the state of the output from the blocking circuit in the test circuit. The timing buffers reestablish synchronism between the signal and the bit and byte clocks. The shift register and timing buffers delay the signal by one byte.

3.04 The line drivers convert the signal from unipolar back to bipolar form for transmission toward the branch stations.

3.05 The HL68 CP of the MJU receives bipolar signals from the branches and the line terminators in the COMBINER circuit convert the signal from bipolar to unipolar format. The shift registers regenerate the signals and determine if each byte is a data byte or control byte.

3.06 The converting circuit then provides the following modes of operation according to the input from the test circuit:

(a) Normal mode—Data bytes pass through and control bytes are converted to all ones bytes, i.e., bytes with all bits being a "1".

(b) Test mode—In this mode, signals from unselected branches are converted to all ones bytes and signals from the selected branch pass through unchanged. The output from the logic and the

blocking circuits determines the operation of the test mode.

3.07 The combiner gate combines the signals from the branches and the bytes from the character-generate circuit in the test circuit. If all branches are sending control codes, the idle generator generates the idle code toward the control location.

3.08 The combiner gate and timing buffers delay the signal by one byte so that the signal will be synchronized to the bit and byte clocks. The line driver converts the unipolar signal back to bipolar format for transmission toward the control location.

3.09 The TEST CIRCUIT provides a means for selecting a particular branch for test purposes. In the test circuit, the character-detect circuit observes bits 2 through 8 of each byte in the splitter shift register coming from the control channel and activates the appropriate state in the logic circuitry when the bytes are detected in the following sequence:

(1) TA (test alert) code

(2) MA (MJU alert) code

(3) Branch select 1, 2, 3, or 4 code

(4) UMC (unassigned multiplexer channel) code

(5) Idle code.

3.10 When a TA byte is detected, the MJU is placed in the initial test state. The blocking circuit causes the gating circuit and converting circuits to block transmission to and from the branches with the UMC code sent toward the branches. The TA byte (01101100) is generated by the character-generate circuit and transmitted back toward the channel via the combiner gate. After reception of TA bytes, the MJU receives MA bytes. For each MA byte (01110010) received, the MJU generates and transmits the MJU HUB ID toward the control location. If the MJU receives a code other than the MA code after receiving the TA code, the MJU is returned to normal operation. The MJU then receives branch select (BR-) bytes, the identity of which determines which branch (1-4) is selected for testing. The MJU generates and transmits a BR- byte back toward the control location for each BR- byte received. Control bytes of UMC code are received next, placing the MJU in the final test mode. In the final test mode, the selected MJU branch will be in a point-to-point communication state with the control channel. This will cause all bytes to pass freely in both directions and the other branches will have the UMC code sent to them. Reception of idle code from the control channel places the MJU back in normal operation.

HL69

3.11 A block diagram of the HL69 CP is shown in Fig. 11. Since the circuitry for the bit and byte clocks is similar, only the bit circuit will be described. The bit clock terminator buffers and amplifies the clock signal received from the BCPA unit. The timing alarm circuit checks the clock signal for the presence of clock pulses. If approximately ten clock pulses in succession are lost, the timing alarm circuit will light a minor alarm LED (MNL) on the CP faceplate and cause a minor alarm indication at the BCPA unit. If the clock signal is faulty or lost, the MJUs can receive clock signals from a second CLKD CP (B). If this clock signal is also faulty or lost, the timing alarm circuit will light a major alarm LED (MJL) on the CP faceplate and cause a major alarm indication on the BCPA unit.

3.12 For each failure of a negative clock transition, the bit failure blocking circuit will block the clock input. This ensures no loss of timing when the clock fails in the high state and loss of only one clock cycle when the clock fails in the low state. The bit timing drivers amplify the clock signal for distribution to the MJUs.

3.13 The MJUs and CLKD CPs obtain power from a 5-volt power supply shelf and each MJU and CLKD CP is fused separately at the MJU shelf location. For information concerning the power units in a 5-volt power supply shelf, refer to Practice 314-970-101.

HL223/HL224

3.14 ◗A block diagram of an HL223/HL224 CP FDX MJU (ports 0-2 and ports 3-4) is shown in Fig. 12. The circuitry of an HL223/HL224 CP can be divided into four sections.

(a) Input buffers

(b) Microprocessor

(c) Clock generator

(d) Output timing buffers.

3.15 The INPUT TIMING BUFFERS convert serial bipolar data into parallel data for each port for presentation to the microprocessor.

3.16 The MICROPROCESSOR accomplishes all upstream and downstream processing associated with the management of primary and secondary channel data. The microprocessor also responds to test stimulus from DDS test facilities.

3.17 The CLOCK GENERATOR provides phases of bit clock and byte clocks to allow synchronous FDX operation.

3.18 The OUTPUT TIMING BUFFERS convert parallel data to serial synchronous bipolar data.

4. REFERENCES

4.01 This part contains additional information, such as practices, CDs (circuit descriptions), and SDs (schematic diagrams), concerning the MJU and associated equipment.

4.02 Refer to CD- and SD-73086-01 for detailed information concerning the MJU and CLKD CPs.

4.03 The following AT&T practices contain additional information concerning the MJU and associated equipment:

PRACTICE	TITLE
314-901-011	Digital Data System—Serving Test Center—Private Line Circuit—Hub Identification Coding Plan
314-916-100	Digital Data System—Bay Clock, Power, and Alarms Circuit—Description
314-917-300	Digital Data System—Multipoint Junction Units and Auxiliary Circuits—Maintenance and Troubleshooting Procedures
314-917-500	Digital Data System—Multipoint Junction Units and Auxiliary Circuits—Test Procedures
314-970-101	Digital Data System—5-Volt Power Supply Shelf—Description
666-600-100	Digital Data System—950A Testboard (J70176A and B)—Description and Operation
666-600-500	Digital Data System—950A Testboard (J70176A and B)—Test Procedures

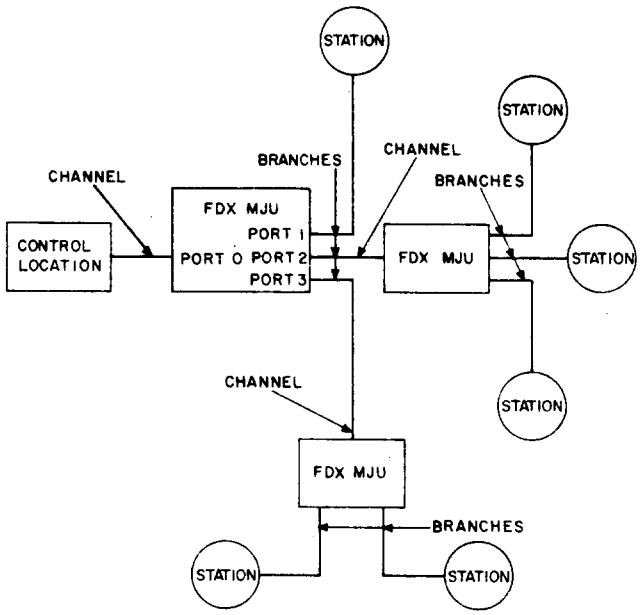
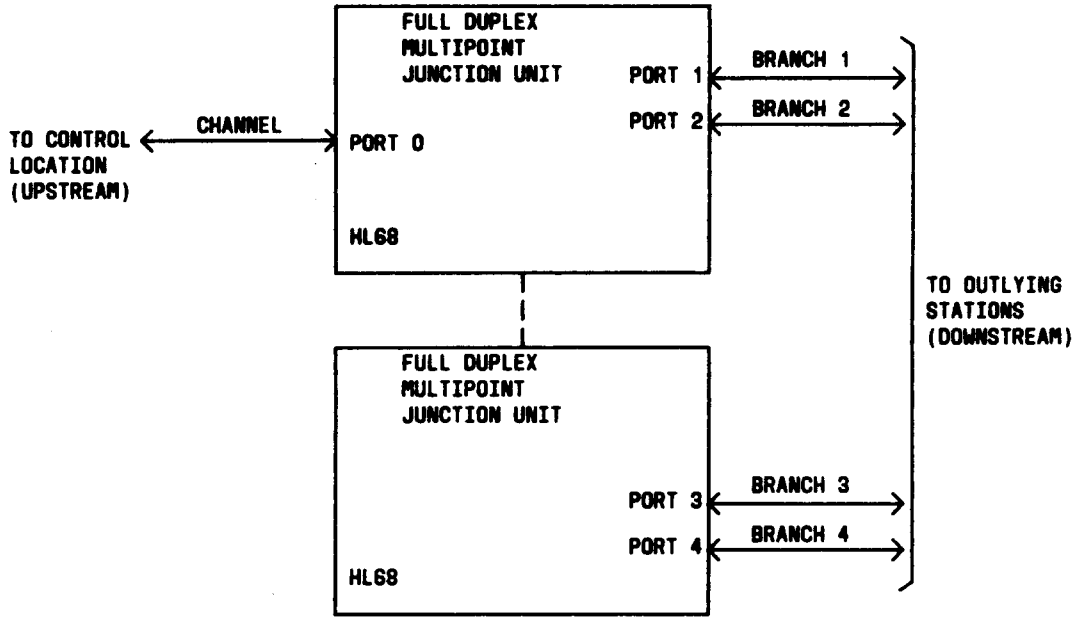
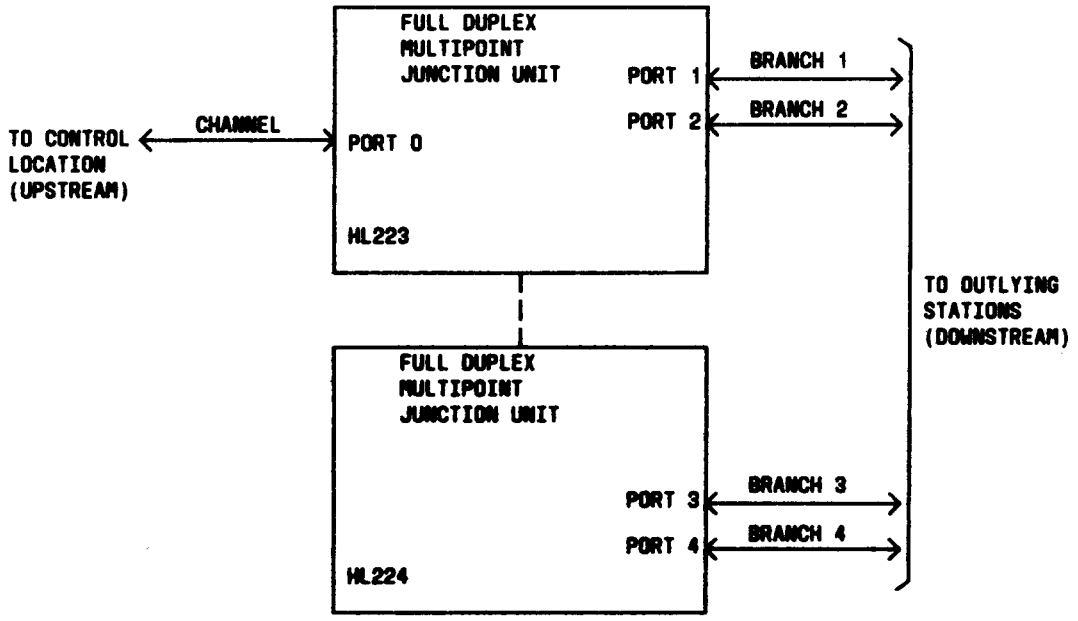


Fig. 1—Digital Data System Full-Duplex Multipoint Network



A. MJU with HL68



B. MJU with HL223/HL224

Fig. 2—4-Branch Full-Duplex Multipoint Junction Unit (HL223/HL224 or HL68)

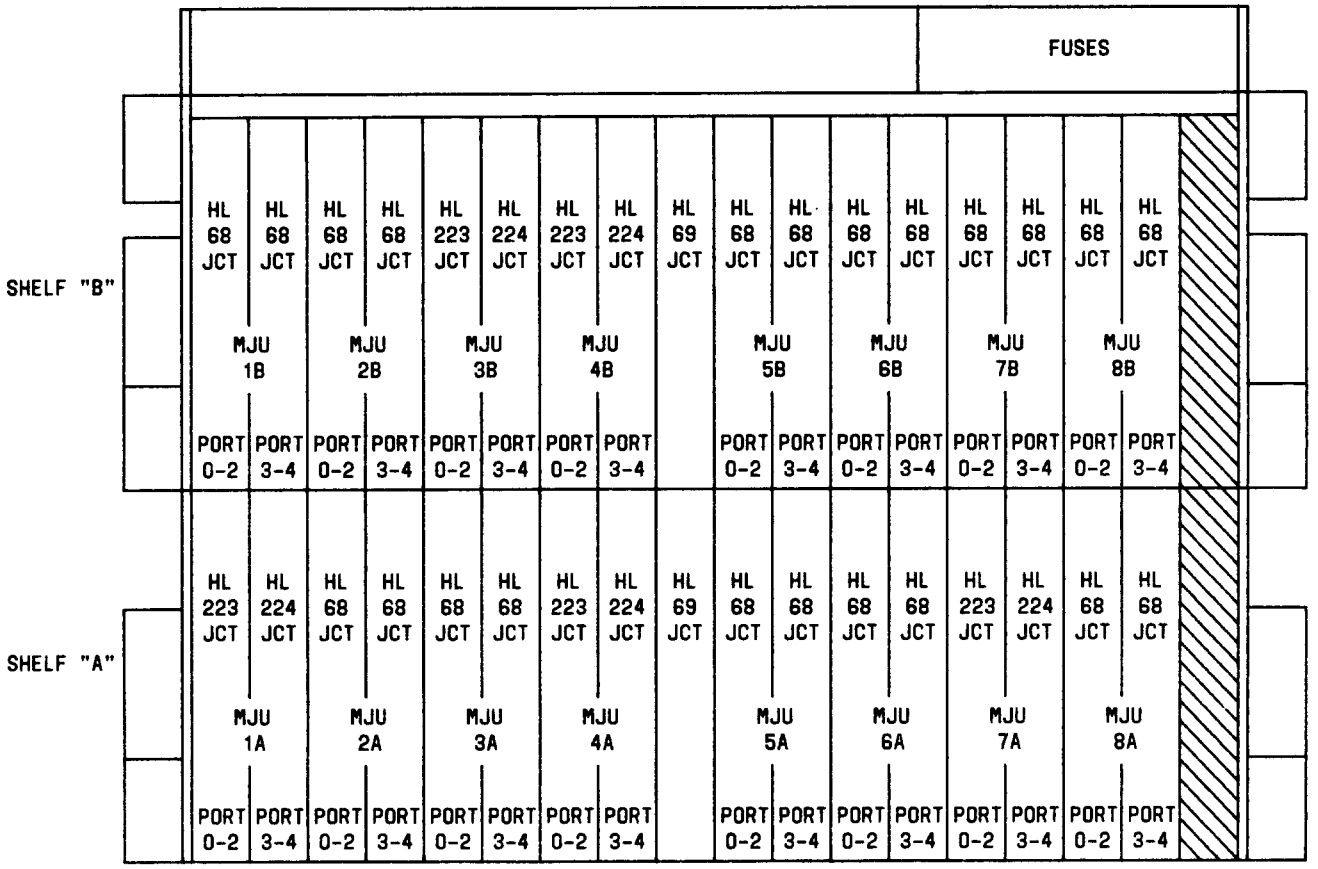


Fig. 3—2-Shelf Multipoint Junction Unit Assembly (J70177AH)

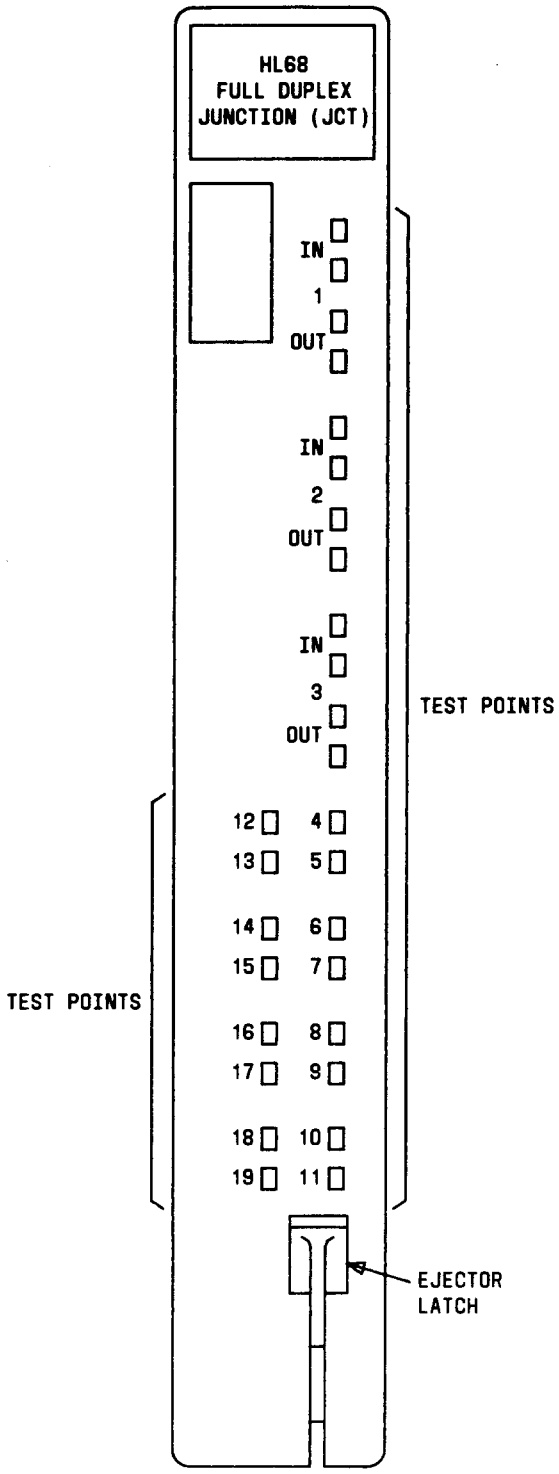


Fig. 4—Faceplate of an HL68 Circuit Pack

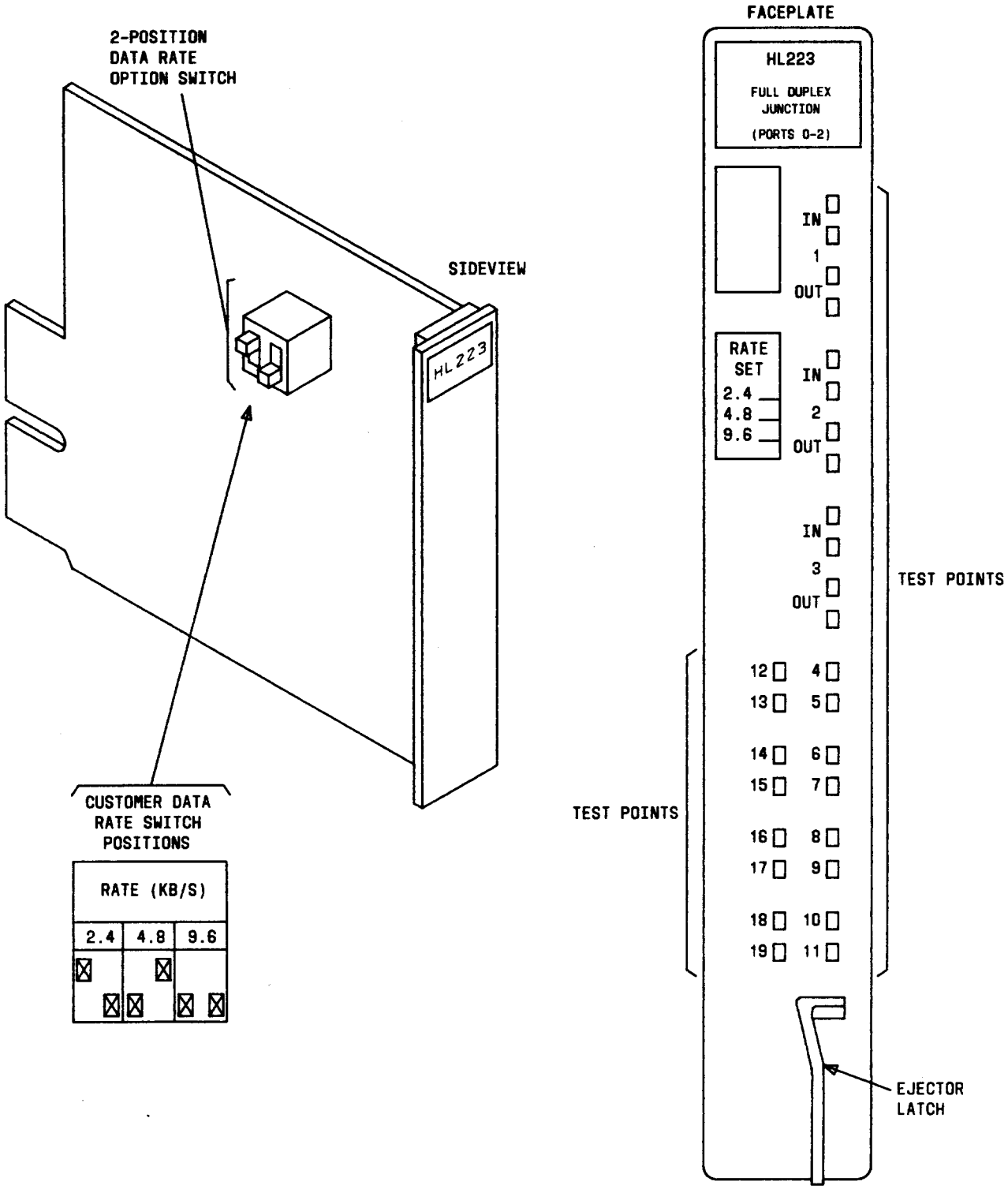


Fig. 5—Faceplate and Side View of an HL223 Circuit Pack

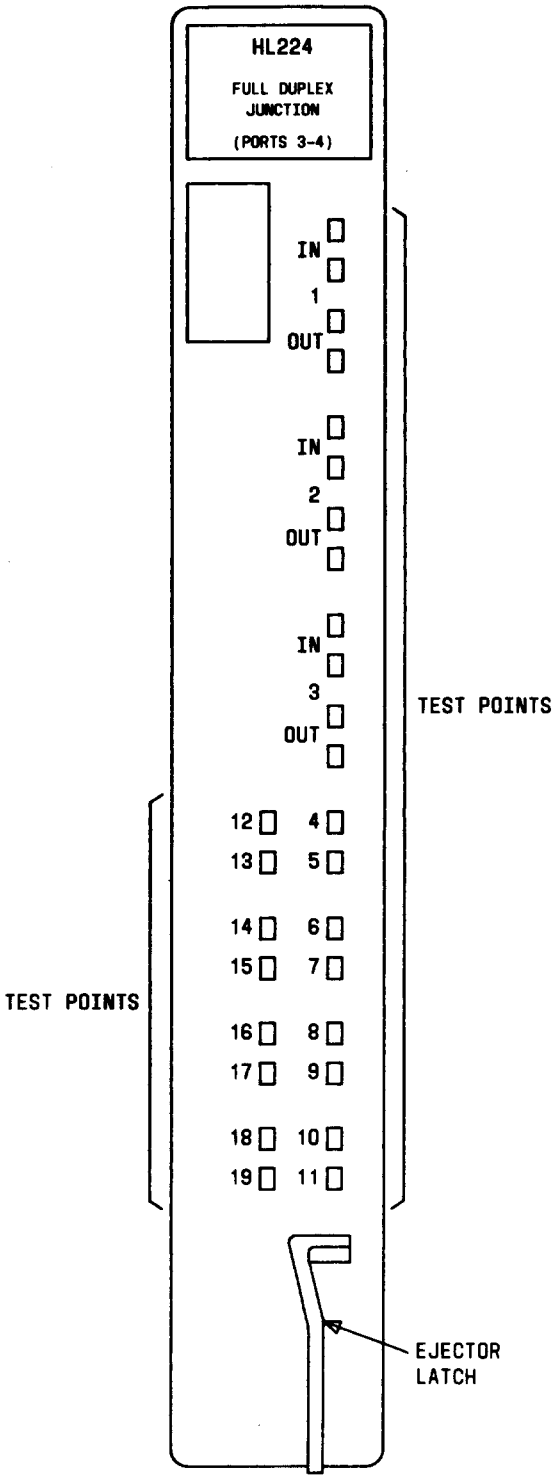


Fig. 6—Faceplate of an HL224 Circuit Pack

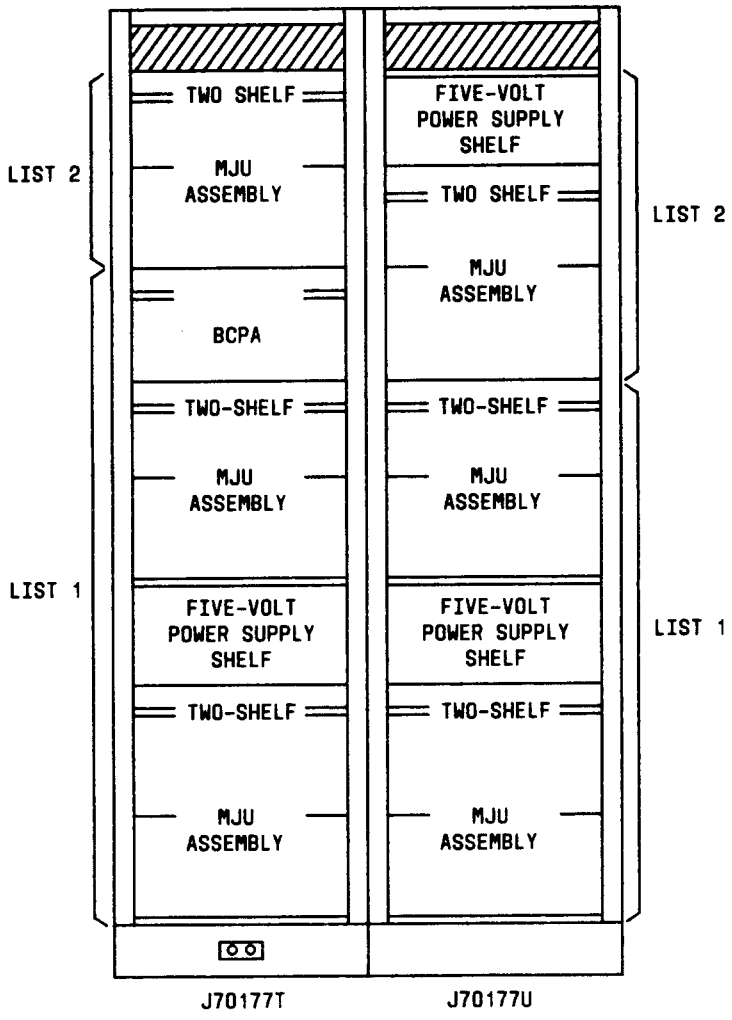


Fig. 7—Multipoint Junction 7-Foot Bay (J70177T and J70177U)

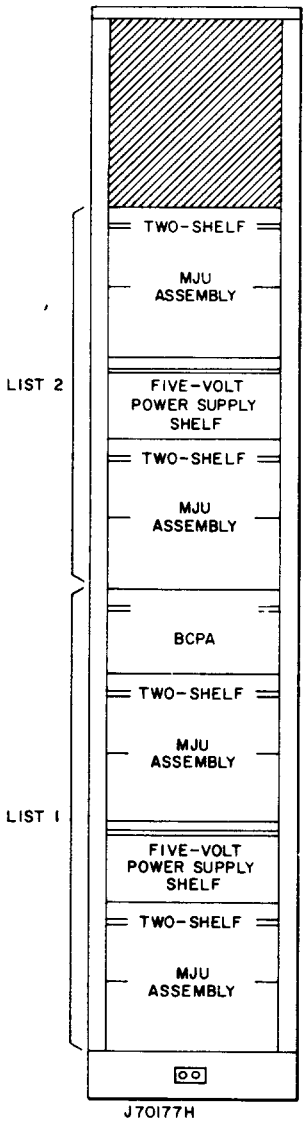


Fig. 8—Multipoint Junction 11 1/2 Foot Bay (J70177H)

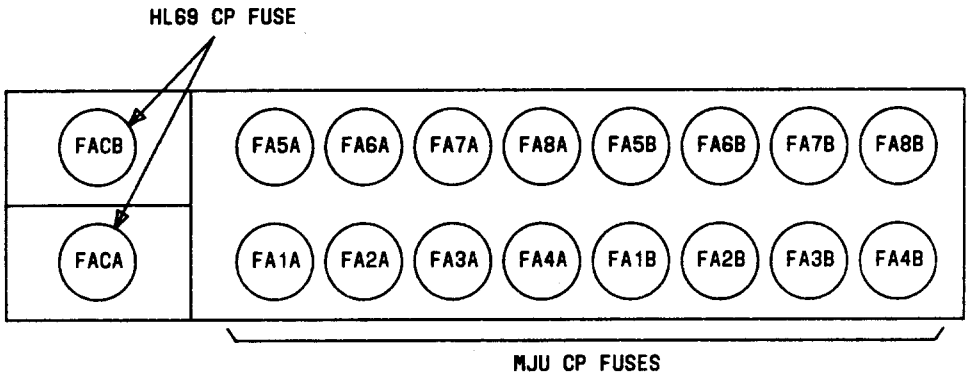


Fig. 9—Fuse Panel in Multipoint Junction Unit 2-Shelf Assembly

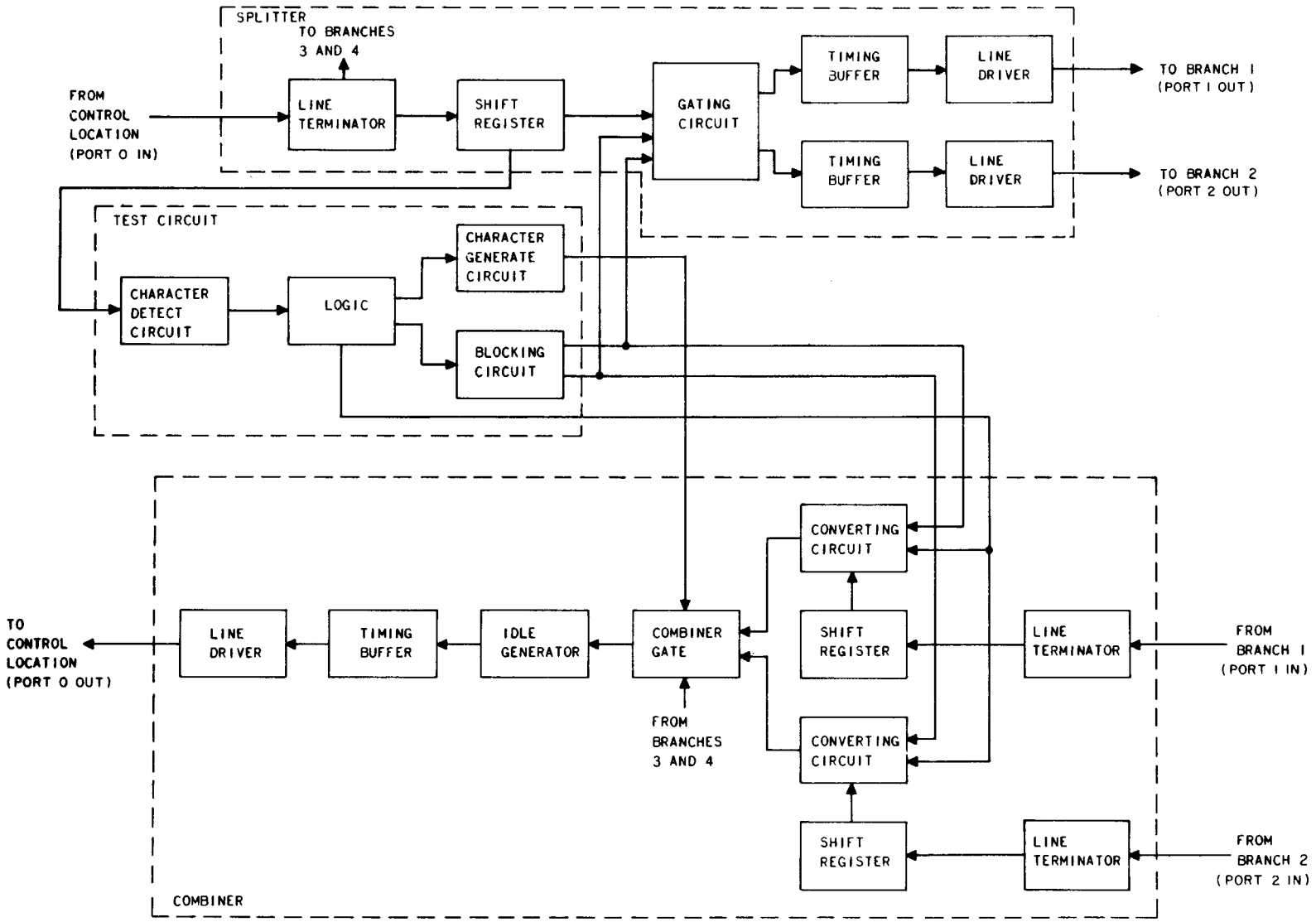


Fig. 10—Block Diagram of Full-Duplex Multipoint Junction Unit (HL68 CP)

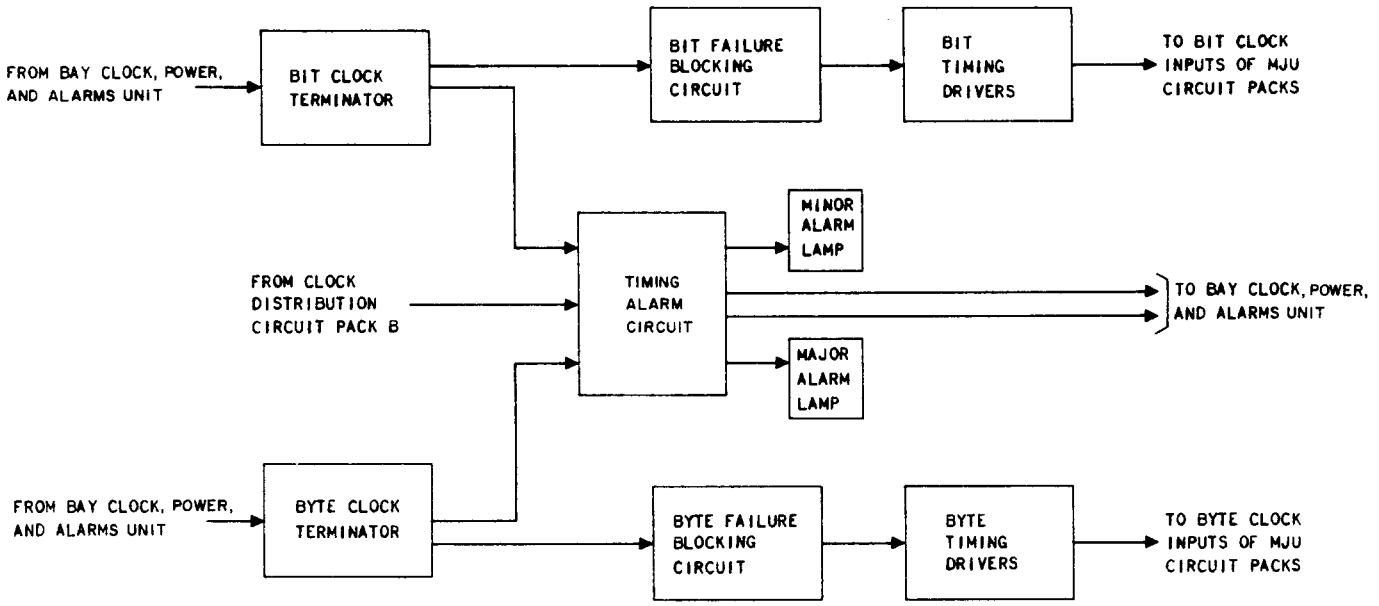


Fig. 11—Block Diagram of Clock Distribution Circuit Pack (HL69)

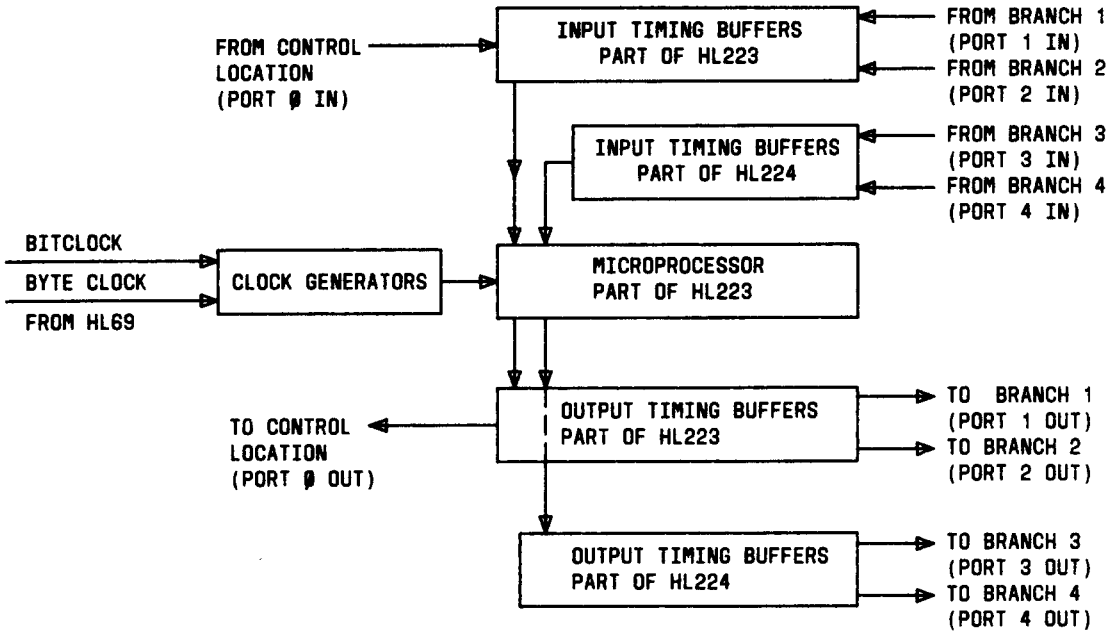


Fig. 12—Block Diagram of Full-Duplex Multipoint Junction Unit (HL223/HL224 CP)