DEMULTIPLEXER UNIT (DMUX:X0301)
FUNCTIONAL DESCRIPTION

1. GENERAL

1.01 This section is a cover sheet for the NEC America, Inc., Demultiplexer Unit (DMUX:X0301) Functional Description. This section is reproduced with permission of NEC America, Inc., and is equivalent to NEC practice NECA 365-407-404, Issue 1.

1.02 Whenever this section is reissued the reason(s) for reissue will be listed in this paragraph.

1.03 This section provides a general description of the Demultiplexer Unit (DMUX:X0301-).

1.04 If corrections are required in the attached document, use Form-3973 as described in Section 000-010-015.

1.05 If equipment design and/or manufacturing problems should occur, refer to Section SW 010-522-906 for procedures on filing an Engineering complaint.

2. ORDERING PROCEDURE

2.01 The Demultiplexer Unit (DMUX:X0301) may be ordered via the Southwestern Inventory Management System (SWIMS).

2.02 To order additional copies of this practice, use NECA 365-407-815SW as the section number.

3. REPAIR/RETURN

3.01 Malfunctioning units may be returned to NEC America, Inc., for repair.

Attachment: NEC America, Inc.
Demultiplexer Unit (DMUX:X0301)
Functional Description

NEC PRACTICE

NEC

NECA 365-407-404
Issue 1, December 1986

DEMULTIPLEXER UNIT (DMUX : X0301)

FUNCTIONAL DESCRIPTION

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♦ DEMULTIPLEXER UNIT (DMUX:X0301) ♦
FUNCTIONAL DESCRIPTION

CONTENTS

ILLUSTRATIONS

TABLES

1. GENERAL

1.01 This practice provides a general description of the Demultiplexer unit (DMUX; X0301-) and contains the following information:

(1) Description

(2) Functional operation

(3) Indicators

(4) Strapping selection

1.02 Whenever this practice is reissued, the reason for reissue will be listed in this paragraph.

2. DESCRIPTION

2.01 This unit consists of one epoxy-glass printed wire board (PWB) and associated circuit components. Printed circuit wiring is etched on both sides of the PWB.

2.02 LEDs for indicating the operational status are located on the front edge of this unit.

2.03 This unit is mounted in the FD-2240A E8980 shelf with back board connectors J17 (Sys 1), J14 (Sys 2), J10 (Sys 3) and J7 (Sys 4). The unit inputs and outputs are terminated at a connector on the rear of the PWB.

2.04 The unit designation, unit code, manufacturing date and serial No. are printed on the right side surface of the connector.

2.05 The lower front edge of the PWB is fitted with ejector to facilitate insertion and removal of the board from the shelf. A CLEI and bar code label is placed on the surface of the ejector. See Figures 4-1 and 4-2.

2.06 There are five groups for DMUX unit. Table 2-1 lists these groups.

◆Table 2-1◆

DMUX Unit's Groups

No.	Unit Code and Group	Power Voltage	Line Code	Remarks
1	X0301A	-48 Vdc	AMI	DS1 primary version
2	X0301A1	-48 Vdc	AMI	
◆ 3	X0301B	-24 Vdc	AMI	◆
◆ 4	◆ X0301A2	-48 Vdc	AMI or B8ZS	◆DS1 new version◆
◆ 5	◆ X0301B2	-24 Vdc	AMI or B8ZS	

3. FUNCTIONAL OPERATION

3.01 The demultiplexer (DMUX) unit receives 6.312 Mb/s data signal and clock signal from the on-line HS INF unit. It demultiplexes the data signal into four 1.544 Mb/s (DS1) bipolar data signals. Figures 3-1 and 3-2 show block diagram of the DMUX unit.

3.02 Incoming 6.312 Mb/s data signals enter the unit at the 6M DATA inputs. Incoming clock signals enter the unit at the 6M CLK inputs. The 6M DATA and 6M CLK inputs for each unit are selected according to the position in the shelf where the unit is mounted, or according to control signals received from the CTRL unit at MON SEL 1, 2 and 3.

A. DMUX Digital Interface

3.03 The DMPX (LSI) digital interface chip contains a receive counter, a data demultiplexer, a synchronization circuit, a stuff bit decoder and a remote loopback bit detector. It also contains 6M DATA and 6M CLK signal selection circuit and the four write clock signals generating circuit.

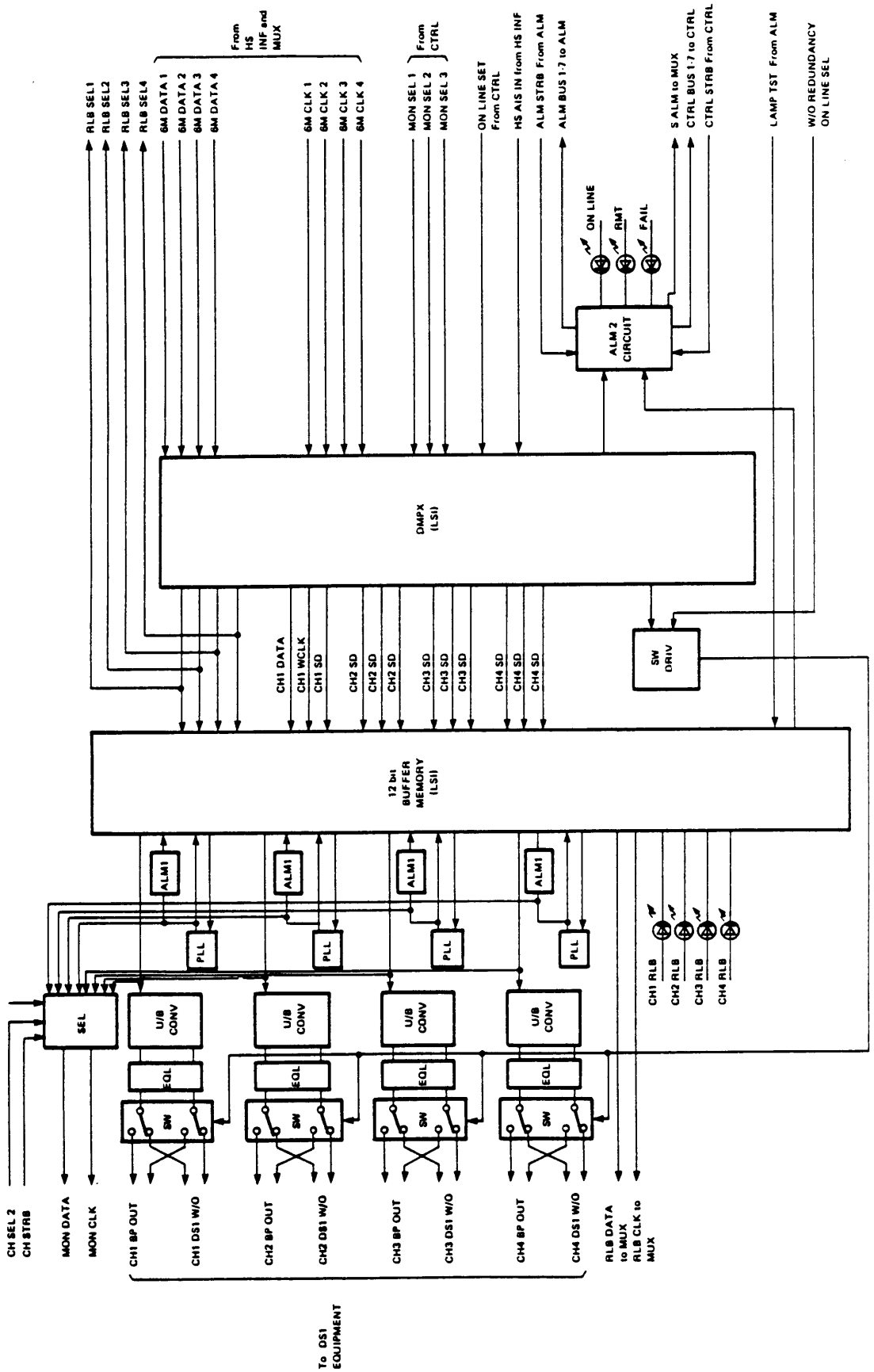
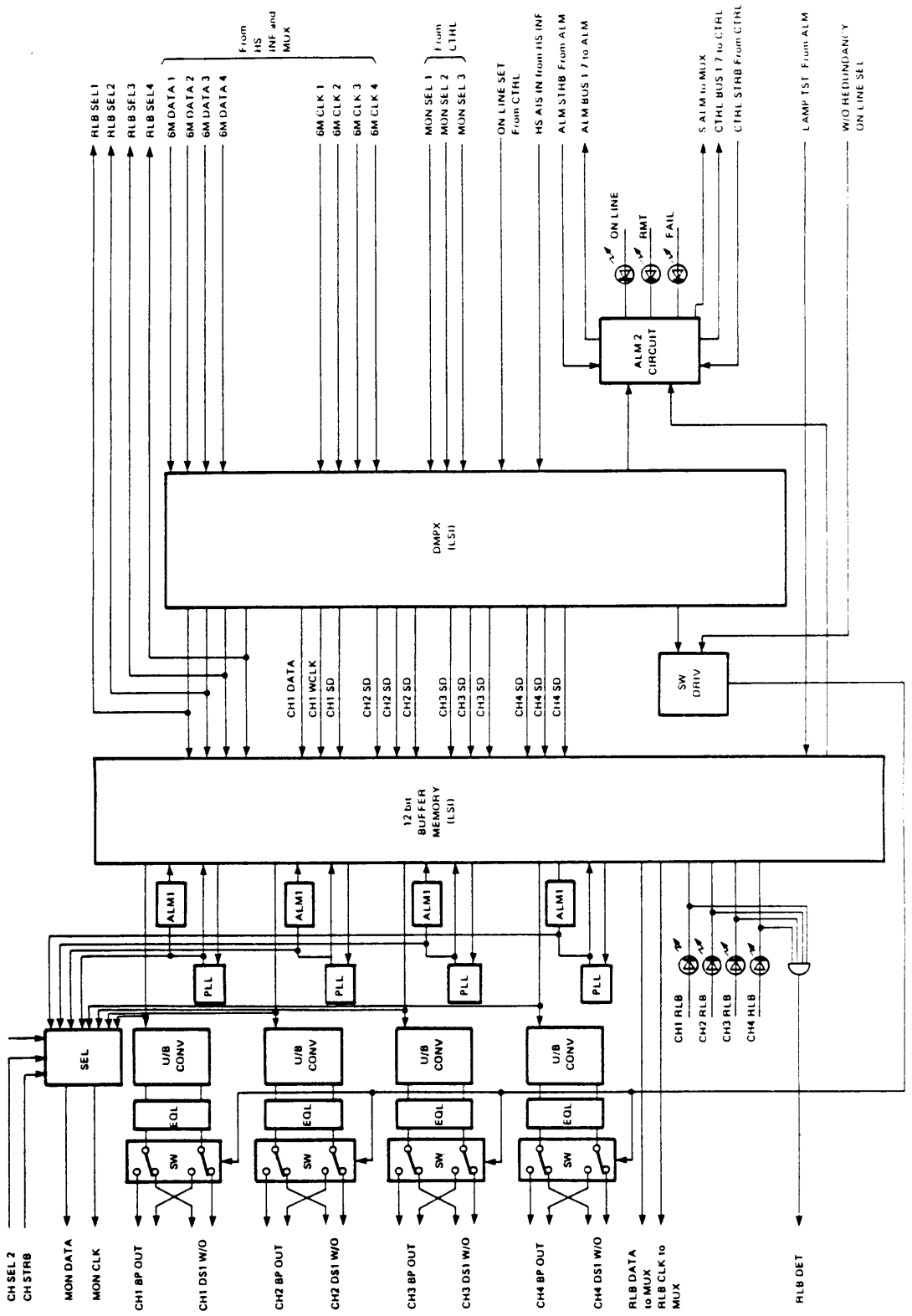


Figure 3-1 DMUX Unit (Grp: 0A00) Block Diagram

NOTE: Switching positions in this figure show on line side when the system is redundant configuration.



NOTE: Switching positions in this figure show on line side when the system is redundant configuration.

♦ Figure 3-2 DMUX Unit (Grp: 0A01/0B00) Block Diagram ♦

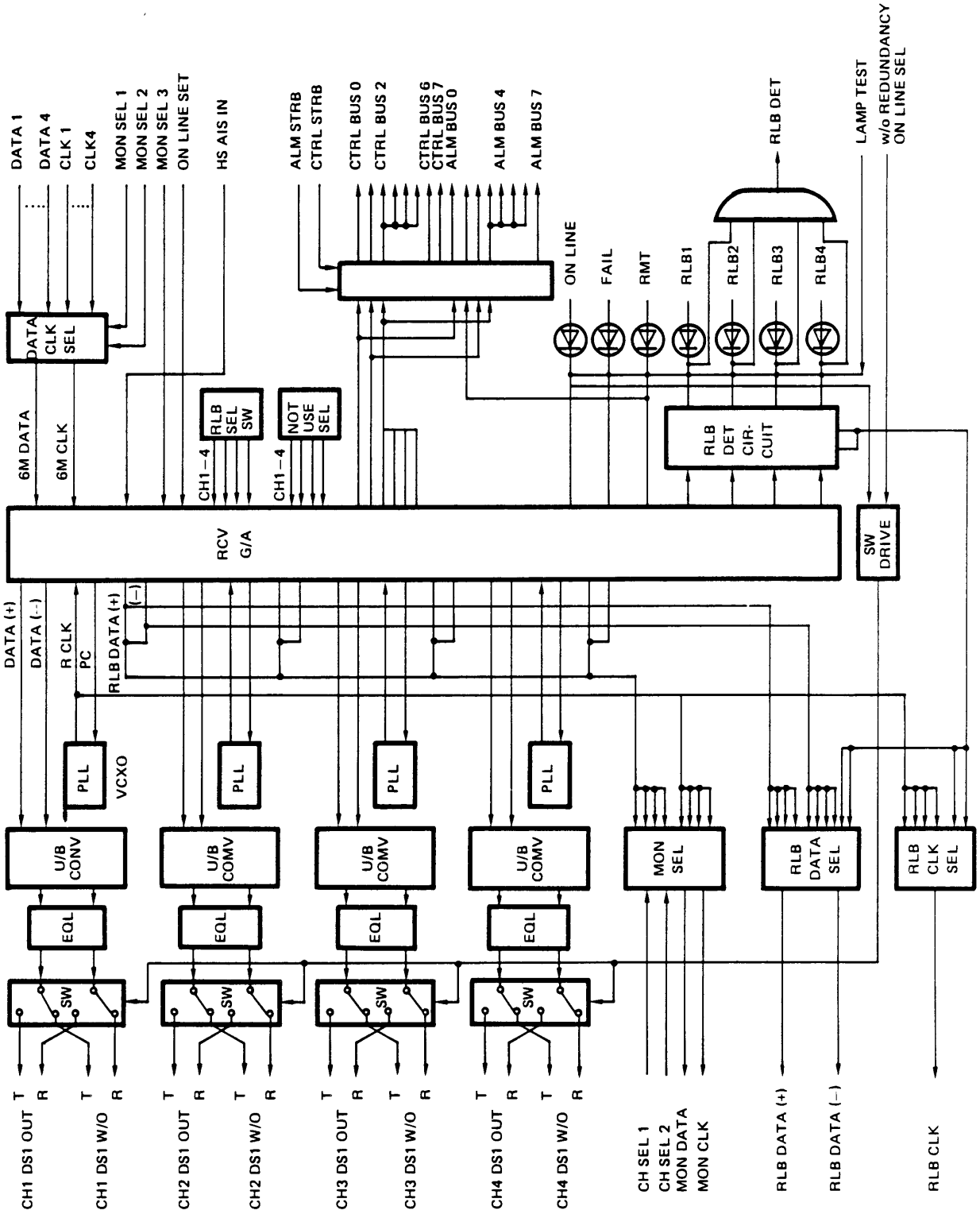


Figure 3-3 DMUX Unit (GRP: 0A02/0B02) Block Diagram

3.04 The incoming 6M DATA and 6M CLK signals enter the DMPX and go to the signal selection circuit. This circuit selects the correct input signals according to the control signals appearing at selection control inputs MON SEL 1, 2 and 3 and ON LINE SET. The selected signals are then routed to the appropriate internal circuitry for further processing.

3.05 The selected clock signal goes to the receive counter. The receive counter develops the timing signals required for demultiplexing the data signal and extracting the framing bits, stuff bits and remote alarm bit.

3.06 The selected data signal goes to sync decoder and frame bit decoder circuits. These circuits together with the multiframe sync circuit and receive counter circuit, develop and maintain synchronization between the LS muldem units of the local and remote equipment.

3.07 The data demultiplexer circuit demultiplexes the 6.312 Mb/s data signal into four 1.544 Mb/s signals. These signals leave the DMPX and go to the 12 bit BUFFER MEMORY (LSI). They are also sent to a stuff decoder within the DMPX which extracts the stuff bits and send them to the receive clock gate circuit and the remote loopback bit detector circuit.

3.08 The stuff decoder also controls the write clock generator. The outputs of this generator circuit are the write clock signals utilized to clock data into the BUFFER MEMORY. When a stuff bit is detected, the write clock generator is momentarily stopped so the stuff bit will not be transferred into the BUFFER MEMORY.

3.09 A remote alarm combiner circuit within the DMPX monitors signals from the frame sync and multiframe sync circuits, and in case a failure is confirmed, its information is transferred from alarm circuit 2 (ALM2) to MUX unit as S ALM signal, and then transferred to the remote station via HS INF unit.

B. LSI Buffer Memory

3.10 In addition to buffer memory, the LSI buffer memory chip contains remote loopback (RLB) gates, a data forcing circuit and circuitry for generating phase locked loop (PLL) control signals.

3.11 The write clock and receive data go to the buffer memory of the BUFFER MEMORY chip. Read clock signals, generated by PLL circuits, read the data out of the buffer memory. PLL control signals from the BUFFER MEMORY chip control the PLL frequencies so as to maintain an even output bit rate for each channel. PLL frequency increases when buffer overflow is detected, and decreases when buffer underflow is detected.

3.12 The output data and PLL clock signals also go to a remote loopback (RLB) gate and to a data forcing circuit. When an RLB request is received from the distant end, the RLB gate sends the designated channel's data and clock signals to the RLB DATA and RLB CLK outputs of the BUFFER MEMORY. As with the receive side, the data forcing circuit places a steady 1 or 0 signal on the line if the 6.312 Mb/s signal is lost, or if out of sync condition is detected at the 6.312 Mb/s level (AIS active).

3.13 Unipolar-bipolar converters convert the outgoing 1.544 Mb/s RCV DATA signals to bipolar form. The bipolar signals then pass through a passive equalization circuit. This circuit compensates for differences in output cable length, and can be configured in one of three ways by strap selection.

C. Alarm Function

3.14 PLL alarm circuits (ALM 1) monitor the read clock signals generated by the PLLs. When a PLL output is lost, ALM 1 sends an alarm signal to the BUFFER MEMORY, which is turn sends a CH FAIL signal to the ALM 2 circuit.

3.15 The alarm circuit 2 (ALM 2) monitors the alarm signals generated by the DMPX and CH FAIL (1-4) output from LSI buffer memory. When DMPX detects loss of the 6M CLK signal (from the HS INF unit), ALM 2 generates an alarm signal. The generated alarm is combined with the LS alarm signal from the DMPX sync loss detector, and the resulting signal is sent to the CTRL and ALM units through bus line.

D. RCV G/A (GRP:0A02/0B02 only)

3.16 Receive Gate Array (RCV G/A) mainly consists of 6M DMPX section, MEMORY section, B8ZS CODER section and ALM section.

3.17 6M DATA and 6M CLK are demultiplexed into four 1.544 Mb/s signals in the 6M DMPX section. The data and CLK signals separated into CH1 through CH4 are input to the MEMORY section.

3.18 The MEMORY section contains 12-bit buffer memory for each CH and writes the data by the Write Clock (W CLK) from the DMPX section. The written data is read by the 1.5M level Read Clock (R CLK) from the PLL VCXO. The read data is then input to the B8ZS CODER section.

3.19 If B8ZS code is selected byn the SW on the DMUX unit, the data is code converted to B8ZS and becomes the output of G/A. If AMI code is selected, the data is output as it is.

3.20 Each output data and CLK signal from G/A is input to the unipolar/bipolar conversion circuit (U/B CONV) and converted from unipolar signal to bipolar signal.

3.21 Each converted bipolar signal goes to the equalizer circuit which allows to compensate for the difference of output cable length in two steps by strapping. After passing through the equalizer circuit, the signal becomes DMUX unit output via relay SW.

3.22 The ALM section has various functions such as RLB, ALM detection, etc., and ON LINE LED, FAIL LED, RMT LED and RLB1 through RLB4 LEDs are lit by the output from the ALM section. In addition, RCV G/A has optional functions such as AMI B8ZS switching, X bit polarity switching (0 or 1), polarity section for fixing 1.5M line output data, ALM Inhibit function for other manufacturer's equipment, and various RLB receive functions, all of which are enabled by the operation of SW on the unit.

4. INDICATORS

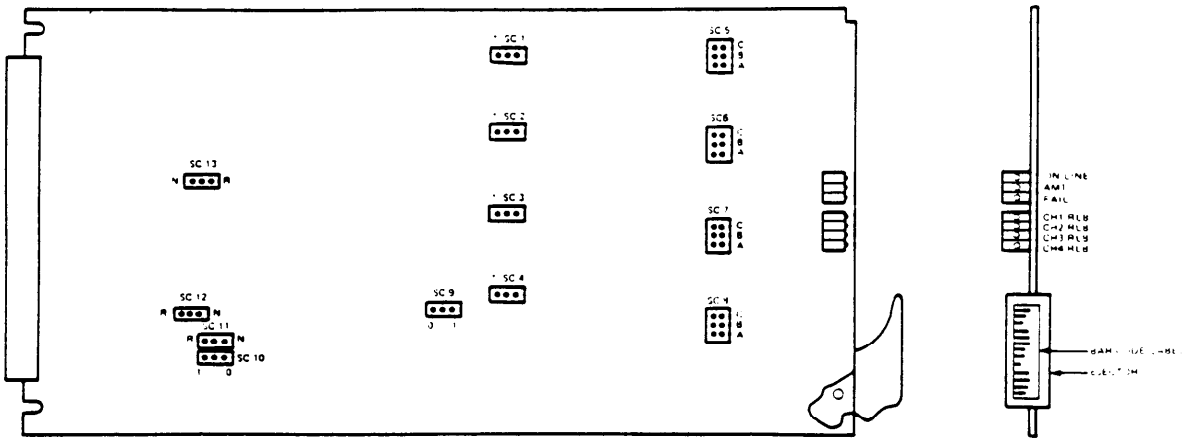
4.01 Table 4-1 shows the indicators on the DMUX unit. Phsical location on the unit are shown in Figures 4-1 and 4-2.

Table 4-1
DMUX Unit Indicators

Feature	Type	Indicator	Function
Status	Green LED	ON LINE	Lights when this unit is used for on-line circuit.
Status	Red LED	RMT	Lights when detects an alarm signal from the remote station.
Alarm	Red LED	FAIL	Lights when an alarm occurs in this unit.
Status	Red LED	CH 1 RLB CH 2 RLB CH 3 RLB CH 4 RLB	Lights when RLB SW of corresponding CH (MUX unit) is ON at the remote station and detects this commands signal.

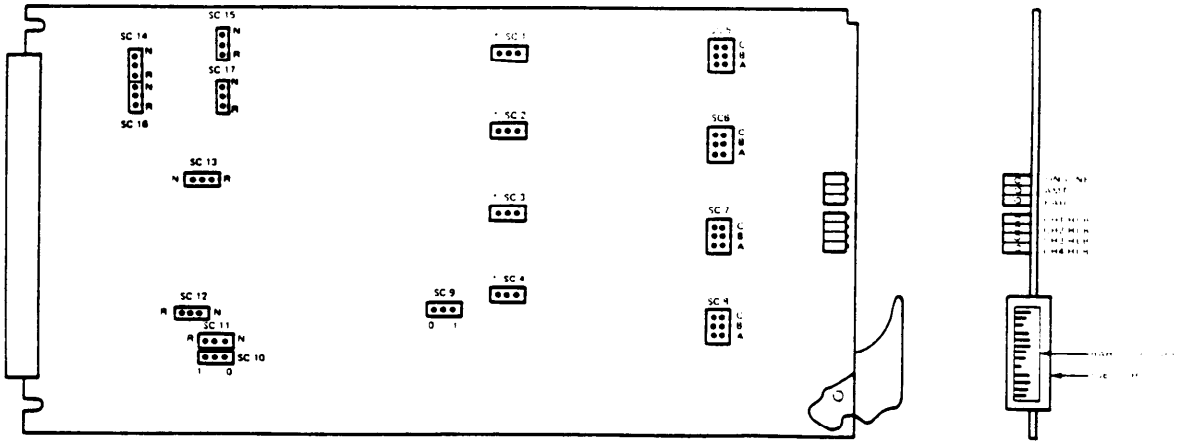
5. STRAPPING SELECTION

5.01 As shown in Figures 4-1 and 4-2, there are 13 strapping locations (Grp:0A00), 17 strapping locations (Grp:0A01/0B00), and 15 strapping locations (Grp: 0A02/0B02) on the DMUX unit. Detailed strapping selections are described in NEC practice NECA 365-407-203.



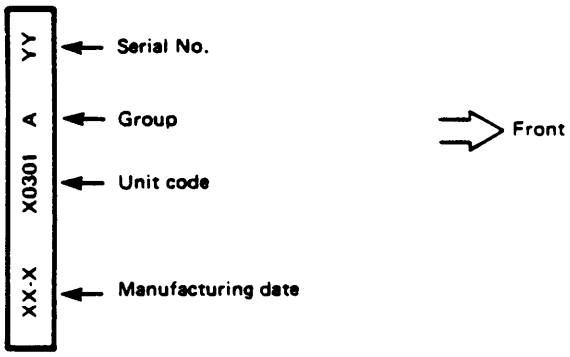
* Factory adjustment

(A) DMUX (Grp: 0A00) Unit



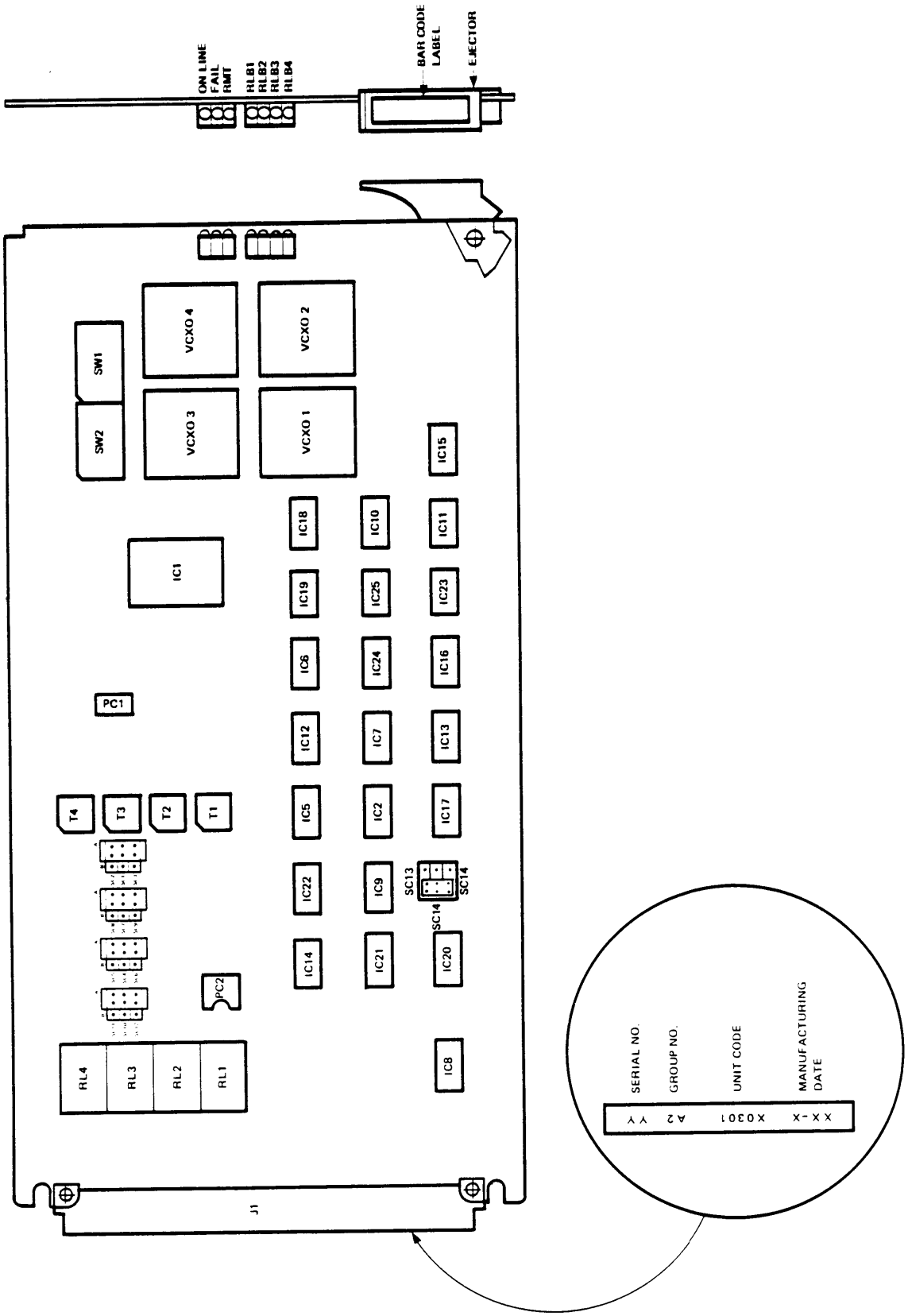
* Factory adjustment

◆ (B) DMUX (Grp: 0A01/0800) Unit ◆



NOTE: Printed on the right side surface of the main board connector.

Figure 4-1 DMUX Unit Indicators



♦Figure 4-2 DMUX Unit (GRP:0A02/0B02) Indicators♦