MULTIPLEXER UNIT (MUX:X0300)
FUNCTIONAL DESCRIPTION

1. GENERAL

1.01 This section is a cover sheet for the NEC America, Inc., Multiplexer Unit (MUX:X0300) Functional Description. This section is reproduced with permission of NEC America, Inc., and is equivalent to NEC practice NECA 365-407-406, Issue 1.

1.02 Whenever this section is reissued the reason(s) for reissue will be listed in this paragraph.

1.03 This section provides a general description of the Multiplexer Unit (MUX:X0300).

1.04 If corrections are required in the attached document, use Form-3973 as described in Section 000-010-015.

1.05 If equipment design and/or manufacturing problems should occur, refer to Section SW 010-522-906 for procedures on filing an Engineering complaint.

2. ORDERING PROCEDURE

2.01 The Multiplexer Unit (MUX:X0300) may be ordered via the Southwestern Inventory Management System (SWIMS).

2.02 To order additional copies of this practice, use NECA 365-407-817SW as the section number.

3. REPAIR/RETURN

3.01 Malfunctioning units may be returned to NEC America, Inc., for repair.

Attachment: NEC America, Inc.
Multiplexer Unit (MUX:X0300)
Functional Description

NEC PRACTICE

NEC

NECA 365-407-406
Issue 1, December 1986

MULTIPLEXER UNIT (MUX : X0300)

FUNCTIONAL DESCRIPTION

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MULTIPLEXER UNIT (MUX)
X0300-0A00/0A02/0B02
FUNCTIONAL DESCRIPTION

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ILLUSTRATIONS

TABLE

1. GENERAL

1.01 This practice provides a general description of the Multiplexer unit (MUX: X0300-) and contains the information as listed below.

(1) Description

(2) Functional operation

(3) Controls and indicators

(4) Strapping selection

1.02 Whenever this practice is reissued, the reason for reissue will be listed in this paragraph.

2. DESCRIPTION

2.01 This unit consists of one epoxy-glass printed wire board (PWB) and associated circuit components. Printed circuit wiring is etched on both sides of the PWB. On the left side surface (viewed from front) of the PWB, the components are mounted.

2.02 LEDs and switch for controlling and indicating the operational status are located on the front edge of this unit.

2.03 This unit is mounted in the FD-2240A E8980A shelf with back board connectors J18 (Sys 1), J15 (Sys 2), J11 (Sys 3) and J8 (Sys 4). The unit inputs and outputs are terminated at the connector on the rear of this PWB.

2.04 The unit designation, unit code, manufacturing date and serial No. are printed on the right side surface of the connector.

2.05 The lower front edge of the PWB is fitted with ejectors to facilitate insertion and removal of the board from the shelf. A CLEI and bar code label is placed on the surface of the ejector. See Figures 4-1 and 4-2.

2.06 There are four groups for MUX unit. These groups lists in Table 2-1.

♦Table 2-1♦

MUX Unit's Groups

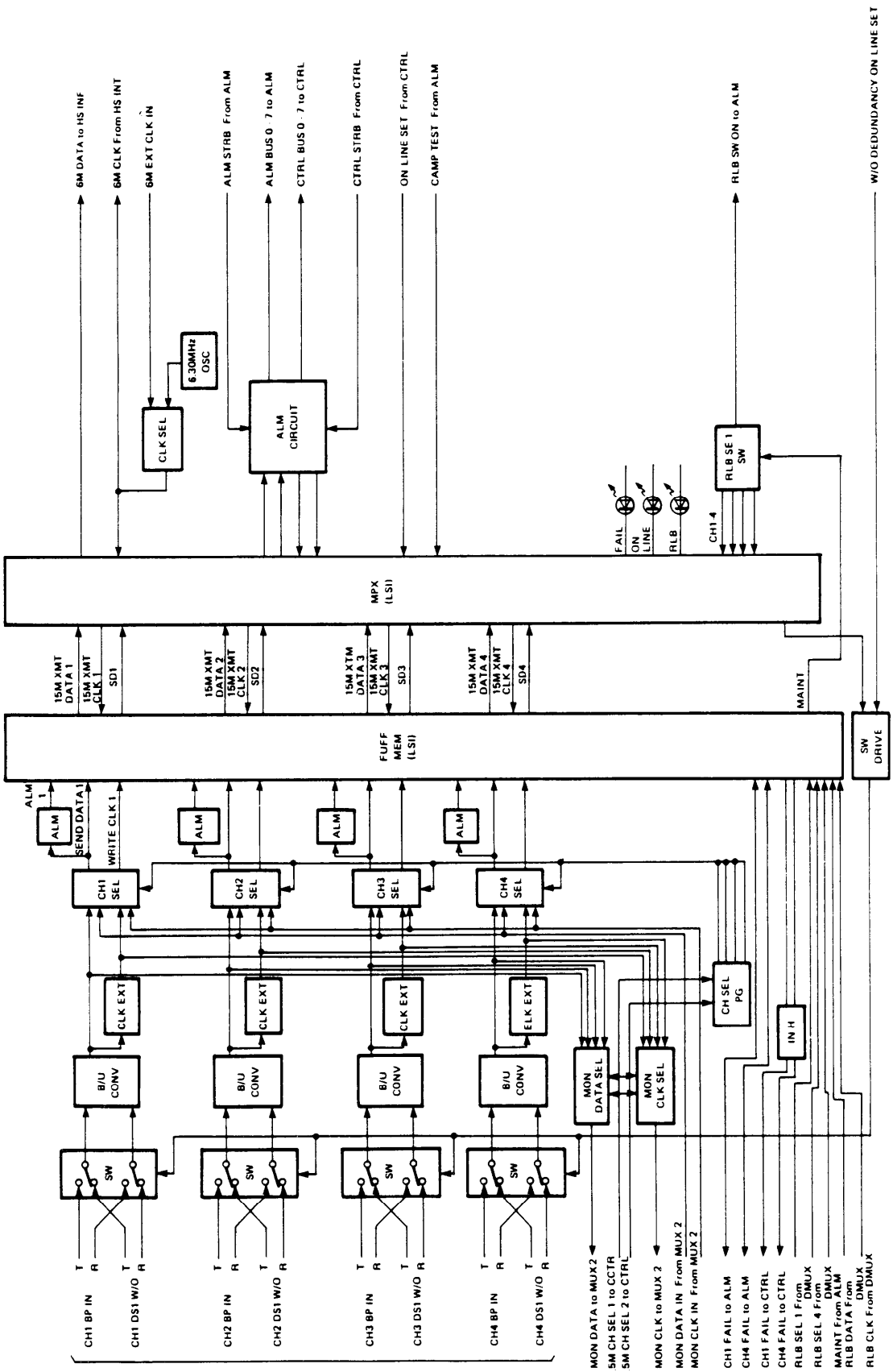
No.	Unit Code and Group	Power Voltage	Line Code	Remarks
1 ♦	X0300A	♦ -48 Vdc	AMI	DS1 primary version
2	X0300B	-24 Vdc	AMI	
3	X0300A2	-48 Vdc	AMI or B8ZS	DS1 new version
4	X0300B2	-24 Vdc	AMI or B8ZS	

3. FUNCTIONAL OPERATION

3.01 The MUX unit receives four 1.544 Mb/s (DS1) bipolar data signals and multiplexes them into a single 6.312 Mb/s serial data signal. The MUX unit block diagram are shown in Figures 3-1 and 3-2.

A. 1.544 Mb/s Input Path

3.02 Incoming DS1 data signals, via relay switches (SW), go to the bipolar-to-unipolar converters (B/U CONV) which convert them from bipolar to unipolar (TTL level) form and then go to channel selectors (CH SEL). B/U CONV output signals are also processed by clock extractors (CLK EXT) and they also go to CH SELs. CH1 through CH4 SELs select input signals whether they are output data from B/U CONV or monitor data and send them out to buffer memory LSI (BUFF MEM). The alarm circuits 1 (ALM 1) make data loss detection on output data from CH SEL and the detected result is sent to LSI BUFF MEM.



NOTE: This figure shows that switching status is in non-redundant configuration.

♦ Figure 3-1 MUX Unit (GRP: 0A00) Block Diagram ♦

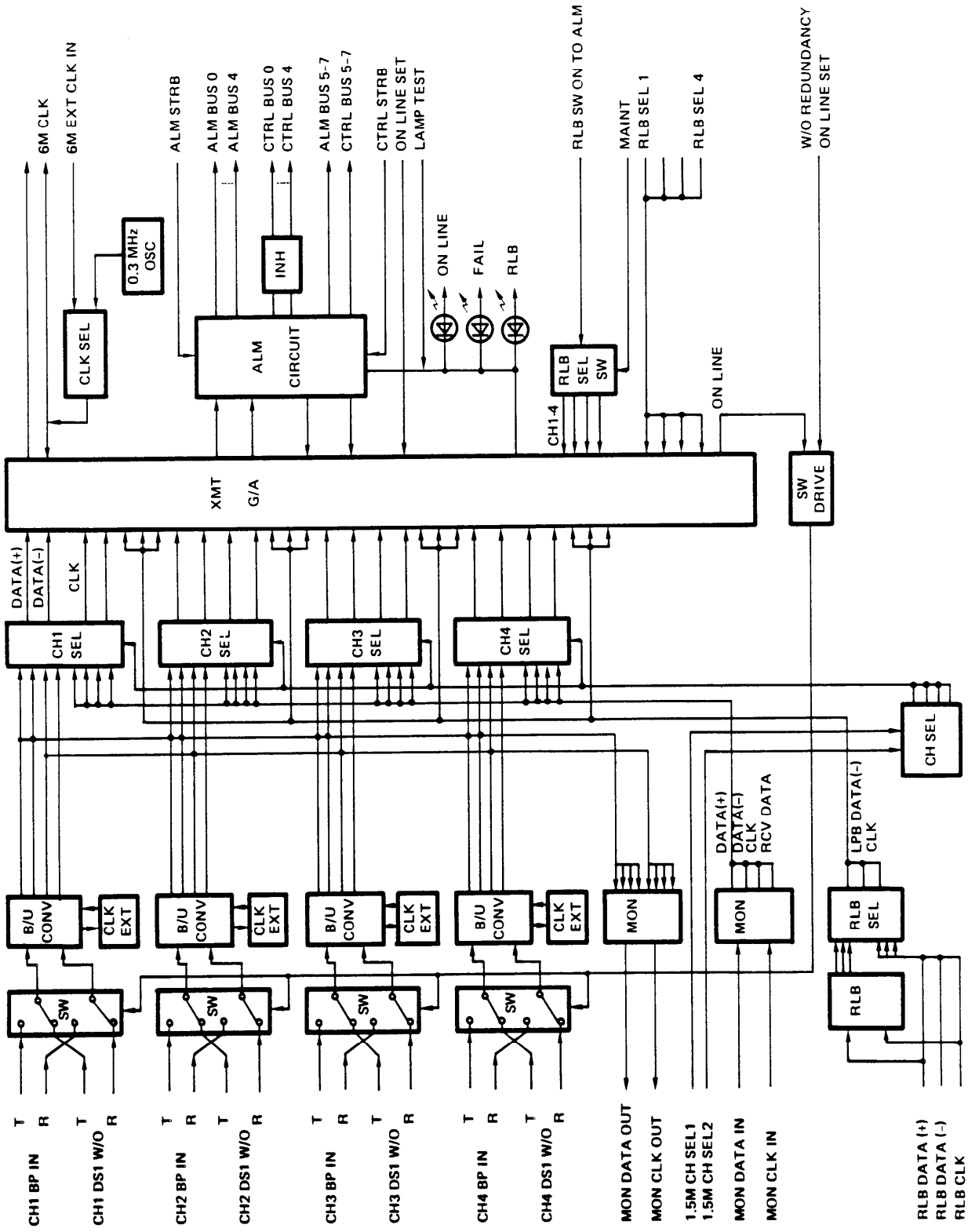


Figure 3-2 MUX Unit (GRP: 0A02/0B02) Block Diagram

B. LSI Buffer Memory

3.03 In addition to 11 bit buffer memory circuitry, the BUFF MEM also contains remote loopback (RLB) gates, read clock/write clock phase comparison circuits, and data forcing circuits. The RLB gate for each channel selects the data and clock signals to be transferred to the buffer memory circuit for that channel. During normal operation the send data and send clock signals are passed. A remote loopback command signal from the remote station (detected by the DMUX unit's RLB decoder) cause the appropriate RLB gate to change states and pass the receive (RLB) data and clock signals. When this occurs, the normal transmit function of the RLB mode channel is inhibited as long as the channel remains in RLB mode. The signals appearing at RLB DATA and RLB CLK come from the DMUX unit, and are the received signals of the channel selected for loopback at the remote station.

3.04 A read clock (1.5M XMT CLK) then reads the data from the buffer memory. The buffer memory output (1.5M XMT DATA) goes to the multiplexer LSI (MPX). The LSI buffer memory's phase comparison circuit compares the read clock and write clock signals. If the phase difference becomes less than a predetermined amount, a stuff demand (SD) signal is sent to the MPX, thereby inhibiting the read clock and avoiding buffer memory overflow or underflow.

3.05 The data forcing circuit passes the data to the MPX as long as data is being received. If the ALM circuit detects that no data is being received, the data forcing circuit places a steady 1 or 0 (as selected by strap selection) on the 1.5M XMT DATA line.

C. MPX Digital Interface (LSI)

3.06 The MPX digital interface chip contains a transmit counter, a frame time slot generator, a stuff bit generator, a data multiplexer and a remote loopback command multiplexer. It adds the required stuff bits to the four incoming DS1 data signals and then combines them to form a 6.312 Mb/s unipolar data signal. The resulting 6.312 Mb/s data, which includes the various control bits and framing bits, then goes to the high-speed interface (HS INF) unit.

3.07 The 6.312 Mb/s transmit clock signal from clock selector (CLK SEL) enter the MPX and is applied to the chip's internal transmit counter. The 6.312 Mb/s clock which is supplied to the MPX can be selected from either the internal oscillator of the unit or external clock generator, by means of strapping selection.

3.08 Each incoming stuff demand (SD) signal from the LSI buffer memory goes to a stuff demand latch circuit. A timing signal from the frame time slot generator latches the circuit and the latched output is sent to a stuff bit generator which then inserts a stuff bit. A multiframe bit generator codes the location of the stuffed bit into the overhead bit pattern to allow the distant end destuff circitry to properly remove the stuff bit.

3.09 After inserting the stuff bits, the data multiplexer combines the four 1.5M XMT DATA signals to form a 6.312 Mb/s data signal. The remote loopback command multiplexer adds remote loopback command bits and the data multiplexer adds framing bits and control bits to the data.

D. 6.312 Mb/s Output Path

3.10 The outgoing 6.312 Mb/s data and clock signal go to the high speed interface (HS INF) unit. (There are two types of HS INF unit; one is 6M OPT unit and other is DS2 INF unit.)

E. Alarm and Control Function

3.11 The MUX unit communicates with the ALM unit using the following signals:

(1) CH FAIL 1 through 4 : Alarm data bus signal for DS1 CH 1 through 4 failure

(2) MUX FAIL : Alarm data bus signal for MUX failure

(3) ALM STROB : Control signals from ALM unit

(4) RLB SW ON : RLB switch ON information to send to ALM unit

(5) ALM TST : Low level signal input when ALM TST SW on ALM unit is ON

(6) MAINT : MAINT SW on ALM unit ON to send to MUX unit

3.12 The MUX unit communicates with the CTRL unit using the following signals:

(1) CH FAIL 1 through 4 : Control bus signal for DS1 CH 1 through 4 failure

(2) MUX FAIL : Control data bus signal for MUX failure

(3) CTRL STROB : Control signal from CTRL unit

F. XMT G/A Circuit (GRP:0A02/0B02 only)

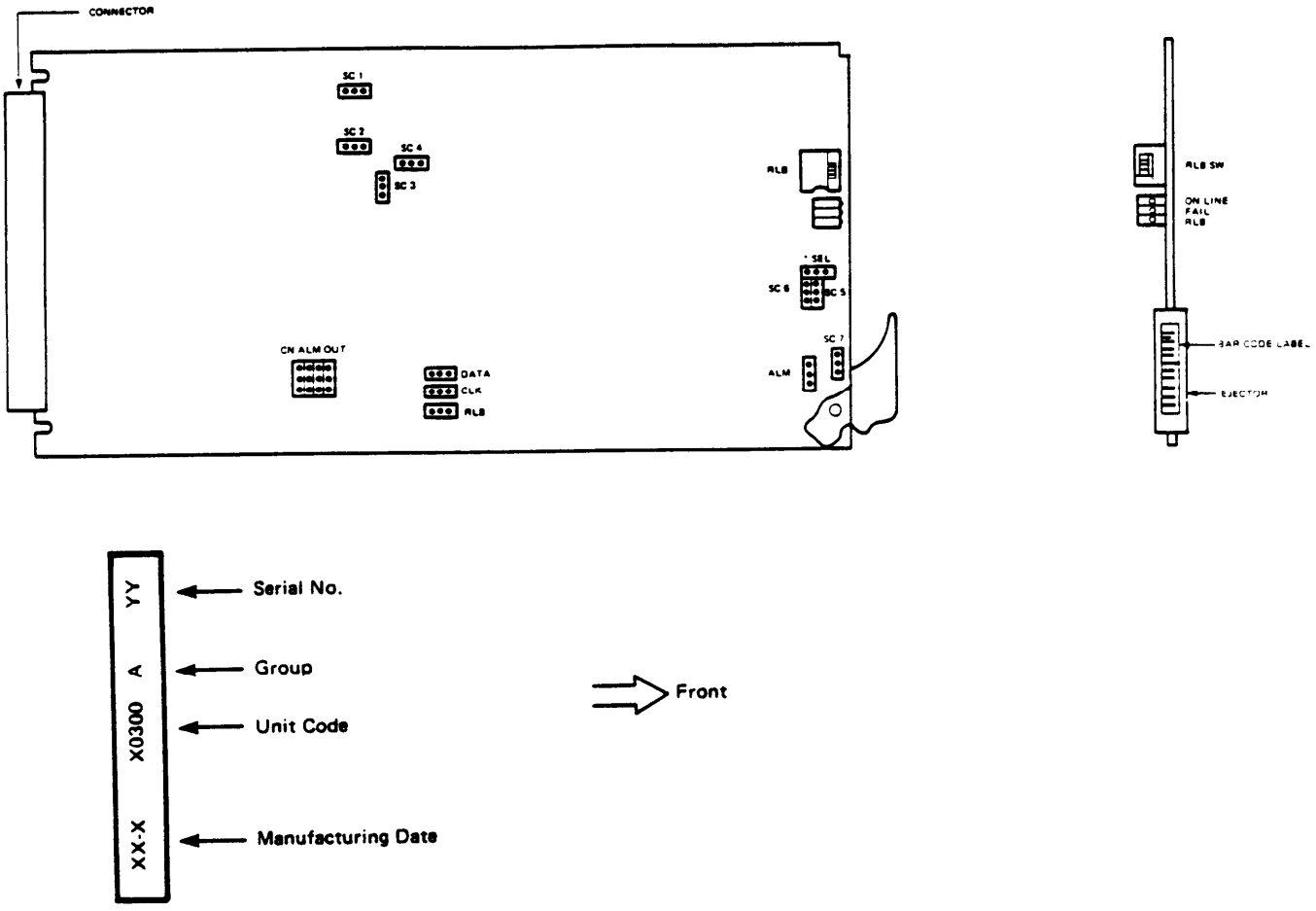
3.13 Transmit Gate Array (XMT G/A) circuit mainly consists of the B8ZS DECODER section, MEMORY section, 6M MPX section and ALM section.

3.14 Data and CLK from each CH SEL circuit first go to each B8ZS DECODER section in G/A. If the data is AMI coded, it merely passes through this circuit. If the data has been converted to B8ZS code, it is decoded in the circuit and sent to the MEMORY section.

3.15 The MEMORY section contains 11-bit buffer memory and writes the data by 1.5M level Write Clock (W CLK). The written data is read by external 6M level Read Clock (R CLK), and each CH data and clock are output to the 6M MPX section.

3.16 Data and clock of CH1 through CH4 read from buffer memory are multiplexed in the 6M MPX section and sent out as one 6M data and 6M clock.

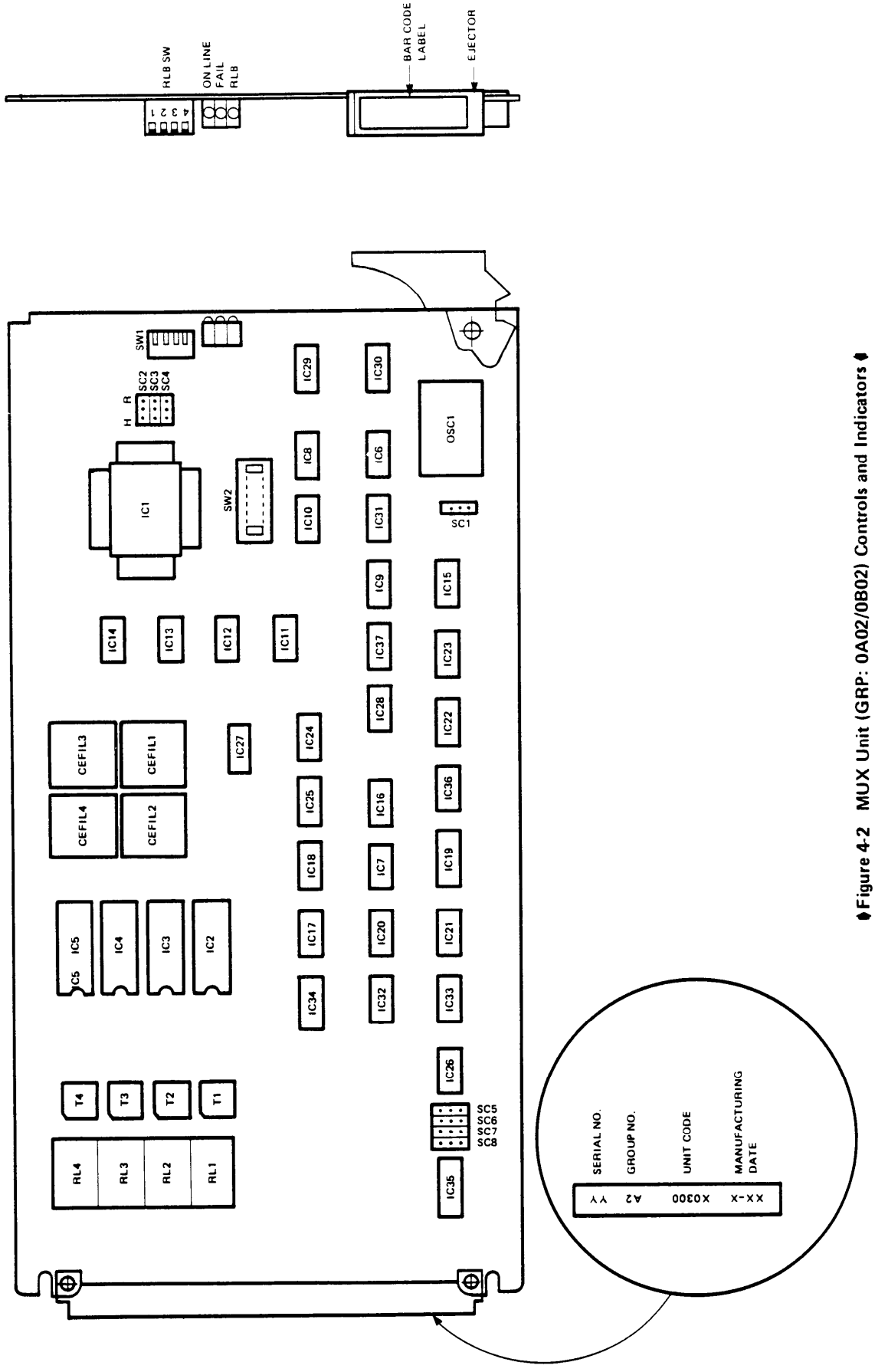
3.17 The ALM section has various functions such as RLB, ALM detection etc., and ON LINE LED, FAIL LED and RMT LED are lit by the output from the ALM section. The 6M DATA and 6M CLK output from the XMT G/A are sent to the HS INF.



NOTE: Printed on the right side surface of connector.

◗ Figure 4-1 MUX Unit (Grp: 0A00/0B00) Control and Indicators ◖

♦DELETE♦



♦Figure 4-2 MUX Unit (GRP: 0A02/0B02) Controls and Indicators♦

5. STRAPPING SELECTION

5.01 The MUX units have, as shown in Figures 4-1 and 4-2, 16 strapping locations (GRP:0A00/0B00) and 8 strapping locations (GRP:0A02/0B02). Detailed strapping selections are described in NEC practice NECA 365-407-203.